

The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Components Group



**Supplement to
The TTL
Data Book**

**for
Design Engineers**

TEXAS INSTRUMENTS
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ALAN

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Supplement to The TTL Data Book for Design Engineers

First Edition



TEXAS INSTRUMENTS
INCORPORATED

IMPORTANT NOTICES

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

Information contained herein is supplemental to the data published in CC-411. Where information on a product is given in this supplement as well as in CC-411, the information contained herein supercedes the data published in CC-411.

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**Supplement to
The TTL Data Book
for Design Engineers
First Edition**

This 400-page supplement provides detailed specifications on 171 new Texas Instruments TTL device types. Included are:

- 9 high-performance Schottky-clamped[†] TTL memory functions
- 48 Series 54LS/74LS Schottky-clamped functions plus five functions with improved specifications
- 15 Series 54S/74S Schottky-clamped logic functions
- 15 functions in the 54/74 family
- 4 beam-lead chips

As an example, the memory circuits include two 1024-bit PROM's, two 256-bit RAM's, and four 2048-bit ROM's. The low-power Schottky and 54S/74S add high-performance counters, arithmetic elements, and even a complete accumulator, the SN54S281/SN74S281. Series 54/74 adds dual 4-bit counters, bus-driving circuits with 3-state outputs, and other functions designed to simplify and reduce the costs of systems. Furthermore, several new devices are included that are in a new 20-pin plastic dual-in-line package with pins on 300-mil row spacing.

Margin tabs in this supplement correspond to those in the first edition of *The TTL Data Book for Design Engineers* (CC-411) even though in some of these sections no new or revised data are included in this supplement.

Both the numerical and the functional indexes are complete listings of all TI TTL integrated circuits available at this writing. Moreover, the functional index provides a more up-to-date listing of packages available for each device type than previously published information. Page numbers with an "S-" prefix refer to pages in this supplement; page numbers without a prefix refer to pages in *The TTL Data Book for Design Engineers*.

In the SSI section of this supplement, only the new device types are included. However in the MSI/LSI section, where a new device type has been added, all device types that appear in the same data sheet with the new type are included with their complete specifications. For example, the SN54LS156 and SN74LS156 are additions covered by this supplement, but since they are included in the same data sheet as the SN54155, SN74155, SN54156, SN74156, SN54LS155, and SN74LS155, complete specifications on all of these types are included.

The 38510/MACH IV Procurement Specification is included in its entirety and now incorporates revised level IV (SNH) processing and technological criteria for preap of complex circuits. The new listing of JAN MIL-M-38510 integrated circuits provides a current cross-reference from circuit type number to 38510 slash sheet and from 38510 slash sheet to circuit type number.

This supplement includes an errata for the first edition of *The TTL Data Book for Design Engineers*. This errata includes the corrections that have already been made on those pages that reappear in this supplement.

Another addition is the section on IC sockets and interconnection panels. TI produces a complete line of these products, and their inclusion here provides a handy reference for the design engineer.

[†]Integrated Schottky-barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

Although *The TTL Data Book for Design Engineers* and this supplement offer design and specification data only for TTL integrated circuits, additional technical data for any TI semiconductor/component product are available from your nearest TI field sales office, local authorized TI distributor, or by writing directly to:

Marketing and Information Services
Texas Instruments Incorporated
P.O. Box 5012 MS 308
Dallas, Texas 75222

Additional information on IC sockets and interconnection panels is available from the above sources, or by writing directly to:

Texas Instruments Incorporated
Connector Product Marketing
34 Forest Street
MS 11-1
Attleboro, Massachusetts 02703

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- **Functional/Selection Guide**

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SN54L91	SN74L91	S-136	S-136	SN54LS123	SN74LS123	S-58	S-58
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SN5492A	SN7492A	S-127	S-127	SN54S124	SN74S124	S-62	S-62
SN54LS92	SN74LS92	S-127	S-127	SN54125	SN74125	142	83
SN5493A	SN7493A	S-127	S-127	SN54126	SN74126	142	83
SN54L93	SN74L93	S-127	S-127	SN54128	SN74128	104	83
SN54LS93	SN74LS93	S-127	S-127	SN54132	SN74132	98	83
SN5494	SN7494	234	234	SN54LS132	SN74LS132	S-67	S-67
SN5495A	SN7495A	S-141	S-141	SN54S132	SN74S132	98	83
SN54L95	SN74L95	S-141	S-141	SN54S133	SN74S133	86	84
SN54LS95B	SN74LS95B	S-141	S-141	SN54S134	SN74S134	142	84
SN5496	SN7496	S-147	S-147	SN54S135	SN74S135	269	269
SN54L96	SN74L96	S-147	S-147	SN54136	SN74136	271	271
SN54LS96	SN74LS96	S-147	S-147	SN54LS136	SN74LS136	271	271
SN5497	SN7497	248	248	SN54LS138	SN74LS138	274	274
SN54L98	SN74L98	253	253	SN54S138	SN74S138	274	274
SN54L99	SN74L99	255	255	SN54LS139	SN74LS139	274	274
SN54100	SN74100	259	259	SN54S139	SN74S139	274	274
SN54H101	SN74H101	126	78	SN54S140	SN74S140	104	84
SN54H102	SN74H102	126	78		SN74141	278	278
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SN54107	SN74107	120	79	SN54LS145	SN74LS145	S-154	S-154
SN54LS107	SN74LS107	S-56	S-56	SN54147	SN74147	290	290
SN54H108	SN74H108	126	79	SN54148	SN74148	290	290
SN54109	SN74109	120	80	SN54150	SN74150	294	294
SN54LS109	SN74LS109	130	80	SN54151A	SN74151A	294	294
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SN54111	SN74111	120	80	SN54S151	SN74S151	294	294
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SN54LS113	SN74LS113	130	81	SN54153	SN74153	302	302
SN54S113	SN74S113	132	81	SN54L153	SN74L153	302	302
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‡Redesignated SN29000

§Redesignated SN29001

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SN54LS162	SN74LS162	S-170	S-170
SN54S162	SN74S162	S-170	S-170
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SN54LS163	SN74LS163	S-170	S-170
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SN54LS164	SN74LS164	S-186	S-186
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SN54181	SN74181	381	381
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SN54LS191	SN74LS191	417	417
SN54192	SN74192	427	427
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SN54LS192	SN74LS192	427	427
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SN54LS194A	SN74LS194A	S-215	S-215
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SN54LS195A	SN74LS195A	S-223	S-223
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SN54LS247	SN74LS247	S-233	S-233
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SN54LS249	SN74LS249	S-233	S-233
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SN54278	SN74278	488	488
SN54279	SN74279	141	85
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SN54S281	SN74S281	S-271	S-271
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SN54366	SN74366	S-84	S-84
SN54367	SN74367	S-84	S-84
SN54368	SN74368	S-84	S-84
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FUNCTIONAL INDEX/SELECTION GUIDE

The following pages contain functional indexes and selection guides designed to simplify the choice of a particular function to fit a specific application. Essential characteristics of similar or like functions are grouped for comparative analysis, and the electrical specifications are referenced by page number. The following categories of functions are covered:

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Positive-NAND gates and inverters with open-collector outputs	S-16
Positive-NOR gates with totem-pole outputs	S-17
Positive-AND gates with totem-pole outputs	S-17
Positive-AND gates with open-collector outputs	S-17
Schmitt-trigger positive-NAND gates and inverters with totem-pole outputs	S-17
Buffers/clock drivers with totem-pole outputs	S-18
50-ohm/75-ohm line drivers	S-18
Buffer and interface gates with open-collector outputs	S-19
Positive-OR gates with totem-pole outputs	S-19
AND-OR-INVERT gates with totem-pole outputs	S-19
AND-OR-INVERT gates with open-collector outputs	S-19
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Open-collector display decoders/drivers	S-29
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FUNCTIONAL INDEX/SELECTION GUIDE

POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS
ELECTRICAL TABLES—PAGE 88†

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS PAGE NO.†
			-55°C to 125°C		0°C to 70°C		
HEX INVERTERS	3 ns	19 mW	SN54S04	J, W	SN74S04	J, N	63
	6 ns	22 mW	SN54H04	J, W	SN74H04	J, N	
	9.5 ns	2 mW	SN54LS04	J, W	SN74LS04	J, N	
	10 ns	10 mW	SN5404	J, W	SN7404	J, N	
	33 ns	1 mW	SN54L04	J, N, T	SN74L04	J, N, T	
QUADRUPLE 2-INPUT POSITIVE-NAND GATES	3 ns	19 mW	SN54S00	J, N, W	SN74S00	J, N	62
	6 ns	22 mW	SN54H00	J, W	SN74H00	J, N	
	9.5 ns	2 mW	SN54LS00	J, W	SN74LS00	J, N	
	10 ns	10 mW	SN5400	J, W	SN7400	J, N	
	33 ns	1 mW	SN54L00	J, N, T	SN74L00	J, N, T	
TRIPLE 3-INPUT POSITIVE-NAND GATES	3 ns	19 mW	SN54S10	J, W	SN74S10	J, N	64
	6 ns	22 mW	SN54H10	J, W	SN74H10	J, N	
	9.5 ns	2 mW	SN54LS10	J, W	SN74LS10	J, N	
	10 ns	10 mW	SN5410	J, W	SN7410	J, N	
	33 ns	1 mW	SN54L10	J, N, T	SN74L10	J, N, T	
DUAL 4-INPUT POSITIVE-NAND GATES	3 ns	19 mW	SN54S20	J, W	SN74S20	J, N	66
	6 ns	22 mW	SN54H20	J, W	SN74H20	J, N	
	9.5 ns	2 mW	SN54LS20	J, W	SN74LS20	J, N	
	10 ns	10 mW	SN5420	J, W	SN7420	J, N	
	33 ns	1 mW	SN54L20	J, N, T	SN74L20	J, N, T	
8-INPUT POSITIVE-NAND GATES	3 ns	19 mW	SN54S30	J, W	SN74S30	J, N	68
	6 ns	22 mW	SN54H30	J, W	SN74H30	J, N	
	17 ns	2.4 mW	SN54LS30	J, W	SN74LS30	J, N	
	10 ns	10 mW	SN5430	J, W	SN7430	J, N	
	33 ns	1 mW	SN54L30	J, N, T	SN74L30	J, N, T	
13-INPUT POSITIVE-NAND GATES	3 ns	19 mW	SN54S133	J, W	SN74S133	J, N	84

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS
ELECTRICAL TABLES—PAGE 88†

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS PAGE NO.†
			-55°C to 125°C		0°C to 70°C		
HEX INVERTERS	5 ns	17.5 mW	SN54S05	J, W	SN74S05	J, N	63
	8 ns	22 mW	SN54H05	J, W	SN74H05	J, N	
	16 ns	2 mW	SN54LS05	J, W	SN74LS05	J, N	
	22 ns	10 mW	SN5405	J, W	SN7405	J, N	
QUADRUPLE 2-INPUT POSITIVE-NAND GATES	5 ns	17.5 mW	SN54S03	J, W	SN74S03	J, W	63
	8 ns	22 mW	SN54H01	J, W	SN74H01	J, N	62
	16 ns	2 mW	SN54LS01	J, W	SN74LS01	J, N	62
	16 ns	2 mW	SN54LS03	J, W	SN74LS03	J, N	63
	22 ns	10 mW	SN5401	J, W	SN7401	J, N	62
	22 ns	10 mW	SN5403	J	SN7403	J, N	63
	41 ns	1 mW	SN54L01	T	SN74L01	T	62
	41 ns	1 mW	SN54L03	J, N	SN74L03	J, N	63
TRIPLE 3-INPUT POSITIVE-NAND GATES	16 ns	2 mW	SN54LS12	J, W	SN74LS12	J, N	S-48
	22 ns	10 mW	SN5412	J, W	SN7412	J, N	65
DUAL 4-INPUT POSITIVE-NAND GATES	5 ns	17.5 mW	SN54S22	J, W	SN74S22	J, N	67
	8 ns	22 mW	SN54H22	J, W	SN74H22	J, N	
	16 ns	2 mW	SN54LS22	J, W	SN74LS22	J, N	
	22 ns	10 mW	SN5422	J, W	SN7422	J, N	

†Page numbers with "S-" preceding the number refer to pages in this supplement; those without "S-" refer to pages in *The TTL Data Book for Design Engineers* (CC-411). Electrical tables for devices in this supplement are on the same page as (or immediately following) the pin assignments.

SSI FUNCTIONS FUNCTIONAL INDEX/SELECTION GUIDE

POSITIVE-NOR GATES WITH TOTEM-POLE OUTPUTS
ELECTRICAL TABLES—PAGE 92[†]

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS PAGE NO.†
			-55°C to 125°C		0°C to 70°C		
QUADRUPLE 2-INPUT POSITIVE-NOR GATES	3.5 ns	29 mW	SN54S02	J, W	SN74S02	J, N	62
	10 ns	2.75 mW	SN54LS02	J, W	SN74LS02	J, N	
	10 ns	14 mW	SN5402	J, W	SN7402	J, N	
	33 ns	1.5 mW	SN54L02	J, N, T	SN74L02	J, N, T	
TRIPLE 3-INPUT POSITIVE-NOR GATES	8.5 ns	22 mW	SN5427	J, W	SN7427	J, N	68
	10 ns	4.5 mW	SN54LS27	J, W	SN74LS27	J, N	
DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE	10.5 ns	23 mW	SN5425	J, W	SN7425	J, N	67
DUAL 5-INPUT POSITIVE-NOR GATES	4 ns	54 mW	SN54S260	J, W	SN74S260	J, N	84

POSITIVE-AND GATES WITH TOTEM-POLE OUTPUTS
ELECTRICAL TABLES—PAGE 94[†]

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS
			-55°C to 125°C		0°C to 70°C		PAGE NO.†
QUADRUPLE 2-INPUT POSITIVE-AND GATES	4.75 ns	32 mW	SN54S08	J, W	SN74S08	J, N	S-47
	12 ns	4.25 mW	SN54LS08	J, W	SN74LS08	J, N	64
	15 ns	19 mW	SN5408	J, W	SN7408	J, N	64
TRIPLE 3-INPUT POSITIVE-AND GATES	4.75 ns	31 mW	SN54S11	J, W	SN74S11	J, N	65
	8.2 ns	40 mW	SN54H11	J, W	SN74H11	J, N	
	12 ns	4.25 mW	SN54LS11	J, W	SN74LS11	J, N	
DUAL 4-INPUT POSITIVE-AND GATES	8.2 ns	40 mW	SN54H21	J, W	SN74H21	J, N	67
	12 ns	4.25 mW	SN54LS21	J, W	SN74LS21	J, N	

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS
ELECTRICAL TABLES—PAGE 96[†]

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS
			-55°C to 125°C		0°C to 70°C		PAGE NO.†
QUADRUPLE 2-INPUT POSITIVE-AND GATES	6.5 ns	32 mW	SN54S09	J, W	SN74S09	J, N	S-47
	18.5 ns	19.4 mW	SN5409	J, W	SN7409	J, N	64
	20 ns	4.25 mW	SN54LS09	J, W	SN74LS09	J, N	64
TRIPLE 3-INPUT POSITIVE-AND GATES	6 ns	28 mW	SN54S15	J, W	SN74S15	J, N	66
	10.5 ns	38 mW	SN54H15	J, W	SN74H15	J, N	
	20 ns	4.25 mW	SN54LS15	J, W	SN74LS15	J, N	

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS
ELECTRICAL TABLES—PAGE 98[†]

DESCRIPTION	TYPICAL HYSTERESIS	TYPICAL DELAY TIME	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS PAGE NO.†
			-55°C to 125°C		0°C to 70°C		
HEX SCHMITT TRIGGER INVERTERS	0.8 V	15 ns	SN5414	J, W	SN7414	J, N	65
	0.8 V	15 ns	SN54LS14	J, W	SN74LS14	J, N	S-49
QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS	0.55 V	8 ns	SN54S132	J, W	SN74S132	J, N	83
	0.8 V	15 ns	SN54132	J, W	SN74132	J, N	83
	0.8 V	15 ns	SN54LS132	J, W	SN74LS132	J, N	S-67
DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS	0.8 V	16.5 ns	SN5413	J, W	SN7413	J, N	65
	0.8 V	16.5 ns	SN54LS13	J, W	SN74LS13	J, N	S-49

[†]Page numbers with "S-" preceding the number refer to pages in this supplement; those without "S-" refer to pages in *The TTL Data Book for Design Engineers* (CC-411). Electrical tables for devices in this supplement are on the same page as (or immediately following) the pin assignments.

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BUFFERS/CLOCK DRIVERS WITH TOTEM-POLE OUTPUTS
(ALSO SEE CLOCK GENERATOR CIRCUITS)
ELECTRICAL TABLES—PAGE 102†

DESCRIPTION	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYP POWER PER GATE	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS PAGE NO. [†]
					-55°C to 125°C		0°C to 70°C		
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS	48 mA	-2.4 mA	7 ns	28 mW	SN5428	J, W	SN7428	J, N	68
	24 mA	-1.2 mA	12 ns	5.5 mW			SN74LS28	J, N	
	12 mA	-1.2 mA	12 ns	5.5 mW	SN54LS28	J, W			
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS	60 mA	-3 mA	4 ns	41 mW	SN54S37	J, W	SN74S37	J, N	S-55
	48 mA	-1.2 mA	10.5 ns	27 mW	SN5437	J, W	SN7437	J, N	69
	24 mA	-1.2 mA	12 ns	4.3 mW			SN74LS37	J, N	69
	12 mA	-1.2 mA	12 ns	4.3 mW	SN54LS37	J, W			69
DUAL 4-INPUT POSITIVE-NAND BUFFERS	60 mA	-3 mA	4 ns	44 mW	SN54S40	J, W	SN74S40	J, N	70
	60 mA	-1.5 mA	7.5 ns	44 mW	SN54H40	J, W	SN74H40	J, N	
	48 mA	-1.2 mA	10.5 ns	26 mW	SN5440	J, W	SN7440	J, N	
	24 mA	-1.2 mA	12 ns	4.3 mW			SN74LS40	J, N	
	12 mA	-1.2 mA	12 ns	4.3 mW	SN54LS40	J, W			

50-OHM/75-OHM LINE DRIVERS
ELECTRICAL TABLES—PAGE 104†

DESCRIPTION	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYP POWER PER GATE	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS PAGE NO.†
					-55°C to 125°C		0°C to 70°C		
DUAL 4-INPUT POSITIVE-NAND LINE DRIVERS	60 mA	-40 mA	4 ns	44 mW	SN54S140	J, W	SN74S140	J, N	84
QUADRUPLE 2-INPUT POSITIVE-NOR LINE DRIVERS	48 mA	-42.4 mA	7 ns	28 mW	SN54128	J, W	SN74128	J, N	83
	48 mA	-29 mA	7 ns	28 mW					

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS
ELECTRICAL TABLES—PAGE 106†

DESCRIPTION	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYP POWER PER GATE	DEVICE TYPE AND PACKAGE			PIN ASSIGNMENTS PAGE NO.†	
					-55°C to 125°C		0°C to 70°C		
HEX BUFFERS/DRIVERS	30 V	40 mA	13 ns	21 mW			SN7407	J, N	64
	30 V	30 mA	13 ns	21 mW	SN5407	J, W			64
	15 V	40 mA	13 ns	21 mW			SN7417	J, N	66
	15 V	30 mA	13 ns	21 mW	SN5417	J, W			66
HEX INVERTER BUFFERS/DRIVERS	30 V	40 mA	12.5 ns	26 mW			SN7406	J, N	63
	30 V	30 mA	12.5 ns	26 mW	SN5406	J, W			63
	15 V	40 mA	12.5 ns	26 mW			SN7416	J, N	66
	15 V	30 mA	12.5 ns	26 mW	SN5416	J, W			66
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS	15 V	16 mA	13.5 ns	10 mW	SN5426	J	SN7426	J, N	68
	15 V	8 mA	16 ns	2 mW			SN74LS26	J, N	S-53
	15 V	4 mA	16 ns	2 mW	SN54LS26	J, W			S-53
	5.5 V	60 mA	6.5 ns	41 mW	SN54S38	J, W	SN74S38	J, N	S-55
	5.5 V	48 mA	12.5 ns	24.4 mW	SN5438	J, W	SN7438	J, N	69
	5.5 V	24 mA	19 ns	4.3 mW			SN74LS38	J, N	69
	5.5 V	12 mA	19 ns	4.3 mW	SN54LS38	J, W			69
QUADRUPLE 2-INPUT POSITIVE- NOR BUFFERS	5.5 V	48 mA	11 ns	28 mW	SN5433	J, W	SN7433	J, N	69
	5.5 V	24 mA	19 ns	5.45 mW			SN74LS33	J, N	69
	5.5 V	12 mA	19 ns	5.45 mW	SN54LS33	J, W			69

†Page numbers with "S-" preceding the number refer to pages in this supplement; those without "S-" refer to pages in *The TTL Data Book for Design Engineers* (CC-411). Electrical tables for devices in this supplement are on the same page as (or immediately following) the pin assignments.

SSI FUNCTIONS FUNCTIONAL INDEX/SELECTION GUIDE

POSITIVE-OR GATES WITH TOTEM-POLE OUTPUTS
ELECTRICAL TABLES—PAGE 108†

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS PAGE NO.†
			–55°C to 125°C		0°C to 70°C		
			4 ns	35 mW	SN54S32	J, W	SN74S32
QUADRUPLE 2-INPUT POSITIVE-OR GATES	12 ns	24 mW	SN5432	J, W	SN7432	J, N	69
	12 ns	5 mW	SN54LS32	J, W	SN74LS32	J, N	69

AND-OR-INVERT GATES WITH TOTEM-POLE OUTPUTS
ELECTRICAL TABLES—PAGE 110†

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS PAGE NO.†
			–55°C to 125°C		0°C to 70°C		
2-WIDE 4-INPUT	12.5 ns	2.75 mW	SN54LS55	J, W	SN74LS55	J, N	73
	43 ns	1.5 mW	SN54L55	J, N, T	SN74L55	J, N, T	
4-WIDE 4-2-3-2-INPUT	3.5 ns	29 mW	SN54S64	J, W	SN74S64	J, N	74
4-WIDE 2-2-3-2-INPUT	6.6 ns	41 mW	SN54H54	J, W	SN74H54	J, N	72
4-WIDE 2-1-INPUT	10.5 ns	23 mW	SN5454	J, W	SN7454	J, N	72
4-WIDE 2-3-3-2-INPUT	12.5 ns	4.5 mW	SN54LS54	J, W	SN74LS54	J, N	72
4-WIDE 2-3-3-2-INPUT	43 ns	1.5 mW	SN54L54	J, N, T	SN74L54	J, N, T	72
DUAL 2-WIDE 2-INPUT	3.5 ns	28 mW	SN54S51	J, W	SN74S51	J, N	70
	6.5 ns	29 mW	SN54H51	J, W	SN74H51	J, N	
	10.5 ns	14 mW	SN5451	J, W	SN7451	J, N	
	12.5 ns	2.75 mW	SN54LS51	J, W	SN74LS51	J, N	
	43 ns	1.5 mW	SN54L51	J, N, T	SN74L51	J, N, T	

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS
ELECTRICAL TABLES—PAGE 112†

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS
			–55°C to 125°C		0°C to 70°C		PAGE NO.†
4-WIDE 4-2-3-2-INPUT	5.5 ns	36 mW	SN54S65	J, W	SN74S65	J, N	74

EXPANDABLE GATES
ELECTRICAL TABLES—PAGE 113†

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	DEVICE TYPE AND PACKAGE			PIN ASSIGNMENTS	
			–55°C to 125°C	0°C to 70°C		PAGE NO.†	
DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE	10.5 ns	23 mW	SN5423	J, W	SN7423	J, N	67
4-WIDE AND-OR GATES	9.9 ns	88 mW	SN54H52	J, W	SN74H52	J, N	71
4-WIDE AND-OR-INVERT GATES	6.6 ns	41 mW	SN54H53	J, W	SN74H53	J, N	71
	10.5 ns	23 mW	SN5453	J, W	SN7453	J, N	
2-WIDE AND-OR-INVERT GATES	6.8 ns	30 mW	SN54H55	J, W	SN74H55	J, N	73
DUAL 2-WIDE AND-OR-INVERT GATES	6.5 ns	29 mW	SN54H50	J, W	SN74H50	J, N	70
	10.5 ns	14 mW	SN5450	J, W	SN7450	J, N	

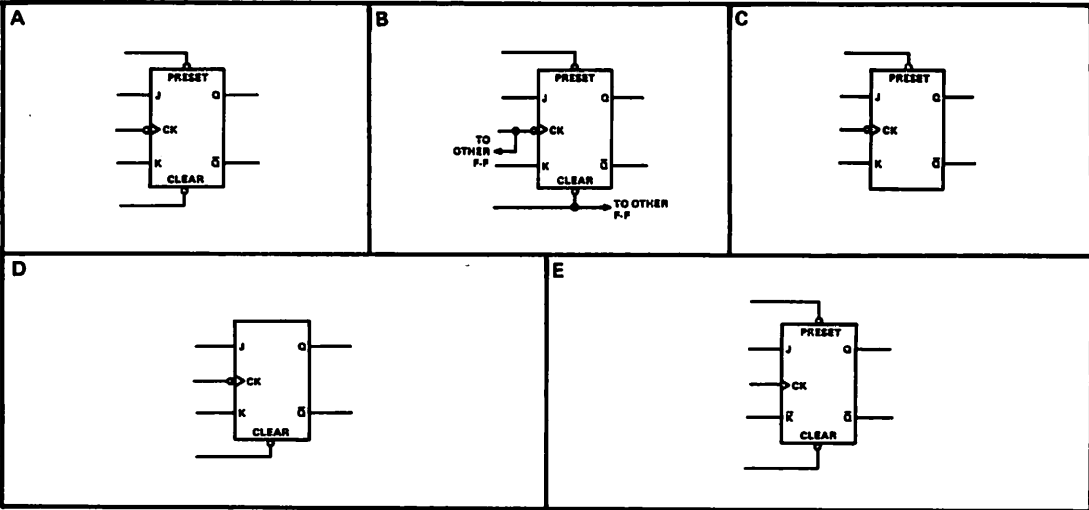
EXPANDERS
ELECTRICAL TABLES—PAGE 117†

DESCRIPTION	TYP POWER DISSIPATION PER GATE	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS PAGE NO.†
		–55°C to 125°C		0°C to 70°C		
DUAL 4-INPUT EXPANDERS	4 mW	SN5460	J, W	SN7460	J, N	73
	6 mW	SN54H60	J, W	SN74H60	J, N	
TRIPLE 3-INPUT EXPANDERS	13 mW	SN54H61	J, W	SN74H61	J, N	73
3-2-2-3-INPUT AND-OR EXPANDERS	25 mW	SN54H62	J, W	SN74H62	J, N	74

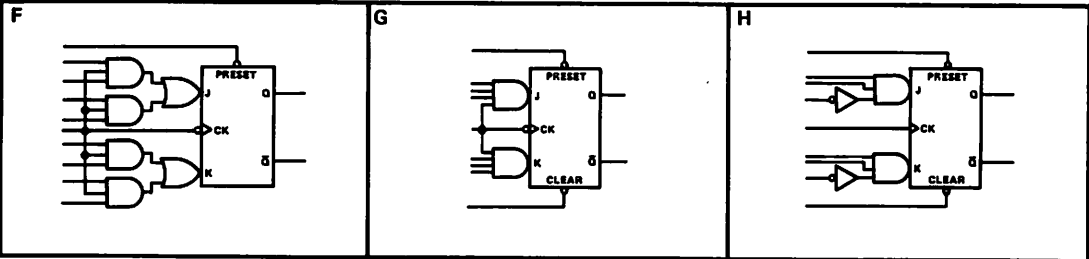
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SSI FUNCTIONS
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DUAL J-K EDGE-TRIGGERED FLIP-FLOPS



SINGLE J-K EDGE-TRIGGERED FLIP-FLOPS

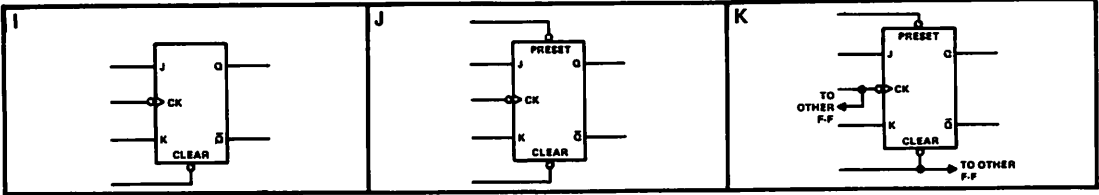


DWG REF.	TYPICAL CHARACTERISTICS		DATA TIMES		DEVICE TYPE AND PACKAGE				PAGE REFERENCES†	
	f _{max} (MHz)	P _{wr} /F-F (mW)	SETUP (ns)	HOLD (ns)	-55°C to 125°C		0°C to 70°C		PIN ASSIGNMENTS	ELECTRICAL
A	125	75	6↓	0↓	SN54S112	J, W	SN74S112	J, N	81	132
	50	100	13↓	0↓	SN54H106	J, W	SN74H106	J, N	79	126
	45	10	20↓	0↓	SN54LS76	J, W	SN74S76	J, N	77	130
	45	10 ✓	20↓	0↓	SN54LS112	J, W	SN74LS112 ✓	J, N	81	130
B	125	75	6↓	0↓	SN54S114	J, W	SN74S114	J, N	81	132
	50	100	13↓	0↓	SN54H108	J, W	SN74H108	J, N	79	126
	45	10	20↓	0↓	SN54LS78	J, W	SN74LS78	J, N	77	130
	45	10	20↓	0↓	SN54LS114	J, W	SN74LS114	J, N	81	130
C	125	75	6↓	0↓	SN54S113	J, W	SN74S113	J, N	81	132
	45	10	20↓	0↓	SN54LS113	J, W	SN74LS113	J, N	81	130
D	50	100	13↓	0↓	SN54H103	J, W	SN74H103	J, N	78	126
	45	10	20↓	0↓	SN54LS73	J, W	SN74LS73	J, N	76	130
	45	10	20↓	0↓	SN54LS107	J	SN74LS107	J, N	S-56	S-57
E	33	10	20↓	5↓	SN54LS109	J, W	SN74LS109	J, N	80	130
	33	45	10↓	6↓	SN54109	J, W	SN74109	J, N	80	120
F	50	100	13↓	0↓	SN54H101	J, W	SN74H101	J, N	78	126
G	50	100	13↓	0↓	SN54H102	J, W	SN74H102	J, N	78	126
H	35	65	20↓	5↓	SN5470	J, W	SN7470	J, N	75	120

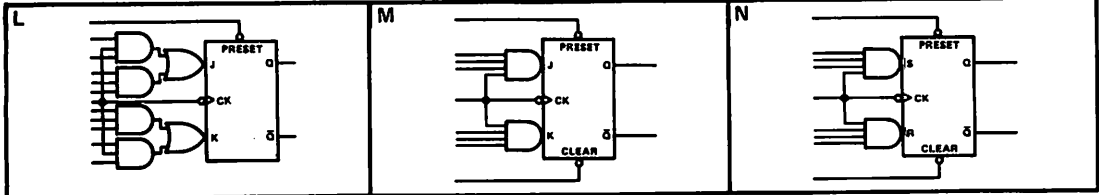
†↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.
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PULSE-TRIGGERED DUAL FLIP-FLOPS

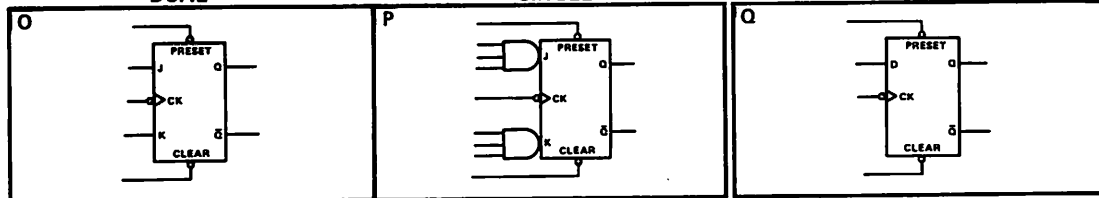


PULSE-TRIGGERED SINGLE FLIP-FLOPS



DWG. REF.	TYPICAL CHARACTERISTICS		DATA TIMES		DEVICE TYPE AND PACKAGE				PAGE REFERENCES [†]	
									PIN ASSIGNMENTS	ELECTRICAL
	f_{max} (MHz)	Pwr/F-F (mW)	SETUP (ns)	HOLD (ns)	-55°C to 125°C					
I	30	80	01	01	SN54H73	J, W	SN74H73	J, N	76	124
	20	50	01	01	SN5473	J, W	SN7473	J, N	76	120
	20	50	01	01	SN54107	J	SN74107	J, N	79	120
	3	3.8	01	01	SN54L73	J, N, T	SN74L73	J, N, T	76	128
J	30	80	01	01	SN54H76	J, W	SN74H76	J, N	77	124
	20	50	01	01	SN5476	J, W	SN7476	J, N	77	120
K	30	80	01	01	SN54H78	J, W	SN74H78	J, N	77	124
	3	3.8	01	01	SN54L78	J, N, T	SN74L78	J, N, T	77	128
L	30	80	01	01	SN54H71	J, W	SN74H71	J, N	75	124
M	30	80	01	01	SN54H72	J, W	SN74H72	J, N	76	124
	20	50	01	01	SN5472	J, W	SN7472	J, N	76	120
	3	3.8	01	01	SN54L72	J, N, T	SN74L72	J, N, T	76	128
N	3	3.8	01	01	SN54L71	J, N, T	SN74L71	J, N, T	75	128

J-K FLIP-FLOPS WITH DATA LOCKOUT



DWG. REF.	TYPICAL CHARACTERISTICS		DATA TIMES		DEVICE TYPE AND PACKAGE				PAGE REFERENCES [†]	
									PIN ASSIGNMENTS	ELECTRICAL
	f_{max} (MHz)	Pwr/F-F (mW)	SETUP (ns)	HOLD (ns)	-55°C to 125°C					
O	25	70	01	301	SN54111	J, W	SN74111	J, N	80	120
P	25	100	201	51	SN54110	J, W	SN74110	J, N	80	120
Q	110	75	31	21	SN54S74	J, W	SN74S74	J, N	76	132
	43	75	151	51	SN54H74	J, W	SN74H74	J, N	76	124
	33	10	251	51	SN54LS74	J, W	SN74LS74	J, N	76	130
	25	43	201	51	SN5474	J, W	SN7474	J, N	76	120
	3	4	501	151	SN54L74	J, N, T	SN74L74	J, N, T	76	128

† The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

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SSI FUNCTIONS

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MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS
ELECTRICAL TABLES—PAGE 134†

DESCRIPTION	NO. OF INPUTS		OUTPUT PULSE RANGE	TYP TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS PAGE NO. [†]
	POSITIVE	NEGATIVE			-55°C to 125°C		0°C to 70°C		
SINGLE	1	2	40 ns–28 s	90 mW	SN54121	J, W	SN74121	J, N	82
	1	2	40 ns–28 s	40 mW	SN54L121	J,N,T	SN74L121	J,N,T	
DUAL	1	1	20 ns–70 s	23 mW	SN54LS221	J, W	SN74LS221	J, N	S-69
	1	1	20 ns–49 s	23 mW					
	1	1	20 ns–28 s	130 mW	SN54221	J, W	SN74221	J, N	
	1	1	20 ns–21 s	130 mW					

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS
ELECTRICAL TABLES—PAGE 138†

ELECTRONIC TABLES—PAGE 130										
DESCRIPTION	NO. OF INPUTS		DIRECT CLEAR	OUTPUT PULSE RANGE	TYP TOTAL POWER	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS
	POSITIVE	NEGATIVE				-55°C to 125°C		0°C to 70°C		
SINGLE	2	2	Yes	45 ns—∞	115 mW	SN54122	J, W	SN74122	J, N	82
	2	2	Yes	90 ns—∞	55 mW	SN54L122	J,N,T	SN74L122	J,N,T	82
	2	2	Yes	45 ns—∞	30 mW	SN54LS122	J, W	SN74LS122	J, N	S-58
DUAL	1	1	Yes	45 ns—∞	230 mW	SN54123	J, W	SN74123	J, N	82
	1	1	Yes	90 ns—∞	115 mW	SN54L123	J	SN74L123	J, N	82
	1	1	Yes	45 ns—∞	60 mW	SN54LS123	J, W	SN74LS123	J, N	S-58

SR LATCHES
ELECTRICAL TABLES—PAGE 141†

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PIN ASSIGNMENTS PAGE NO. [†]
			-55°C to 125°C		0°C to 70°C		
QUADRUPLE $\overline{S}\overline{R}$ LATCHES	12 ns	19 mW	SN54LS279	J, W	SN74LS279	J, N	S-82
	12 ns	90 mW	SN54279	J, W	SN74279	J, N	85

BUS INTERFACE GATES WITH 3-STATE TOTEM-POLE OUTPUTS
ELECTRICAL TABLES—PAGE 142†

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	DEVICE TYPE AND PACKAGES				PIN ASSIGNMENTS PAGE NO.†
			-55°C to 125°C		0°C to 70°C		
			HEX BUS DRIVERS	12 ns	54 mW	SN54365 SN54367	J, W J, W
HEX INVERTER BUS DRIVERS	11 ns	49 mW	SN54366 SN54368	J, W J, W	SN74366 SN74368	J, N J, N	S-84
QUADRUPLE BUS BUFFERS	10 ns 10 ns	40 mW 45 mW	SN54125 SN54126	J, W J, W	SN74125 SN74126	J, N J, N	83
12-INPUT POSITIVE-NAND GATES	4.5 ns	45 mW	SN54S134	J, W	SN74S134	J, N	84

CLOCK GENERATOR CIRCUITS

DESCRIPTION	TYP TOTAL POWER	DEVICE TYPE AND PACKAGE				PAGE NO.†
	DISSIPATION	-55°C to 125°C		0°C to 70°C		
QUADRUPLE COMPLEMENTARY-OUTPUT LOGIC ELEMENTS	125 mW	SN54265	J, W	SN74265	J, N	S-77
DUAL VOLTAGE-CONTROLLED OSCILLATORS	90 mW	SN54LS124	J, W	SN74LS124	J, N	S-62
	525 mW	SN54S124	J, W	SN74S124	J, N	

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MSI/LSI FUNCTIONS

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ADDERS

DESCRIPTION	TYPICAL CARRY TIME	TYPICAL ADD TIME	TYP POWER DISSIPATION PER BIT	DEVICE TYPE AND PACKAGE				PAGE NO.†
				-55°C to 125°C		0°C to 70°C		
SINGLE 1-BIT GATED FULL ADDERS	10.5 ns	52 ns	105 mW	SN5480	J, W	SN7480	J, N	187
SINGLE 2-BIT FULL ADDERS	14.5 ns	25 ns	87 mW	SN5482	J, W	SN7482	J, N	195
SINGLE 4-BIT FULL ADDERS	10 ns	15 ns	24 mW	SN54LS83A	J, W	SN74LS83A	J, N	S-115
	10 ns	15 ns	24 mW	SN54LS283	J, W	SN74LS283	J, N	S-276
	10 ns	16 ns	76 mW	SN5483A	J, W	SN7483A	J, N	S-115
	10 ns	16 ns	76 mW	SN54283	J, W	SN74283	J, N	S-276
DUAL 1-BIT CARRY-SAVE FULL ADDERS	11 ns	11 ns	110 mW	SN54H183	J, W	SN74H183	J, N	396

ACCUMULATORS, ARITHMETIC LOGIC UNITS, LOOK-AHEAD CARRY GENERATORS

DESCRIPTION	TYPICAL CARRY TIME	TYPICAL ADD TIME	TYP TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PAGE NO.†
				-55° C to 125° C		0° C to 70° C		
4-BIT PARALLEL BINARY ACCUMULATORS	10 ns	20 ns	720 mW	SN54S281	J, W	SN74S281	J, N	S-271
4-BIT ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS	11 ns	20 ns	525 mW			SN74S381	N	S-312
	7 ns	11 ns	600 mW	SN54S181	J, W	SN74S181	J, N	381
	12.5 ns	24 ns	455 mW	SN54181	J, W	SN74181	J, N	381
	16 ns	24 ns	102 mW	SN54LS181	J, W	SN74LS181	J, N	381
LOOK-AHEAD CARRY GENERATORS	7 ns		260 mW	SN54S182	J, W	SN74S182	J, N	392
	13 ns		180 mW	SN54182	J, W	SN74182	J, N	

MULTIPLIERS

DESCRIPTION	DEVICE TYPE AND PACKAGE				PAGE NO.†
	-55° C to 125° C		0° C to 70° C		
2-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS	SN54LS261	J, W	SN74LS261	J, N	S-248
4-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS	SN54284, SN54285	J, W	SN74284, SN74285	J, N	496
			SN74S274	N	S-262
7-BIT-SLICE WALLACE TREE	SN54S275	J	SN74S275	J, N	S-262
25-MHz 6-BIT-BINARY RATE MULTIPLIERS	SN5497	J, W	SN7497	J, N	248
25-MHz DECADE RATE MULTIPLIERS	SN54167	J, W	SN74167	J, N	347

COMPARATORS

DESCRIPTION	TYPICAL COMPARE TIME	TYP TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PAGE NO.†
			-55° C to 125° C		0° C to 70° C		
4-BIT MAGNITUDE COMPARATORS	11.5 ns	365 mW	SN54S85	J, W	SN74S85	J, N	S-119
	21 ns	275 mW	SN5485	J, W	SN7485	J, N	
	23.5 ns	52 mW	SN54LS85	J, W	SN74LS85	J, N	
	82 ns	20 mW	SN54L85	J	SN74L85	J, N	

PARITY GENERATORS/CHECKERS

DESCRIPTION	TYPICAL DELAY TIME	TYP TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PAGE NO.†
			-55°C to 125°C		0°C to 70°C		
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS	13 ns	335 mW	SN54S280	J, W	SN74S280	J, N	491
8-BIT ODD/EVEN PARITY GENERATORS/CHECKERS	35 ns	170 mW	SN54180	J, W	SN74180	J, N	379

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MSI/LSI FUNCTIONS
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OTHER ARITHMETIC OPERATORS

DESCRIPTION	TYPICAL DELAY TIME	TYP TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PAGE NO.†
			−55°C to 125°C		0°C to 70°C		
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH TOTEM-POLE OUTPUTS	7 ns	250 mW	SN54S86	J, W	SN74S86	J, N	209
	10 ns	30 mW	SN54LS86	J, W	SN74LS86	J, N	209
	10 ns	30 mW	SN54LS386	J, W	SN74LS386	J, N	S-315
	14 ns	150 mW	SN5486	J, W	SN7486	J, N	209
	55 ns	15 mW	SN54L86	J,N,T	SN74L86	J,N,T	209
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS	18 ns	30 mW	SN54LS136	J, W	SN74LS136	J, N	271
	27 ns	150 mW	SN54136	J, W	SN74136	J, N	
QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES	18 ns	40 mW	SN54LS266	J, W	SN74LS266	J, N	486
QUADRUPLE EXCLUSIVE OR/NOR GATES	8 ns	325 mW	SN54S135	J, W	SN74S135	J, N	269
4-BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENT	14 ns	270 mW	SN54H87	J, W	SN74H87	J, N	214

SHIFT REGISTERS

DESCRIPTION	NO OF BITS	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	MODES				TYP TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PAGE NO.†		
					SH	+R	SH	+L		LOAD	HOLD	-55°C to 125°C			0°C to 70°C	
PARALLEL-IN PARALLEL-OUT (BIDIRECTIONAL)	8	50 MHz	D	Low	X	X	X	X	750 mW			SN74S299	N	S-301		
		25 MHz	D	Low	X	X	X	X	360 mW	SN54198	J, W	SN74198	J, N	456		
	4	70 MHz	D	Low	X	X	X	X	450 mW	SN54S194	J, W	SN74S194	J, N	S-215		
		25 MHz	D	Low	X	X	X	X	75 mW	SN54LS194A	J, W	SN74LS194A	J, N			
PARALLEL-IN, PARALLEL-OUT	8	25 MHz	J-K	Low	X		X	X	360 mW	SN54199	J, W	SN74199	J, N	456		
		10 MHz	D	Low	X		X		60 mW	SN54LS96	J, W	SN74LS96	J, N	S-147		
	5	10 MHz	D	Low	X		X		240 mW	SN5496	J, W	SN7496	J, N			
		5 MHz	D	Low	X		X		120 mW	SN54L96	J	SN74L96	J, N			
	4	70 MHz	J-K	Low	X		X		375 mW	SN54S195	J, W	SN74S195	J, N	S-223		
		30 MHz	J-K	Low	X		X		195 mW	SN54195	J, W	SN74195	J, N	S-223		
		25 MHz	D	Low	X		X		75 mW	SN54LS395	J, W	SN74LS395	J, N	S-325		
		25 MHz	D	None	X		X		195 mW	SN5495A	J, W	SN7495A	J, N	S-141		
		25 MHz	D	Low	X		X	X	230 mW	SN54179	J, W	SN74179	J, N	375		
		25 MHz	D	None	X		X	X	230 mW	SN54178	J, W	SN74178	J, N	375		
		30 MHz	J-K	Low	X		X		70 mW	SN54LS195A	J, W	SN74LS195A	J, N	S-223		
		25 MHz	D	None	X		X		65 mW	SN54LS95B	J, W	SN74LS95B	J, N	S-141		
		25 MHz	D	None	X		X		70 mW	SN54LS295A	J, W	SN74LS295A	J, N	S-293		
		3 MHz	J-K	None	X		X		19 mW	SN54L99	J	SN74L99	J, N	255		
		3 MHz	D	None	X		X		19 mW	SN54L95	J,N,T	SN74L95	J,N,T	S-141		
SERIAL-IN, PARALLEL-OUT	8	25 MHz	Gated D	Low	X				80 mW	SN54LS164	J, W	SN74LS164	J, N	S-186		
		25 MHz	Gated D	Low	X				167 mW	SN54164	J, W	SN74164	J, N			
		12 MHz	Gated D	Low	X				84 mW	SN54L164	J,N,T	SN74L164	J,N,T			
PARALLEL-IN, SERIAL-OUT	8	25 MHz	D	None	X		X	X	210 mW	SN54165	J, W	SN74165	J, N	339		
		20 MHz	D	Low	X		X	X	360 mW	SN54166	J, W	SN74166	J, N	343		
SERIAL-IN, SERIAL-OUT	8	10 MHz	D	High	X		X		175 mW	SN5494	J, W	SN7494	J, N	234		
		10 MHz	Gated D	None	X				60 mW	SN54LS91	J, W	SN74LS91	J, N	S-136		
		10 MHz	Gated D	None	X				175 mW	SN5491A	J, W	SN7491A	J, N			
		3 MHz	Gated D	None	X				17.5 mW	SN54L91	J,N,T	SN74L91	J,N,T			

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‡S-R = shift right, S-L = shift left

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REGISTER FILES

DESCRIPTION	TYPICAL ADDRESS	TYP READ ENABLE	DATA INPUT	TYP TOTAL POWER	DEVICE TYPE AND PACKAGE				PAGE NO.†
	TIME	TIME	RATE	DISSIPATION	-55°C to 125°C		0°C to 70°C		
EIGHT WORDS OF TWO BITS	33 ns	15 ns	20 MHz	560 mW			SN74172	J, N	356
FOUR WORDS OF FOUR BITS	27 ns	15 ns	20 MHz	125 mW	SN54LS170	J, W	SN74LS170	J, N	S-203
	30 ns	15 ns	20 MHz	635 mW	SN54170	J, W	SN74170	J, N	
FOUR WORDS OF FOUR BITS (3-STATE OUTPUTS)	24 ns	19 ns	20 MHz	135 mW	SN54LS670	J, W	SN74LS670	J, N	S-332

OTHER REGISTERS

DESCRIPTION	FREQ	ASYNC CLEAR	TYP TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PAGE NO.†
				-55°C to 125°C		0°C to 70°C		
OCTAL D-TYPE REGISTERS						SN74S273	N	S-260
HEX D-TYPE REGISTERS	75 MHz	Low	450 mW	SN54S174	J, W	SN74S174	J, N	363
	30 MHz	Low	80 mW	SN54LS174	J, W	SN74LS174	J, N	363
	25 MHz	Low	225 mW	SN54174	J, W	SN74174	J, N	363
QUADRUPLE D-TYPE REGISTERS	75 MHz	Low	300 mW	SN54S175	J, W	SN74S175	J, N	363
	30 MHz	Low	55 mW	SN54LS175	J, W	SN74LS175	J, N	363
	25 MHz	Low	150 mW	SN54175	J, W	SN74175	J, N	363
QUADRUPLE MULTIPLEXERS WITH STORAGE	25 MHz	None	65 mW	SN54LS298	J, W	SN74LS298	J, N	S-296
	25 MHz	None	195 mW	SN54298	J, W	SN74298	J, N	S-296
	3 MHz	None	25 mW	SN54L98	J	SN74L98	J, N	253
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS	50 MHz	Low	750 mW			SN74S299	N	S-301
QUADRUPLE BUS-BUFFER REGISTERS	25 MHz	High	250 mW	SN54173	J, W	SN74173	J, N	360

LATCHES

DESCRIPTION	NO. OF BITS	CLEAR	OUTPUTS	TYPICAL DELAY TIME	TYP TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PAGE NO.†
						-55°C to 125°C		0°C to 70°C		
DG (CLOCKED) LATCHES	8	Low	Q	11 ns	250 mW	SN54116	J, W	SN74116	J, N	261
		None	Q	15 ns	320 mW	SN54100	J, W	SN74100	J, N	259
	4	None	Q, \bar{Q}	11 ns	32 mW	SN54LS75	J, W	SN74LS75	J, N	S-109
		None	Q	10 ns	35 mW	SN54LS77	W			
		None	Q, \bar{Q}	15 ns	160 mW	SN5475	J, W	SN7475	J, N	
		None	Q	15 ns	160 mW	SN5477	W			
		None	Q, \bar{Q}	30 ns	80 mW	SN54L75	J	SN74L75	J, N	
		None	Q	30 ns	80 mW	SN54L77	T	SN74L77	T	
\bar{S} - \bar{R} Latches (SSI)	4	None	Q	12 ns	19 mW	SN54LS279	J, W	SN74LS279	J, N	S-82
		None	Q	12 ns	90 mW	SN54279	J, W	SN74279	J, N	85

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READ-ONLY MEMORIES (ROM's, PROM's)

DESCRIPTION	ORGANI- ZATION	TYPE OF OUTPUT	TYPICAL ADDRESS TIME	TYPICAL ENABLE TIME	TYP POWER DISSIPATION PER BIT	DEVICE TYPE AND PACKAGE				PAGE NO.†
						-55°C to 125°C		0°C to 70°C		
2048-BIT ROM	512 X 4	O-C	45 ns	15 ns	0.26 mW	SN54S270	J	SN74S270	J, N	S-254
	256 X 8	O-C	45 ns	15 ns	0.26 mW			SN74S271	N	S-254
	512 X 4	3-State	45 ns	15 ns	0.26 mW	SN54S370	J	SN74S370	J, N	S-308
	256 X 8	3-State	45 ns	15 ns	0.26 mW			SN74S371	N	S-308
1024-BIT PROM	256 X 4	3-State	40 ns	15 ns	0.49 mW			SN74S287	J, N	S-279
	256 X 4	O-C	40 ns	15 ns	0.49 mW			SN74S387	J, N	S-317
1024-BIT ROM	256 X 4	O-C	40 ns	20 ns	0.46 mW	SN54187	J, W	SN74187	J, N	410
512-BIT PROM	64 X 8	O-C	50 ns	47 ns	0.6 mW	SN54186	J, W	SN74186	J, N	404
256-BIT PROM	32 X 8	O-C	29 ns	28 ns	1.3 mW			SN74188A	J, N	414
256-BIT ROM	32 X 8	O-C	26 ns	22 ns	1.1 mW	SN5488A	J, W	SN7488A	J, N	216

RANDOM ACCESS READ-WRITE MEMORIES (RAM's)

DESCRIPTION	ORGANI- ZATION	TYPE OF OUTPUT	TYPICAL ADDRESS TIME	TYPICAL ENABLE TIME	TYP POWER DISSIPATION PER BIT	DEVICE TYPE AND PACKAGE				PAGE NO.†
						-55°C to 125°C		0°C to 70°C		
256-BIT READ/WRITE MEMORY	256 X 1	3-State	30 ns	9 ns	1.7 mW	SN54S200	J, W	SN74S200	J, N	466
	256 X 1	3-State	42 ns	17 ns	1.8 mW			SN74200	J, N	463
	256 X 1	O-C	32 ns	17 ns	1.7 mW	SN54S206	J, W	SN74S206	J, N	470
	256 X 1	3-State	42 ns	17 ns	1.9 mW			SN74S201	J, N	S-230
64-BIT READ WRITE MEMORY	16 X 4	3-State	25 ns	12 ns	5.9 mW	SN54S189	J, W	SN74S189	J, N	S-211
	16 X 4	O-C	25 ns	12 ns	5.9 mW	SN54S289	J, W	SN74S289	J, N	S-283
	16 X 4	O-C	32 ns	30 ns	5.9 mW			SN7489	J, N	220
16-BIT READ/WRITE MEMORY	16 X 1	O-C	15 ns	15 ns	14 mW	SN5481A	J, W	SN7481A	J, N	190
	16 X 1	O-C	15 ns	15 ns	14 mW	SN5484A	J, W	SN7484A	J, N	190
16-BIT MULTIPLE-PORT REGISTER FILE	8 X 2	3-State	33 ns	15 ns	35 mW			SN74172	J, N	356
16-BIT REGISTER FILE	4 X 4	O-C	27 ns	15 ns	7.8 mW	SN54LS170	J, W	SN74LS170	J, N	S-203
	4 X 4	O-C	30 ns	15 ns	40 mW	SN54170	J, W	SN74170	J, N	S-203
	4 X 4	3-State	24 ns	19 ns	9.3 mW	SN54LS670	J, W	SN74LS870	J, N	S-332

CODE CONVERTERS

DESCRIPTION	TYPICAL DELAY TIME PER PACKAGE LEVEL	TYPICAL TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PAGE NO.†
			-55°C to 125°C		0°C to 70°C		
6-LINE-BCD TO 6-LINE BINARY, OR 4-LINE TO 4-LINE BCD 9's/BCD 10's CONVERTERS	25 ns	280 mW	SN54184	J, W	SN74184	J, N	398
6-BIT-BINARY TO 6-BIT-BCD CONVERTERS	25 ns	280 mW	SN54185A	J, W	SN74185A	J, N	398

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PRIORITY ENCODERS/REGISTERS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PAGE NO.†
			-55°C to 125°C		0°C to 70°C		
FULL BCD PRIORITY ENCODERS	10 ns	225 mW	SN54147	J, W	SN74147	J, N	290
CASCADABLE OCTAL PRIORITY ENCODERS	12 ns	190 mW	SN54148	J, W	SN74148	J, N	290
4-BIT CASCADABLE PRIORITY REGISTERS	35 ns	275 mW	SN54278	J, W	SN74278	J, N	488

PULSE SYNCHRONIZERS

DESCRIPTION	TYPICAL DELAY TIME	TYP TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PAGE NO.†
			-55°C to 125°C		0°C to 70°C		
DUAL 30-MHz PULSE SYNCHRONIZERS/DRIVERS	16 ns	255 mW	SN54120	J, W	SN74120	J, N	264

DATA SELECTORS/MULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPICAL DELAY TIMES			TYP TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PAGE NO.†
		DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE		-55°C to 125°C		0°C to 70°C		
16-LINE-TO-1-LINE	2-State	11 ns		18 ns	200 mW	SN54150	J, W	SN74150	J, N	294
DUAL 8-LINE-TO-1-LINE	3-State	10 ns		17 ns	220 mW			SN74351	N	S-305
8-LINE-TO-1-LINE	3-State	4.5 ns	8 ns	14 ns	275 mW	SN54S251	J, W	SN74S251	J, N	473
	3-State	17 ns	21 ns	21 ns	250 mW	SN54251	J, W	SN74251	J, N	473
	3-State	17 ns	21 ns	21 ns	35 mW	SN54LS251	J, W	SN74LS251	J, N	473
	2-State	4.5 ns	8 ns	9 ns	225 mW	SN54S151	J, W	SN74S151	J, N	294
	2-State	8 ns	16 ns	22 ns	145 mW	SN54151A	J, W	SN74151A	J, N	294
	2-State	8 ns			130 mW	SN54152A	W			294
	2-State	11 ns	18 ns	27 ns	30 mW	SN54LS151	J, W	SN74LS151	J, N	294
	2-State	11 ns		18 ns	28 mW	SN54LS152	W			294
DUAL 4-LINE-TO-1-LINE	3-State		12 ns	16 ns	35 mW	SN54LS253	J, W	SN74LS253	J, N	480
	2-State		6 ns	9.5 ns	225 mW	SN54S153	J, W	SN74S153	J, N	302
	2-State		14 ns	17 ns	180 mW	SN54153	J, W	SN74153	J, N	302
	2-State		14 ns	17 ns	31 mW	SN54LS153	J, W	SN74LS153	J, N	302
	2-State		27 ns	34 ns	90 mW	SN54L153	J	SN74L153	J, N	302
QUADRUPLE 2-LINE-TO-1-LINE WITH STORAGE	2-State		20 ns from clock		65 mW	SN54LS298	J, W	SN74LS298	J, N	S-296
	2-State				195 mW	SN54298	J, W	SN74298	J, N	S-296
QUADRUPLE 2-LINE-TO-1-LINE	3-State	4 ns		14 ns	280 mW	SN54S258	J, W	SN74S258	J, N	S-244
	3-State		5 ns	14 ns	320 mW	SN54S257	J, W	SN74S257	J, N	S-244
	2-State	4 ns		7 ns	195 mW	SN54S158	J, W	SN74S158	J, N	S-163
	2-State		5 ns	8 ns	250 mW	SN54S157	J, W	SN74S157	J, N	S-163
	3-State	12 ns		20 ns	35 mW	SN54LS258	J, W	SN74LS258	J, N	S-244
	3-State		12 ns	20 ns	50 mW	SN54LS257	J, W	SN74LS257	J, N	S-244
	2-State	7 ns		12 ns	24 mW	SN54LS158	J, W	SN74LS158	J, N	S-163
	2-State		9 ns	14 ns	49 mW	SN54LS157	J, W	SN74LS157	J, N	S-163
	2-State		9 ns	14 ns	150 mW	SN54157	J, W	SN74157	J, N	S-163
	2-State		18 ns	27 ns	75 mW	SN54L157	J	SN74L157	J, N	S-163

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DECODERS/DEMULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPICAL SELECT	TYPICAL ENABLE	TYP TOTAL POWER	DEVICE TYPE AND PACKAGE				PAGE NO.†
		TIME	TIME	DISSIPATION	-55°C to 125°C		0°C to 70°C		
4-LINE-TO-16-LINE	Totem-Pole	23 ns	19 ns	170 mW	SN54154	J, W	SN74154	J, N	308
	Totem-Pole	46 ns	38 ns	85 mW	SN54L154	J	SN74L154	J, N	308
	Open-Collector	24 ns	19 ns	170 mW	SN54159	J, W	SN74159	J, N	323
4-LINE-TO-10-LINE, BCD-TO-DECIMAL	Totem-Pole	17 ns		35 mW	SN54LS42	J, W	SN54LS42	J, N	S-91
	Totem-Pole	17 ns		140 mW	SN5442A	J, W	SN7442A	J, N	
	Totem-Pole	34 ns		70 mW	SN54L42	J	SN74L42	J, N	
4-LINE-TO-10-LINE, EXCESS-3-TO-DECIMAL	Totem-Pole	17 ns		140 mW	SN5443A	J, W	SN7443A	J, N	S-91
	Totem-Pole	34 ns		70 mW	SN54L43	J	SN74L43	J, N	
4-LINE-TO-10-LINE EXCESS-3-GRAY-TO-DECIMAL	Totem-Pole	17 ns		140 mW	SN5444A	J, W	SN7444A	J, N	S-91
	Totem-Pole	34 ns		70 mW	SN54L44	J	SN74L44	J, N	
3-LINE-TO-8-LINE	Totem-Pole	8 ns	7 ns	225 mW	SN54S138	J, W	SN74S138	J, N	274
	Totem-Pole	22 ns	21 ns	31 mW	SN54LS138	J, W	SN74LS138	J, N	274
DUAL 2-LINE-TO-4-LINE	Totem-Pole	7.5 ns	6 ns	300 mW	SN54S139	J, W	SN74S139	J, N	274
	Totem-Pole	22 ns	19 ns	34 mW	SN54LS139	J, W	SN74LS139	J, N	274
	Totem-Pole	18 ns	15 ns	30 mW	SN54LS155	J, W	SN74LS155	J, N	S-157
	Totem-Pole	21 ns	16 ns	250 mW	SN54155	J, W	SN74155	J, N	S-157
	Open-Collector	23 ns	18 ns	250 mW	SN54156	J, W	SN74156	J, N	S-157
	Open-Collector	33 ns	26 ns	31 mW	SN54LS156	J, W	SN74LS156	J, N	S-157

OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS WITH COUNTERS/LATCHES

DESCRIPTION	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TYP TOTAL POWER DISSIPATION	BLANKING	DEVICE TYPE AND PACKAGE				PAGE NO.†
					-55°C to 125°C		0°C to 70°C		
BCD COUNTER/ 4-BIT LATCH/ BCD-TO-DECIMAL DECODER/DRIVER	7 mA	55 V	340 mW				SN74142	J, N	280
BCD COUNTER/ 4-BIT LATCH/ BCD-TO-SEVEN- SEGMENT DECODER/ LED DRIVER	Constant Current 15 mA	7 V	280 mW	Ripple	SN54143	J, W	SN74143	J, N	283
BCD COUNTER/ 4-BIT LATCH/ BCD-TO-SEVEN- SEGMENT DECODER/ LAMP DRIVER	20 mA 25 mA	15 V 15 V	280 mW 280 mW	Ripple Ripple	SN54144	J, W	SN74144	J, N	283 283

RESULTANT DISPLAYS USING '143, '144



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OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS

DESCRIPTION	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TYP TOTAL POWER DISSIPATION	BLANKING	DEVICE TYPE AND PACKAGE				PAGE NO.†
					-55°C to 125°C		0°C to 70°C		
BCD-TO-DECIMAL DECODERS/DRIVERS	80 mA	30 V	215 mW	Invalid Codes	SN5445	J, W	SN7445	J, N	171
	80 mA	15 V	35 mW	Invalid Codes			SN74LS145	J, N	S-154
	12 mA	15 V	35 mW	Invalid Codes	SN54LS145	J, W			S-154
	80 mA	15 V	215 mW	Invalid Codes	SN54145	J, W	SN74145	J, N	S-154
	7 mA	60 V	80 mW	Invalid Codes			SN74141	J, N	278
BCD-TO- SEVEN-SEGMENT DECODERS/DRIVERS	40 mA	30 V	320 mW	Ripple	SN5446A	J, W	SN7446A	J, N	S-96
	40 mA	30 V	320 mW	Ripple	SN54246	J, W	SN74246	J, N	S-233
	40 mA	15 V	320 mW	Ripple	SN5447A	J, W	SN7447A	J, N	S-96
	40 mA	15 V	320 mW	Ripple	SN54247	J, W	SN74247	J, N	S-233
	24 mA	15 V	35 mW	Ripple			SN74LS47	J, N	S-96
	24 mA	15 V	35 mW	Ripple			SN74LS247	J, N	S-233
	12 mA	15 V	35 mW	Ripple	SN54LS47	J, W			S-96
	12 mA	15 V	35 mW	Ripple	SN54LS247	J, W			S-233
	20 mA	30 V	133 mW	Ripple	SN54L46	J	SN74L46	J, N	S-96
	20 mA	15 V	133 mW	Ripple	SN54L47	J	SN74L47	J, N	S-96
	6.4 mA	5.5 V	265 mW	Ripple	SN5448	J, W	SN7448	J, N	S-96
	6.4 mA	5.5 V	265 mW	Ripple	SN54248	J, W	SN74248	J, N	S-233
	6 mA	5.5 V	125 mW	Ripple			SN74LS48	J, N	S-96
	6 mA	5.5 V	125 mW	Ripple			SN74LS248	J, N	S-233
	2 mA	5.5 V	125 mW	Ripple	SN54LS48	J, W			S-96
	2 mA	5.5 V	125 mW	Ripple	SN54LS248	J, W			S-233
	10 mA	5.5 V	165 mW	Direct	SN5449	W			S-96
	10 mA	5.5 V	265 mW	Direct	SN54249	J, W	SN74249	J, N	S-233
	8 mA	5.5 V	40 mW	Direct			SN74LS249	J, N	S-233
	4 mA	5.5 V	40 mW	Direct	SN54LS49	J, W	SN74LS49	J, N	S-96
	4 mA	5.5 V	40 mW	Direct	SN54LS249	J, W			S-233

RESULTANT DISPLAYS USING '46A, '47A, '48, '49, 'L46, 'L47, 'LS47, 'LS48, 'LS49

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----

RESULTANT DISPLAYS USING '246, '247, '248, '249, 'LS247, 'LS248, 'LS249

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----

†Page numbers with "S-" preceding the number refer to pages in this supplement; those without "S-" refer to pages in *The TTL Data Book for Design Engineers* (CC-411).

MSI/LSI FUNCTIONS
FUNCTIONAL INDEX/SELECTION GUIDE

ASYNCHRONOUS COUNTERS (RIPPLE CLOCK)–NEGATIVE-EDGE TRIGGERED

DESCRIPTION	COUNT FREQ	PARALLEL LOAD	CLEAR	TYP TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PAGE NO. [†]
					–55° C to 125° C		0° C to 70° C		
DECADE	50 MHz	Yes	Low	240 mW	SN54196	J, W	SN74196	J, N	451
	35 MHz	Yes	Low	150 mW	SN54176	J, W	SN74176	J, N	369
	32 MHz	Set-to-9	High	40 mW	SN54LS90	J, W	SN74LS90	J, N	S-127
	32 MHz	Set-to-9	High	40 mW	SN54LS290	J, W	SN74LS290	J, N	S-287
	32 MHz	Set-to-9	High	160 mW	SN5490A	J, W	SN7490A	J, N	S-127
	32 MHz	Set-to-9	High	160 mW	SN54290	J, W	SN74290	J, N	S-287
	30 MHz	Yes	Low	60 mW	SN54LS196	J, W	SN74LS196	J, N	451
	3 MHz	Set-to-9	High	20 mW	SN54L90	J,N,T	SN74L90	J,N,T	S-127
4-BIT BINARY	50 MHz	Yes	Low	240 mW	SN54197	J, W	SN74197	J, N	451
	35 MHz	Yes	Low	150 mW	SN54177	J, W	SN74177	J, N	369
	32 MHz	None	High	39 mW	SN54LS93	J, W	SN74LS93	J, N	S-127
	32 MHz	None	High	39 mW	SN54LS293	J, W	SN74LS293	J, N	S-287
	32 MHz	None	High	160 mW	SN5493A	J, W	SN7493A	J, N	S-127
	32 MHz	None	High	160 mW	SN54293	J, W	SN74293	J, N	S-287
	30 MHz	Yes	Low	60 mW	SN54LS197	J, W	SN74LS197	J, N	451
	3 MHz	None	High	20 mW	SN54L93	J,N,T	SN74L93	J,N,T	S-127
DIVIDE-BY-12	32 MHz	None	High	39 mW	SN54LS92	J, W	SN74LS92	J, N	S-127
	32 MHz	None	High	160 mW	SN5492A	J, W	SN7492A	J, N	S-127
DUAL DECADE	25 MHz	None	High	210 mW	SN54390	J, W	SN74390	J, N	S-321
	25 MHz	Set-to-9	High	225 mW	SN54490	J, W	SN74490	J, N	S-328
DUAL 4-BIT BINARY	25 MHz	None	High	190 mW	SN54393	J, W	SN74393	J, N	S-321

†Page numbers with "S-" preceding the number refer to pages in this supplement; those without "S-" refer to pages in *The TTL Data Book for Design Engineers* (CC-411).

MSI/LSI FUNCTIONS

FUNCTIONAL INDEX/SELECTION GUIDE

SYNCHRONOUS COUNTERS—POSITIVE-EDGE TRIGGERED

DESCRIPTION	COUNT FREQ	PARALLEL LOAD	CLEAR	TYP TOTAL POWER DISSIPATION	DEVICE TYPE AND PACKAGE				PAGE NO.†
					-55° C to 125° C		0° C to 70° C		
DECADE	40 MHz	Sync	Sync-L	475 mW	SN54S162	J, W	SN74S162	J, N	S-170
	25 MHz	Sync	Sync-L	93 mW	SN54LS162	J, W	SN74LS162	J, N	
	25 MHz	Sync	Async-L	93 mW	SN54LS160	J, W	SN74LS160	J, N	
	25 MHz	Sync	Sync-L	305 mW	SN54162	J, W	SN74162	J, N	
	25 MHz	Sync	Async-L	305 mW	SN54160	J, W	SN74160	J, N	
DECADE UP/DOWN	40 MHz	Sync	None	500 mW	SN54S168	J, W	SN74S168	J, N	S-192
	25 MHz	Sync	None	100 mW	SN54LS168	J, W	SN74LS168	J, N	S-192
	25 MHz	Async	Async-H	85 mW	SN54LS192	J, W	SN74LS192	J, N	427
	25 MHz	Async	Async-H	325 mW	SN54192	J, W	SN74192	J, N	427
	20 MHz	Async	None	100 mW	SN54LS190	J, W	SN74LS190	J, N	417
	20 MHz	Async	None	325 mW	SN54190	J, W	SN74190	J, N	417
	3 MHz	Async	Async-H	42 mW	SN54L192	J	SN74L192	J, N	427
DECADE RATE MULTIPLIER, $\frac{1}{N_{10}}$	25 MHz	Set-to-9	Async-H	270 mW	SN54167	J, W	SN74167	J, N	347
4-BIT BINARY	40 MHz	Sync	Sync-L	475 mW	SN54S163	J, W	SN74S163	J, N	S-170
	25 MHz	Sync	Sync-L	93 mW	SN54LS163	J, W	SN74LS163	J, N	
	25 MHz	Sync	Async-L	93 mW	SN54LS161	J, W	SN74LS161	J, N	
	25 MHz	Sync	Sync-L	305 mW	SN54163	J, W	SN74163	J, N	
	25 MHz	Sync	Async-L	305 mW	SN54161	J, W	SN74161	J, N	
4-BIT BINARY UP/DOWN	40 MHz	Sync	None	500 mW	SN54S169	J, W	SN74S169	J, N	S-192
	25 MHz	Sync	None	100 mW	SN54LS169	J, W	SN74LS169	J, N	S-192
	25 MHz	Async	Async-H	85 mW	SN54LS193	J, W	SN74LS193	J, N	427
	25 MHz	Async	Async-H	325 mW	SN54193	J, W	SN74193	J, N	427
	20 MHz	Async	None	90 mW	SN54LS191	J, W	SN74LS191	J, N	417
	20 MHz	Async	None	325 mW	SN54191	J, W	SN74191	J, N	417
	3 MHz	Async	Async-H	42 mW	SN54L193	J	SN74L193	J, N	427
6-BIT BINARY RATE MULTIPLIER, $\frac{1}{N_2}$	25 MHz		Async-H	345 mW	SN5497	J, W	SN7497	J, N	248

[†]Page numbers with "S-" preceding the number refer to pages in this supplement; those without "S-" refer to pages in *The TTL Data Book for Design Engineers* (CC-411).

BEAM-LEAD TTL CHIPS

FUNCTIONAL INDEX/SELECTION GUIDE

INVERTERS/NAND/NOR/AND/OR GATES WITH TOTEM-POLE OUTPUTS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE		PAGE NO.†
			-55°C to 125°C	0°C to 70°C	
HEX INVERTERS	9.5 ns	2 mW	BL54LS04Y	BL74LS04Y	568
QUADRUPLE 2-INPUT POSITIVE-NAND GATES	9.5 ns	2 mW	BL54LS00Y	BL74LS00Y	568
	10 ns	10 mW	BL5400Y	BL7400Y	543
	33 ns	1 mW	BL54L00Y	BL74L00Y	545
TRIPLE 3-INPUT POSITIVE-NAND GATES	9.5 ns	2 mW	BL54LS10Y	BL74LS10Y	S-341
	10 ns	10 mW	BL5410Y	BL7410Y	543
DUAL-4-INPUT POSITIVE-NAND GATES	9.5 ns	2 mW	BL54LS20Y	BL74LS20Y	568
	33 ns	1 mW	BL54L20Y	BL74L20Y	545
8-INPUT POSITIVE-NAND GATES	17 ns	2 mW	BL54LS30Y	BL74LS30Y	568
	33 ns	1 mW	BL54L30Y	BL74L30Y	549
QUADRUPLE 2-INPUT POSITIVE-NOR GATES	10 ns	2.75 mW	BL54LS02Y	BL74LS02Y	568
QUADRUPLE 2-INPUT POSITIVE-AND GATES	12 ns	4.25 mW	BL54LS08Y	BL74LS08Y	568
TRIPLE 3-INPUT POSITIVE-AND GATES	12 ns	4.25 mW	BL54LS11Y	BL74LS11Y	568
DUAL 4-INPUT POSITIVE-AND GATES	12 ns	4.25 mW	BL54LS21Y	BL74LS21Y	568
QUADRUPLE 2-INPUT POSITIVE-OR GATES	12 ns	5 mW	BL54LS32Y	BL74LS32Y	568

INVERTERS/NAND/AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE		PAGE NO.†
			-55°C to 125°C	0°C to 70°C	
HEX INVERTERS	16 ns	2 mW	BL54LS05Y	BL74LS05Y	568
QUADRUPLE 2-INPUT POSITIVE-NAND GATES	16 ns	2 mW	BL54LS01Y	BL74LS01Y	568
	16 ns	2 mW	BL54LS03Y	BL74LS03Y	568
	22 ns	10 mW	BL5401Y	BL7401Y	547
DUAL 4-INPUT POSITIVE-NAND GATES	16 ns	2 mW	BL54LS22Y	BL74LS22Y	568
QUADRUPLE 2-INPUT POSITIVE-AND GATES	20 ns	4.25 mW	BL54LS09Y	BL74LS09Y	568
TRIPLE 3-INPUT POSITIVE-AND GATES	20 ns	4.25 mW	BL54LS15Y	BL74LS15Y	568

BUFFERS WITH TOTEM-POLE OUTPUTS

DESCRIPTION	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT VOLTAGE	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE		PAGE NO.†
				-55°C to 125°C	0°C to 70°C	
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS	24 mA	-1.2 mA	4.3 mW		BL74LS37Y	568
	12 mA	-1.2 mA	4.3 mW	BL54LS37Y		
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS	24 mA	-1.2 mA	5.5 mW		BL74LS28Y	568
	12 mA	-1.2 mA	5.5 mW	BL54LS28Y		

BUFFERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT VOLTAGE	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE		PAGE NO.†
				-55°C to 125°C	0°C to 70°C	
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS	24 mA	5.5 V	4.3 mW		BL74LS38Y	568
	12 mA	5.5 V	4.3 mW	BL54LS38Y		
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS	24 mA	5.5 V	5.45 mW		BL74LS33Y	568
	12 mA	5.5 V	5.45 mW	BL54LS33Y		

†Page numbers with "S-" preceding the number refer to pages in this supplement; those without "S-" refer to pages in *The TTL Data Book for Design Engineers* (CC-411).

BEAM-LEAD TTL CHIPS

FUNCTIONAL INDEX/SELECTION GUIDE

AND-OR-INVERT GATES

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER BIT	TEMPERATURE RANGE		PAGE NO. [†]
			-55°C to 125°C	0°C to 70°C	
4-WIDE 2-3-2-INPUT AND-OR-INVERT GATES	12.5 ns	4.5 mW	BL54LS54Y	BL74LS54Y	568
2-WIDE 4-INPUT AND-OR-INVERT GATES	12.5 ns	2.75 mW	BL54LS55Y	BL74LS55Y	568
	43 ns	1.5 mW	BL54LS55Y	BL74LS55Y	551
DUAL 2-WIDE AND-OR-INVERT GATES	12.5 ns	2.75 mW	BL54LS51Y	BL74LS51Y	568

FLIP-FLOPS

DESCRIPTION	TEMPERATURE RANGE		PAGE NO. [†]
	-55°C to 125°C	0°C to 70°C	
J-K EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET	BL54L67Y	BL74L67Y	553
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET	BL54LS76Y	BL74LS76Y	S-341
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR	BL54L68Y	BL74L68Y	556
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK	BL54L69Y	BL74L69Y	559
DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH CLEAR	BL5473Y	BL7473Y	562
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET	BL5474Y	BL7474Y	565

MSI FUNCTIONS

DESCRIPTION/FEATURES		TEMPERATURE RANGE		PAGE NO. [†]
		-55°C to 125°C	0°C to 70°C	
PARALLEL-IN, PARALLEL-OUT, 4-BIT SHIFT REGISTERS	BIDIRECTIONAL	BL54LS194Y	BL74LS194Y	568
	D-TYPE SERIAL INPUT	BL54LS95AY	BL74LS95AY	
	J-K SERIAL INPUTS	BL54LS195Y	BL74LS195Y	
	THREE-STATE OUTPUTS	BL54LS295Y	BL74LS295Y	
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS	TWO-STATE OUTPUTS	BL54LS153Y	BL74LS153Y	
	THREE-STATE OUTPUTS	BL54LS253Y	BL74LS253Y	
	3-LINE-TO-8-LINE	BL54LS138Y	BL74LS138Y	
DECODERS/DEMULTIPLEXERS	DUAL 2-LINE-TO-4-LINE	BL54LS139Y	BL74LS139Y	
		BL54LS155Y	BL74LS155Y	
30-MHz COUNTERS/LATCHES	DECADE	BL54LS196Y	BL74LS196Y	
	4-BIT BINARY	BL54LS197Y	BL74LS197Y	
4-BIT ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR		BL54LS181Y	BL74LS181Y	
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES	TOTEM-POLE OUTPUTS	BL54LS86Y	BL74LS86Y	S-341
	OPEN-COLLECTOR OUTPUTS	BL54LS136Y	BL74LS136Y	
QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES		BL54LS266Y	BL74LS266Y	

[†]Page numbers with "S-" preceding the number refer to pages in this supplement; those without "S-" refer to pages in *The TTL Data Book for Design Engineers* (CC-411).

RADIATION-HARDENED TTL FUNCTIONAL INDEX/SELECTION GUIDE

INVERTERS AND POSITIVE-NAND GATES

DESCRIPTION	TYPE NO.	PACKAGE	PAGE NO. [†]
HEX INVERTERS	RSN5404	H	585
	RSN54H04	H	585
QUADRUPL 2-INPUT POSITIVE-NAND GATES	RSN5400	H	581
	RSN54H00	H	581
	RSN54L00	H	583
TRIPLE 3-INPUT POSITIVE-NAND GATES	RSN5410	H	581
	RSN54H10	H	581
	RSN54L10	H	583
DUAL 3-INPUT POSITIVE-NAND GATE	RSN54L130	H	583
DUAL EXPANDABLE 3-INPUT POSITIVE-NAND GATE	RSN54L131	H	583
DUAL 4-INPUT POSITIVE-NAND GATES	RSN5420	H	581
	RSN54H20	H	581
	RSN54L20	H	583
DUAL 4-INPUT POSITIVE-NAND BUFFERS	RSN5440	H	586
	RSN54H40	H	586
11-INPUT POSITIVE-NAND GATES	RSN5431	H	581
	RSN54H31	H	581

AND-OR INVERT GATES

DESCRIPTION	TYPE NO.	PACKAGE	PAGE NO. [†]
4-WIDE 3-3-2-3-INPUT AND-OR-INVERT GATES	RSN5457	H	587
	RSN54H57	H	587
	RSN54L57	H	589
2-WIDE 4-INPUT AND-OR-INVERT GATES	RSN5458	H	587
	RSN54H58	H	587
2-WIDE 3-INPUT, 2-WIDE 2-INPUT DUAL AND-OR-INVERT GATES	RSN5456	H	587
	RSN54H56	H	587
DUAL 2-WIDE 3-2-INPUT AND-OR-INVERT GATE	RSN54H66	H	587

FLIP-FLOPS

DESCRIPTION	TYPE NO.	PACKAGE	PAGE NO. [†]
S-R MASTER-SLAVE FLIP-FLOP	RSN54L71	H	590
J-K MASTER-SLAVE FLIP-FLOP	RSN54L72	H	593
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS	RSN5474	H	596
	RSN54H74	H	596
	RSN54L74	H	596
DUAL J-K EDGE-TRIGGERED FLIP-FLOP	RSN54H103	H	600

DECODER/DEMULTIPLEXER

DESCRIPTION	TYPE NO.	PACKAGE	PAGE NO. [†]
3-LINE-TO-8-LINE DECODER/DEMULTIPLEXER	RSN54H149	H	603

[†] Page numbers with "S-" preceding the number refer to pages in this supplement; those without "S-" refer to pages in *The TTL Data Book for Design Engineers* (CC-411).

Ordering Instructions and Mechanical Data

TTL INTEGRATED CIRCUITS MECHANICAL DATA

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. Except for the beam-lead chips, the availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section. Beam-lead chip designations and outlines are shown on individual data sheets.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

1

EXAMPLE: SN 54LS75 J -00

1. Prefix

MUST CONTAIN TWO OR THREE LETTERS
(From Individual Data Sheet)

RSN Radiation-Hardened Circuit
SN Standard Prefix
SNM Mach IV, Level I
SNA Mach IV, Level II
SNC Mach IV, Level III
SNH Mach IV, Level IV

2. Unique Circuit Description

MUST CONTAIN FOUR TO EIGHT CHARACTERS
(From Individual Data Sheet)

Examples: 5410
74H10
54S112
54L78
74LS295A
74188A

3. Package

MUST CONTAIN A SINGLE LETTER
H, J, N, T, W
(From Pin-Connection Diagram on Individual Data Sheet)

4. Instructions (Dash No.)

MUST CONTAIN TWO NUMBERS
(From Dash No. Column of Following Table)

PACKAGES	FORMED LEADS	SOLDER-DIPPED LEADS	INSULATOR	CARRIER	ORDER DASH NO.
METAL FLAT PACKAGES					
T	No	No	No	t	00
T	Yes	No	Yes	t	01
T	No	No	No	Mech-Pak	02
T	No	No	Yes	Mech-Pak	03
T	Yes	No	No	Mech-Pak	04
T	Yes	No	Yes	Mech-Pak	05
T	No	No	Yes	t	06
T	Yes	No	No	t	07
T	No	Yes	No	t	10
T	Yes	Yes	Yes	t	11
T	No	Yes	No	Mech-Pak	12
T	No	Yes	Yes	Mech-Pak	13
T	Yes	Yes	No	Mech-Pak	14
T	Yes	Yes	Yes	Mech-Pak	15
T	No	Yes	Yes	t	16
T	Yes	Yes	No	t	17
CERAMIC FLAT PACKAGES					
H, W	No	No	N/A	t	00
H	No	No	N/A	Mech-Pak	02
H, W	No	Yes	N/A	t	10
DUAL-IN-LINE PACKAGES					
J, N	No	No	N/A	t	00
N	No	Yes	N/A	t	10

†These circuits are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method which will best suit your particular needs.

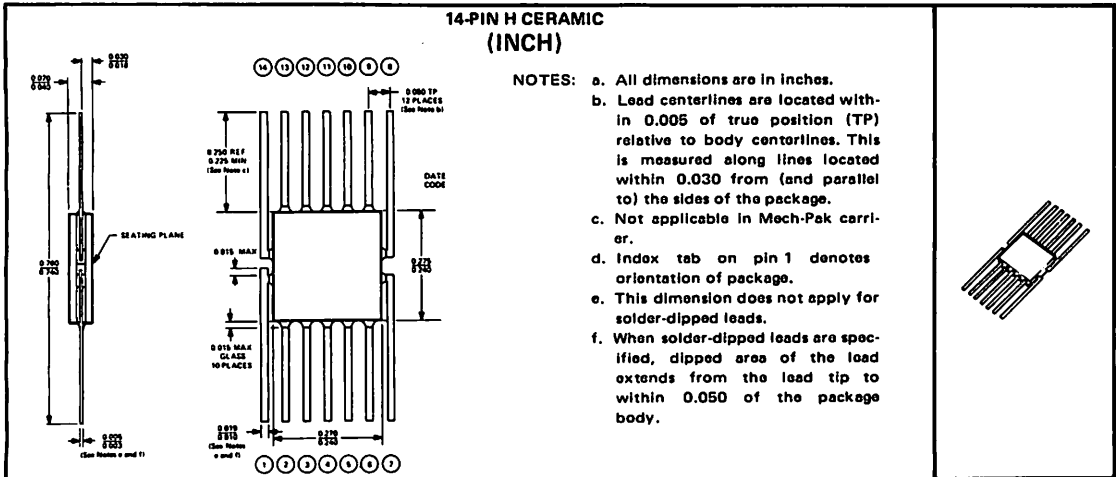
- Flat (H, T, W)
- Mech-Pakette
 - Barnes Carrier
 - Milton Ross Carrier

- Dual-in-line (J, N)
- Slide Magazines
 - A-Channel Plastic Tubing
 - Barnes Carrier (N only)
 - Sectioned Cardboard Box
 - Individual Plastic Box

TTL INTEGRATED CIRCUITS MECHANICAL DATA

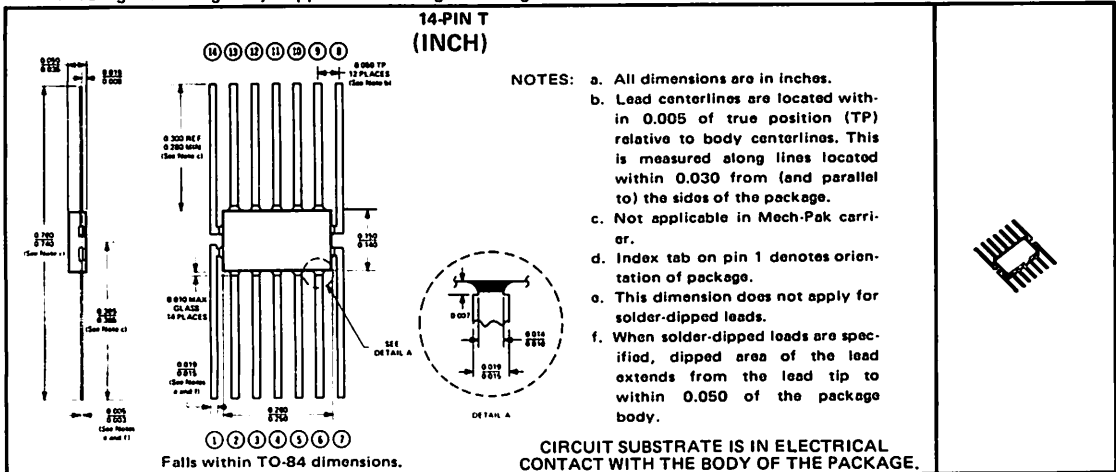
H flat package (inch dimensions, see page S-41 for metric dimensions)

This package consists of a ceramic base, ceramic cap, and a 14-lead frame. Hermetic sealing is accomplished with glass. Gold-plated leads (-00) require no additional cleaning or processing when used in welded or soldered assembly.



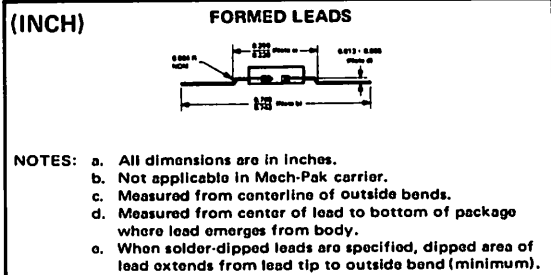
T flat package (inch dimensions, see page S-41 for metric dimensions)

This hermetic package features glass-to-metal seals and welded construction. Package body and leads are gold-plated F-15[‡] glass-sealing alloy. Approximate weight is 0.1 gram.



T package leads

Gold-plated F-15[‡] leads require no additional cleaning or processing when used in soldered or welded assembly. Solder-dipped leads are also available. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Circuits can be removed from Mech-Pak carriers with lead lengths up to 0.300 inch.

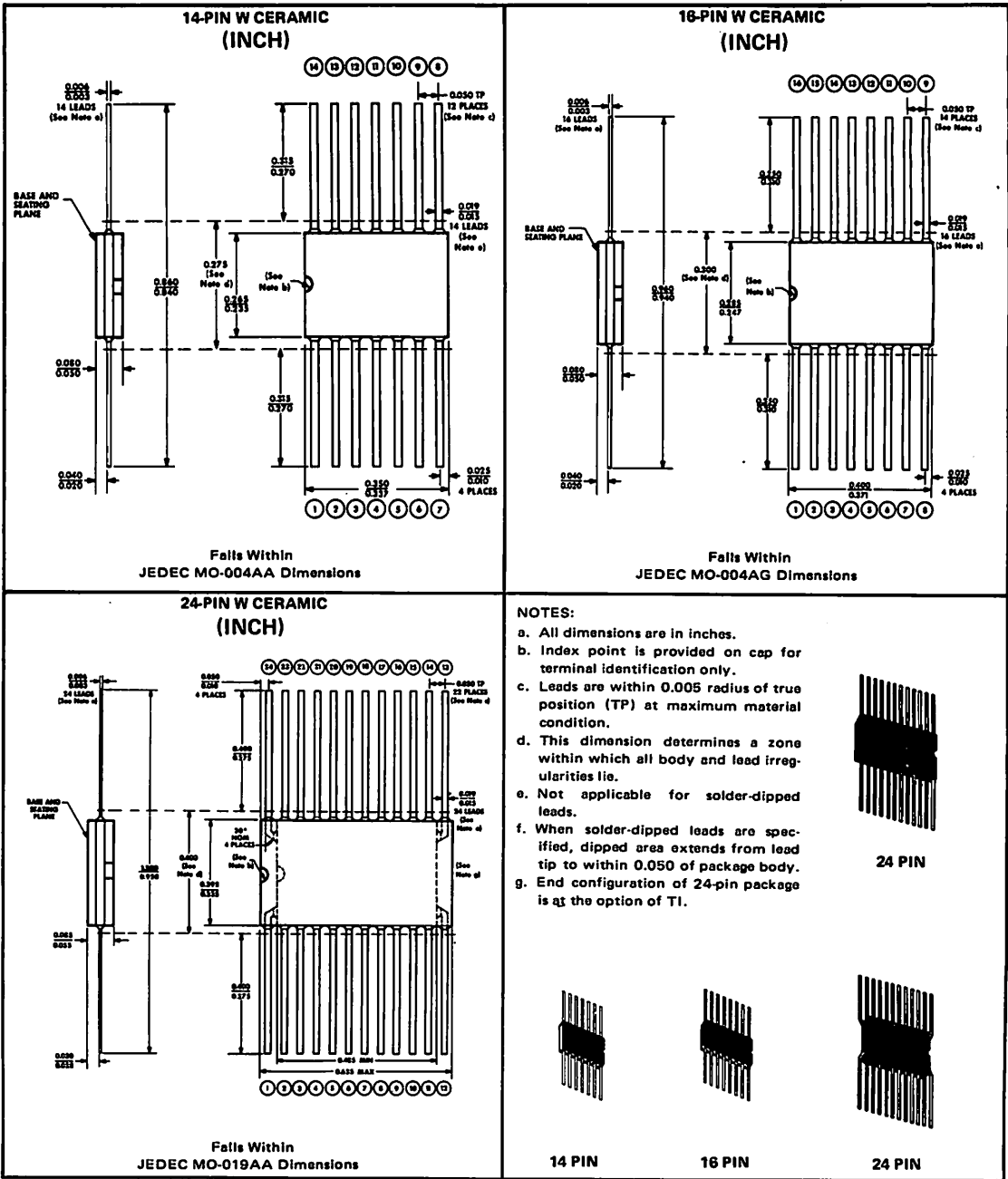


[‡]F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

TTL INTEGRATED CIRCUITS MECHANICAL DATA

W ceramic flat packages (inch dimensions, see page S-42 for metric dimensions)

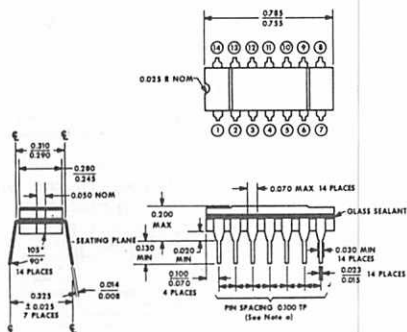
These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap, and a 14-, 16-, or 24-lead frame. Hermetic sealing is accomplished with glass. Tin-plated ("bright-dipped") leads (-00) require no additional cleaning or processing when used in soldered assembly.



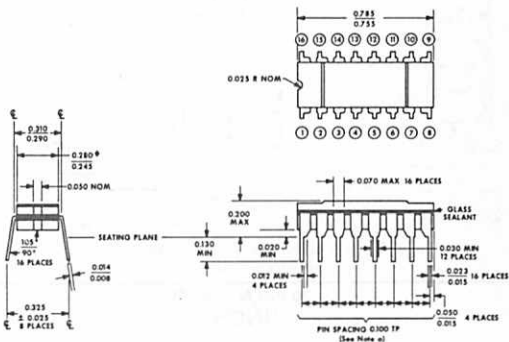
1

These hermetically sealed, dual-in-line packages consist of a ceramic base, ceramic cap, and a 14-, 16-, or 24-lead frame. The packages are intended for insertion in mounting-hole rows on 0.300-inch (or 0.600-inch) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (-00) require no additional cleaning or processing when used in soldered assembly.

16-PIN J CERAMIC
(INCH)

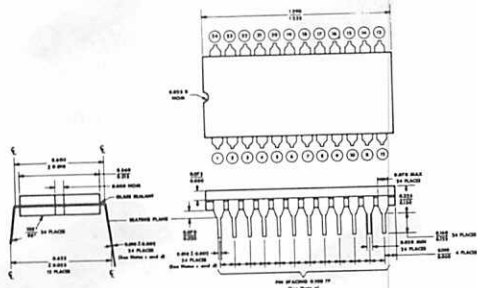


Falls Within JEDEC TO-116 and
MO-001AA Dimensions



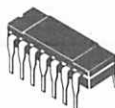
♦For memories of 64 bits and up and a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, this maximum is 0.300-inch. All other dimensions apply without modification.

24-PIN J CERAMIC
(INCH)

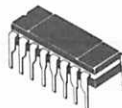


Falls Within
JEDEC MO-015AA Dimensions

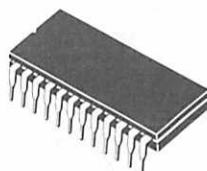
NOTES: a. Each pin centerline is located within 0.010 of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.



14-PIN



16-PIN

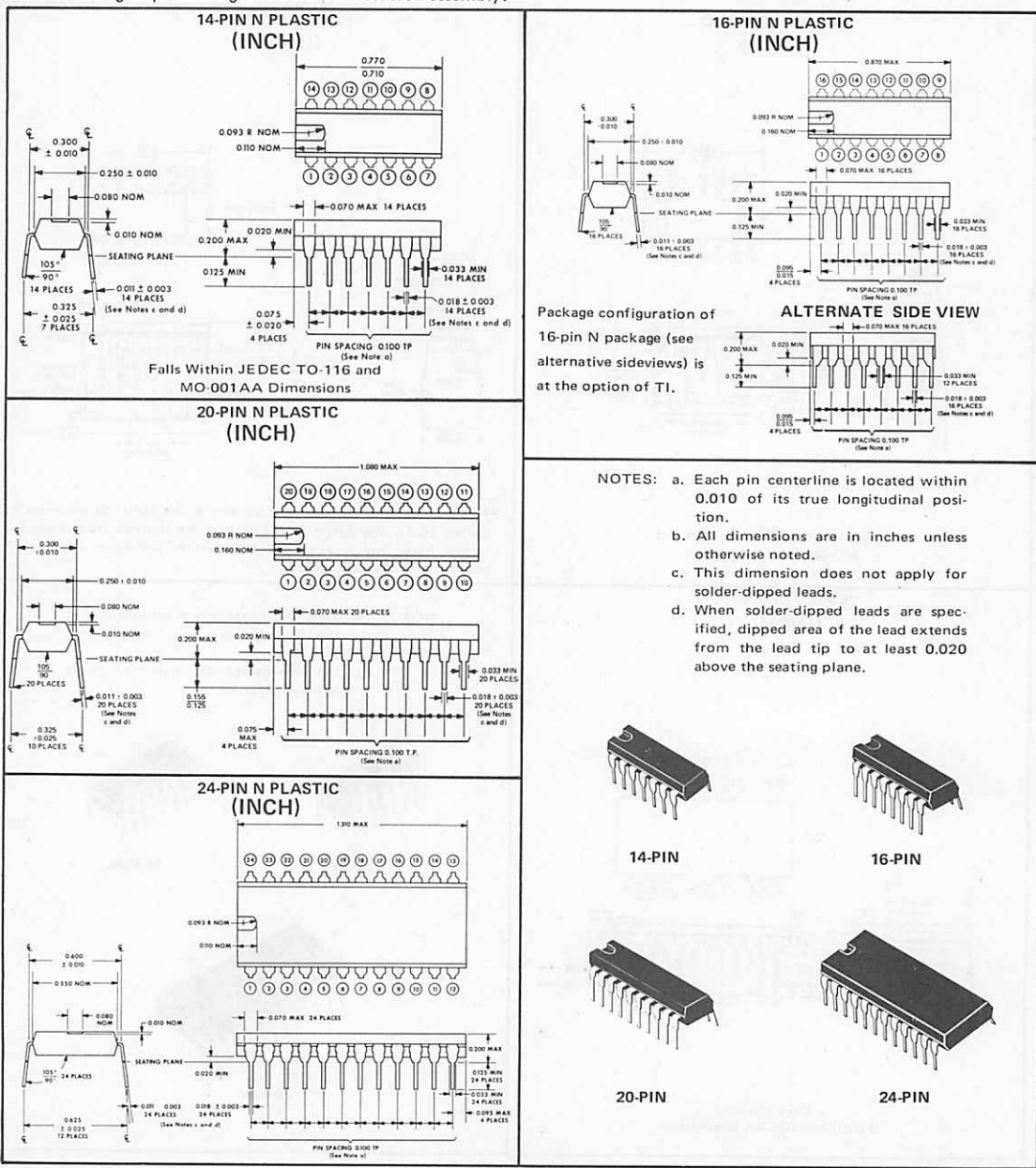


24-PIN

TTL INTEGRATED CIRCUITS MECHANICAL DATA

N plastic dual-in-line packages (inch dimensions, see page S-44 for metric dimensions)

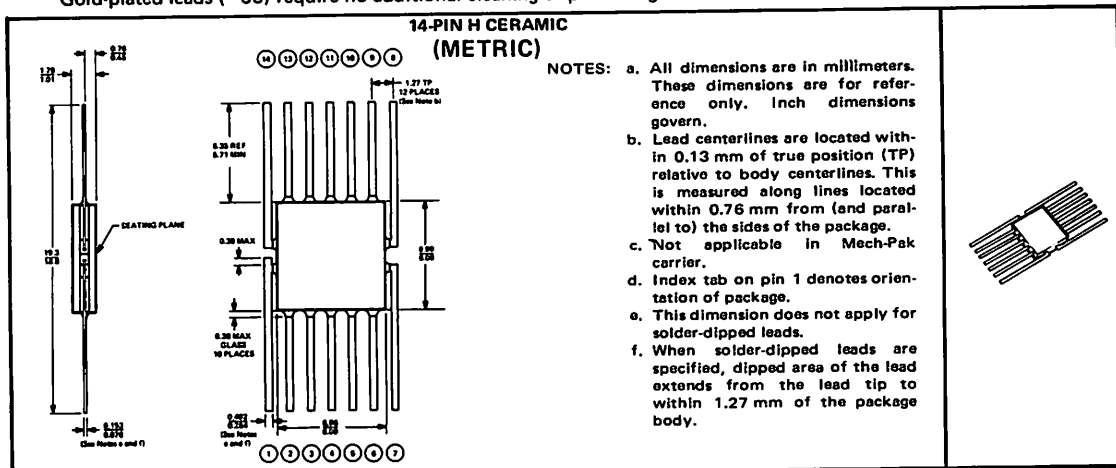
These dual-in-line packages consist of a circuit mounted on a 14-, 16-, 20-, or 24-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300-inch (or 0.600-inch) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



TTL INTEGRATED CIRCUITS MECHANICAL DATA

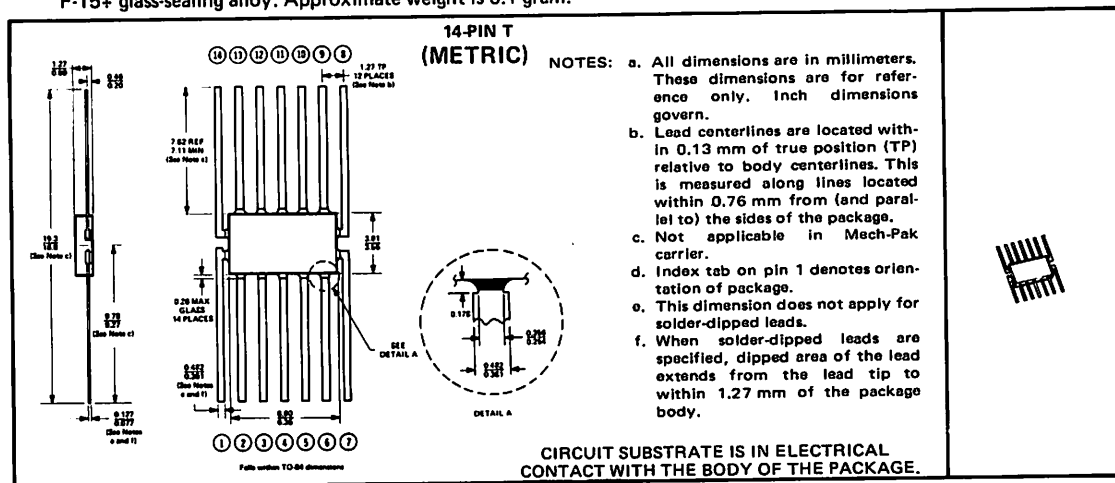
H flat package (metric dimensions, see page S-37 for inch dimensions)

This package consists of a ceramic base, ceramic cap, and a 14-lead frame. Hermetic sealing is accomplished with glass. Gold-plated leads (—00) require no additional cleaning or processing when used in welded or soldered assembly.



T flat package (metric dimensions, see page S-37 for inch dimensions)

This hermetic package features glass-to-metal seals and welded construction. Package body and leads are gold-plated F-15[‡] glass-sealing alloy. Approximate weight is 0.1 gram.

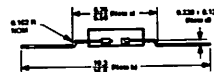


T package leads

Gold-plated F-15[‡] leads require no additional cleaning or processing when used in soldered or welded assembly. Solder-dipped leads are also available. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Circuits can be removed from Mech-Pak carriers with lead lengths up to 7.62 mm.

(METRIC)

FORMED LEADS



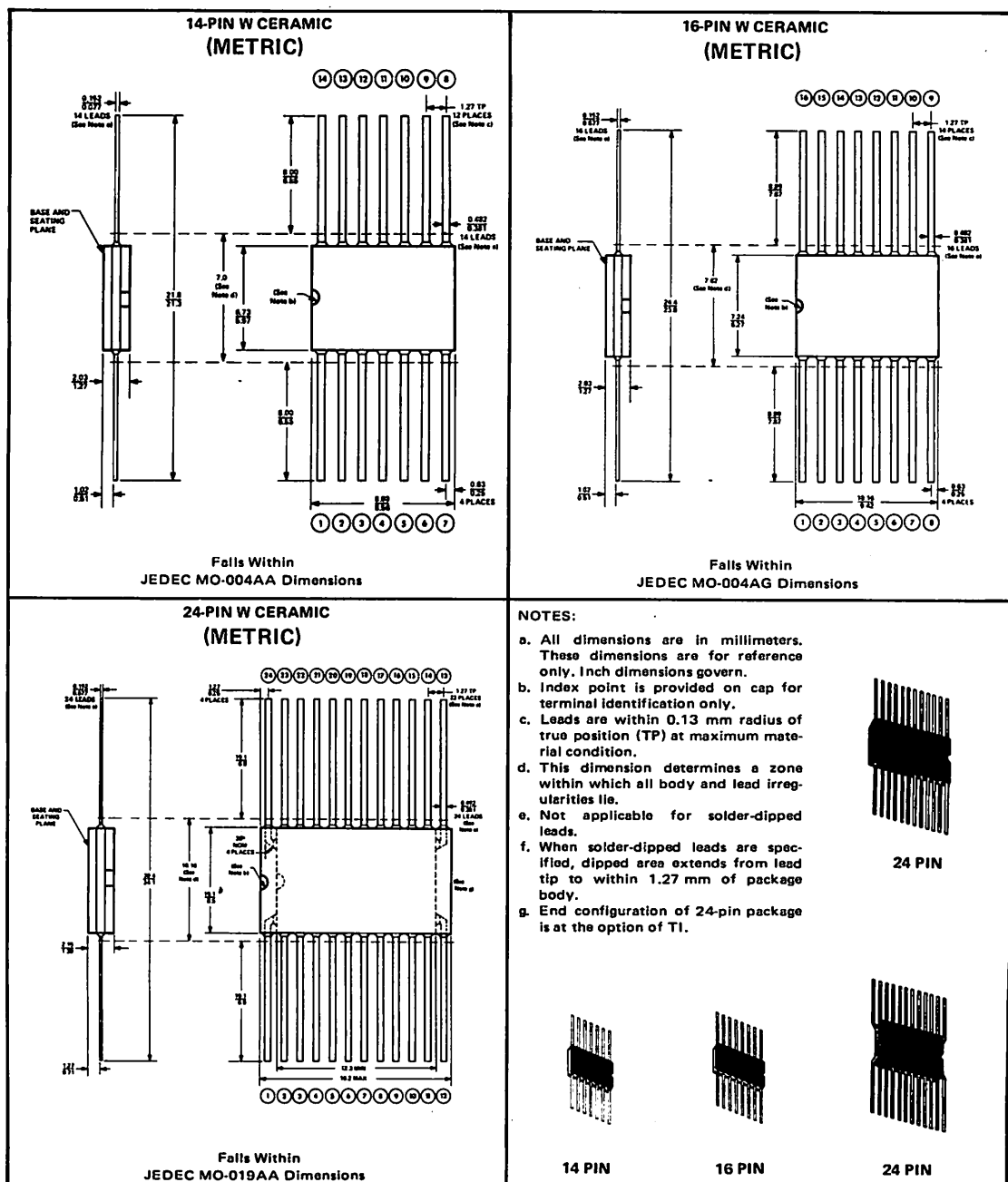
- NOTES:**
- All dimensions are in millimeters. These dimensions are for reference only. Inch dimensions govern.
 - Not applicable in Mech-Pak carrier.
 - Measured from centerline of outside bends.
 - Measured from center of lead to bottom of package where lead emerges from body.
 - When solder-dipped leads are specified, dipped area of lead extends from lead tip to outside bend (minimum).

[‡]F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

TTL INTEGRATED CIRCUITS MECHANICAL DATA

W ceramic flat packages (metric dimensions, see page S-38 for inch dimensions)

These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap, and a 14-, 16-, or 24-lead frame. Hermetic sealing is accomplished with glass. Tin-plated ("bright-dipped") leads (-00) require no additional cleaning or processing when used in soldered assembly.

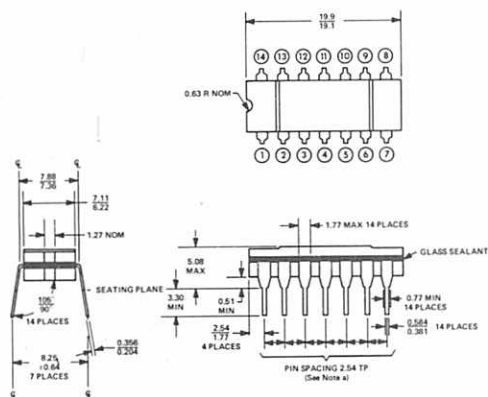


TTL INTEGRATED CIRCUITS MECHANICAL DATA

J ceramic dual-in-line packages (metric dimensions, see page S-39 for inch dimensions)

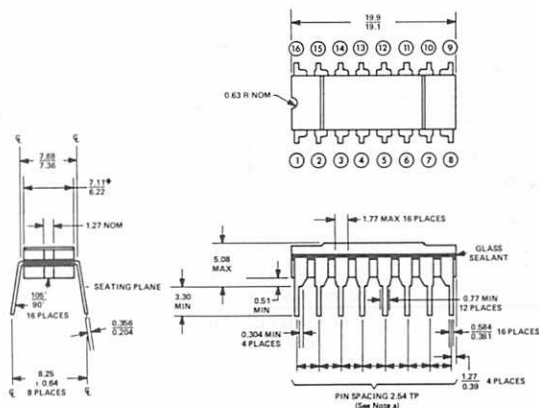
These hermetically sealed, dual-in-line packages consist of a ceramic base, ceramic cap, and a 14-, 16-, or 24-lead frame. The packages are intended for insertion in mounting-hole rows on 7.62-mm (or 15.24-mm) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (-00) require no additional cleaning or processing when used in soldered assembly.

14-PIN J CERAMIC (METRIC)



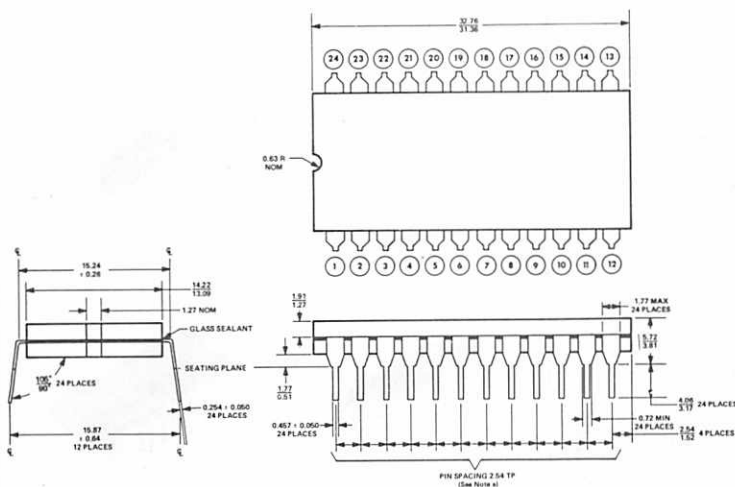
Falls Within JEDEC TO-116 and
MO-001AA Dimensions

16-PIN J CERAMIC (METRIC)



For memories of 64 bits and up and a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, this maximum is 7.62-mm. All other dimensions apply without modification.

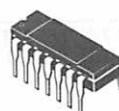
24-PIN J CERAMIC (METRIC)



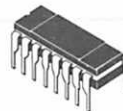
Falls Within
JEDEC MO-015AA Dimensions

NOTES:

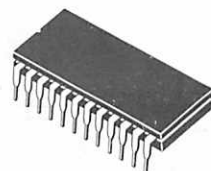
- Each pin centerline is located within 0.26 mm of its true longitudinal position.
- All dimensions are in millimeters unless otherwise noted. These dimensions are for reference only. Inch dimensions govern.



14-PIN



16-PIN



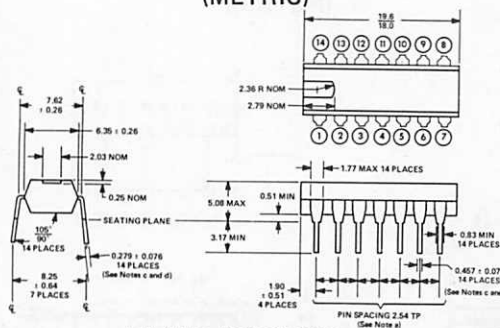
24-PIN

TTL INTEGRATED CIRCUITS MECHANICAL DATA

N plastic dual-in-line packages (metric dimensions, see page S-40 for inch dimensions)

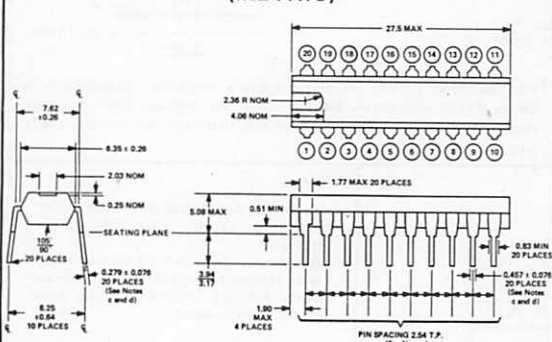
These dual-in-line packages consist of a circuit mounted on a 14-, 16-, 20-, or 24-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 7.62-mm (or 15.24-mm) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

14-PIN N PLASTIC
(METRIC)

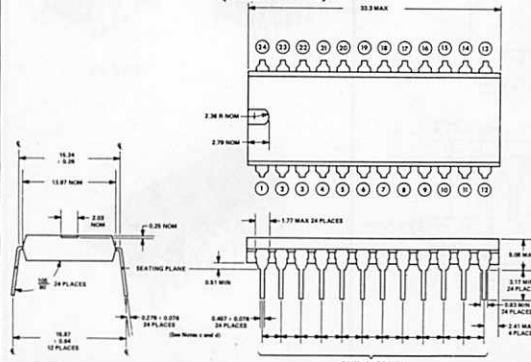


Falls Within JEDEC TO-116 and
MO-001AA Dimensions

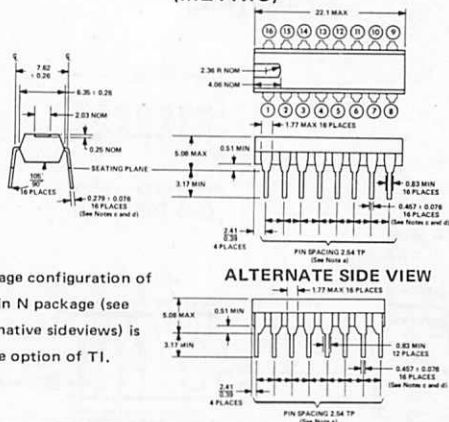
20-PIN N PLASTIC
(METRIC)



24-PIN N PLASTIC
(METRIC)



16-PIN N PLASTIC
(METRIC)



Package configuration of
16-pin N package (see
alternative sideviews) is
at the option of TI.

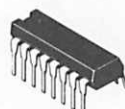
ALTERNATE SIDE VIEW

NOTES:

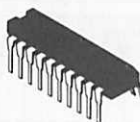
- Each pin centerline is located within 0.26 mm of its true longitudinal position.
- All dimensions are in millimeters unless otherwise noted. These dimensions are for reference only. Inch dimensions govern.
- This dimension does not apply for solder-dipped leads.
- When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.5 mm above the seating plane.



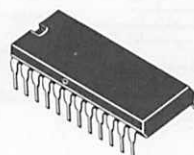
14-PIN N



16-PIN N



20-PIN N



24-PIN N

54/74 Family SSI Circuits

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

This table, which covers the SSI circuits of the entire 54/74 family, is reprinted here for convenience. For information on the treatment of unused inputs of positive-AND/NAND gates, on input-current requirements, and on drive capability of outputs, see pages 60 and 61 of *The TTL Data Book for Design Engineers*, CC-411.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		54 FAMILY	SERIES 54 SERIES 54H	SERIES 54L	SERIES 54LS	SERIES 54LS	SERIES 54S	UNIT	
		74 FAMILY	SERIES 74 SERIES 74H	SERIES 74L	SERIES 74LS WITH DIODE INPUTS	SERIES 74LS WITH EMITTER INPUTS	SERIES 74S		
Supply voltage, V _{CC} (see Note 1)			7	8	7	7	7	V	
Input voltage			5.5	5.5	7	5.5	5.5	V	
Interemitter voltage (see Note 2)			5.5	5.5		5.5	5.5	V	
Off-state (high-level) voltage applied to open-collector outputs	'06, '07	30						V	
	'16, '17, '26	15							
	Others		8	7	7	7			
Operating free-air temperature range	54 Family	-55 to 125						°C	
	74 Family	0 to 70							
Storage temperature range			-65 to 150						°C

- NOTES: 1. Voltage values, unless otherwise noted, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these SSI circuits, this rating applies between inputs that go directly into the same AND or NAND gate in the functional block diagram.

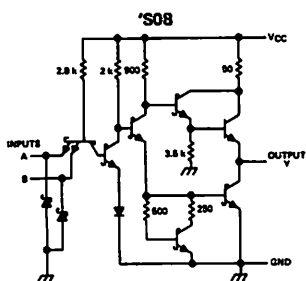
TYPES SN54S08, SN54S09, SN74S08, SN74S09
QUADRUPLE 2-INPUT POSITIVE AND GATES

BULLETIN NO. DL-S 7412082, MARCH 1974

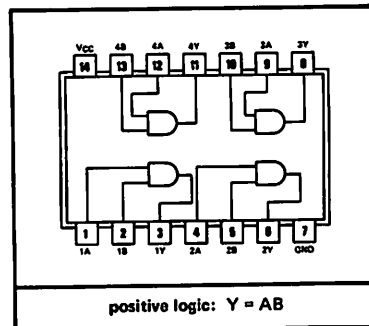
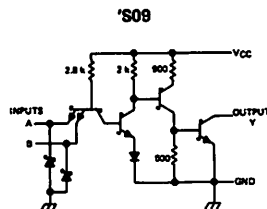
- 'S08 has active pullups
- 'S09 has open-collector outputs

SN54S08, SN54S09 ... J OR W PACKAGE
SN74S08, SN74S09 ... J OR N PACKAGE
(TOP VIEW)

schematics (each gate)



Resistor values shown are nominal and in ohms.



recommended operating conditions

	SN54S08			SN54S09			SN74S08			SN74S09			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}						5.5						5.5	V
High-level output current, I_{OH}			-1						-1				mA
Low-level output current, I_{OL}			20			20			20			20	mA
Operating free-air temperature	-55		125	-55		125	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'S08			'S09			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OH} = -1 \text{ mA}$	2.5	3.4					V
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{OH} = 5.5 \text{ V}$						250	µA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			50			50	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.5 \text{ V}$			-2			-2	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100				mA
I_{CCH} Supply current, all outputs high	$V_{CC} = \text{MAX}$	18		32	18		32	mA
I_{CCL} Supply current, all outputs low	$V_{CC} = \text{MAX}$	32		57	32		57	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	'S08			'S09			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	$R_L = 280 \Omega$, See Note 2	$C_L = 15 \text{ pF}$	4.5	7	6.5	10		ns
		$C_L = 50 \text{ pF}$	6		9			
t_{PHL} Propagation delay time, high-to-low-level output		$C_L = 15 \text{ pF}$	5	7.5	6.5	10		ns
		$C_L = 50 \text{ pF}$	7.5		9			

NOTES: 1. All voltage values are with respect to network ground terminal.

2. Load circuit and voltage waveforms are shown on page S-87.

PRINTED IN U.S.A.

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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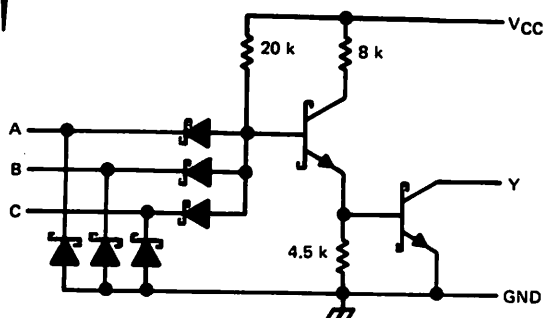
S-47

TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

BULLETIN NO. DLS 7412086, MARCH 1974

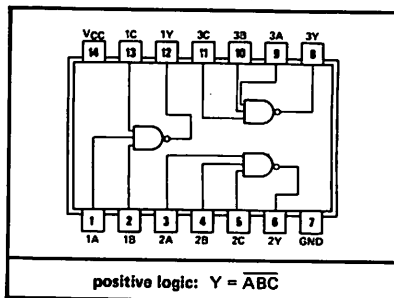
Functionally and Mechanically Identical to SN5412/SN7412

schematic (each gate)



Resistor values shown are nominal and in ohms.

SN54LS12 ... J OR W PACKAGE
SN74LS12 ... J OR N PACKAGE
(TOP VIEW)



recommended operating conditions

	SN54LS12			SN74LS12			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS12			SN74LS12			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{OH} = 5.5 \text{ V}$			100			100	μA
	$V_{IL} = 0.7 \text{ V}$							
	$V_{IL} = 0.8 \text{ V}$							
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}$			0.25			0.25	V
	$I_{OL} = 4 \text{ mA}$						0.35	
	$I_{OL} = 8 \text{ mA}$						0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.36			-0.36	mA
I_{CCH} Supply current, outputs high	$V_{CC} = \text{MAX}, \text{All inputs at } 0 \text{ V}$			0.7			0.7	mA
I_{CCL} Supply current, outputs low	$V_{CC} = \text{MAX}, \text{All inputs at } 4.5 \text{ V}$			1.8			1.8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$		17	32	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Note 2		15	28	ns

NOTE 2: Load circuit and voltage waveforms are shown on page S-88.

TTL
SSI

TYPES SN54LS13, SN54LS14, SN74LS13, SN74LS14 **SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS** **WITH TOTEM-POLE OUTPUTS**

BULLETIN NO. DL-S 7412111, MARCH 1974

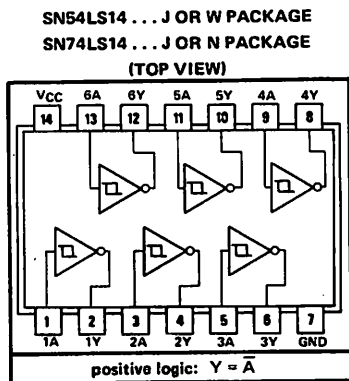
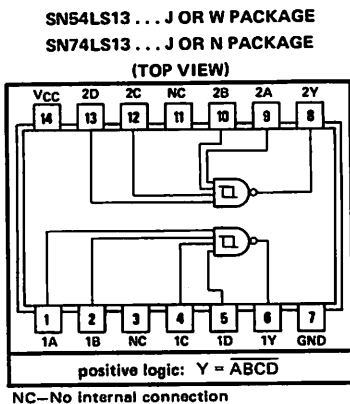
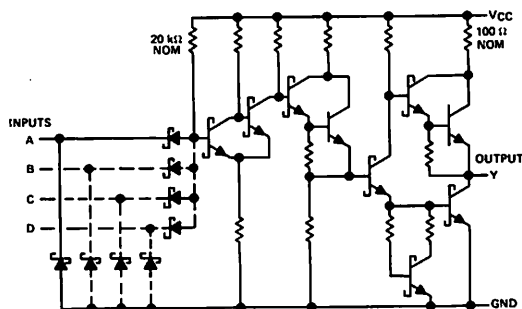
- Operation from Very Slow Transitions
- Temperature-Compensated Threshold Levels
- Temperature-Compensated Hysteresis, Typically 0.8 V
- High Noise Immunity

description

Each circuit functions as a NAND gate or inverter, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The hysteresis or backlash, which is the difference between the two threshold levels, is typically 800 millivolts.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

schematic (each gate)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS13, SN54LS14	-55°C to 125°C
SN74LS13, SN74LS14	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

2

TYPES SN54LS13, SN54LS14, SN74LS13, SN74LS14

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS13 SN54LS14			SN74LS13 SN74LS14			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+} Positive-going threshold voltage	$V_{CC} = 5\text{ V}$	1.5	1.7	2	1.5	1.7	2	V
V_{T-} Negative-going threshold voltage	$V_{CC} = 5\text{ V}$	0.6	0.9	1.1	0.6	0.9	1.1	V
$V_{T+} - V_{T-}$ Hysteresis	$V_{CC} = 5\text{ V}$	0.4	0.8		0.4	0.8		V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18\text{ mA}$		-1.5			-1.5		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, I_{OH} = -400\text{ }\mu\text{A}, V_I = 0.6\text{ V}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_I = 2\text{ V}, I_{OL} = 4\text{ mA}$		0.25	0.4		0.25	0.4	V
	$I_{OL} = 8\text{ mA}$					0.35	0.5	
I_{T+} Input current at positive-going threshold	$V_{CC} = 5\text{ V}, V_I = V_{T+}$		-0.14			-0.14		mA
I_{T-} Input current at negative-going threshold	$V_{CC} = 5\text{ V}, V_I = V_{T-}$		-0.18			-0.18		mA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7\text{ V}$		0.1			0.1		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{ V}$		20			20		μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{ V}$		-0.4			-0.4		mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-6	-40		-5	-42		mA
I_{CCH} Supply current, all outputs high	$V_{CC} = \text{MAX}, V_I = 0\text{ V}$		2.9	6		2.9	6	mA
			8.6	16		8.6	16	
I_{CCL} Supply current, all outputs low	$V_{CC} = \text{MAX}, V_I = 4.5\text{ V}$		4.1	7		4.1	7	mA
			12	21		12	21	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

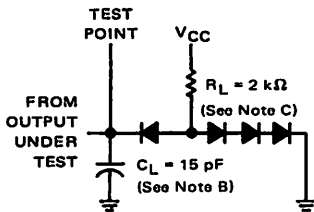
‡All typical values are at $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

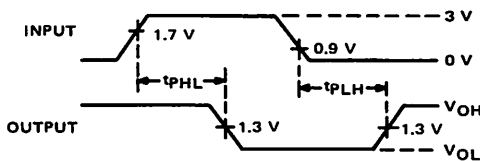
switching characteristics, $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	'LS13			'LS14			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15\text{ pF}, R_L = 2\text{ k}\Omega$	15	22		15	22		ns
t_{PHL} Propagation delay time, high-to-low-level output		18	27		15	22		ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



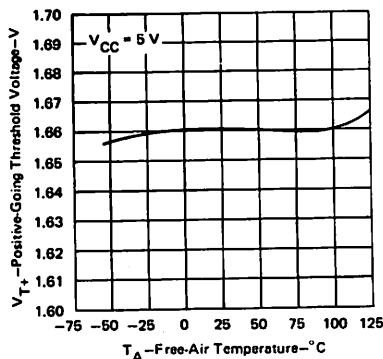
VOLTAGE WAVEFORMS

- NOTES: A. The input waveform is supplied by a generator with the following characteristics:
 $Z_{out} = 50\text{ }\Omega$ and $PRR \leq 1\text{ MHz}$, $t_r \leq 15\text{ ns}$, $t_f \leq 6\text{ ns}$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.

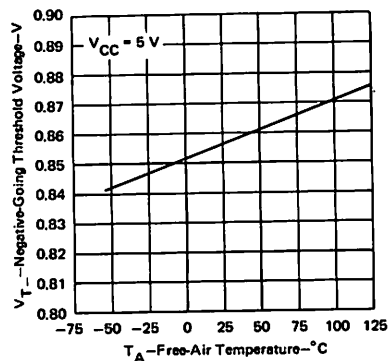
TYPES SN54LS13, SN54LS14, SN74LS13, SN74LS14 SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

TYPICAL CHARACTERISTICS†

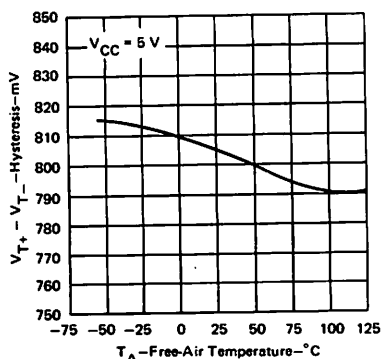
POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



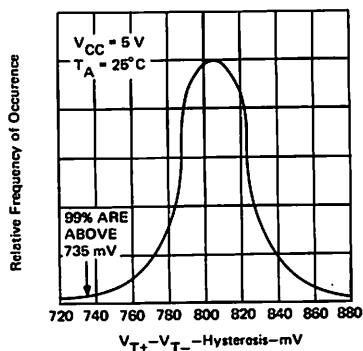
NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



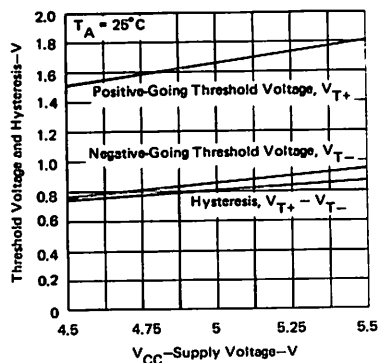
HYSTERESIS
vs
FREE-AIR TEMPERATURE



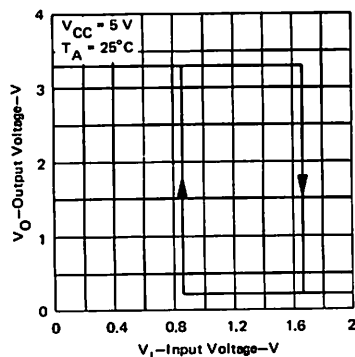
DISTRIBUTION OF UNITS
FOR HYSTERESIS



THRESHOLD VOLTAGES AND HYSTERESIS
vs
SUPPLY VOLTAGE



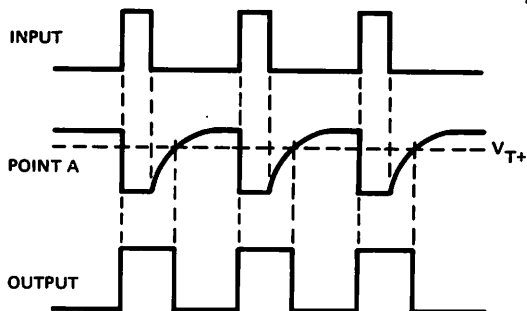
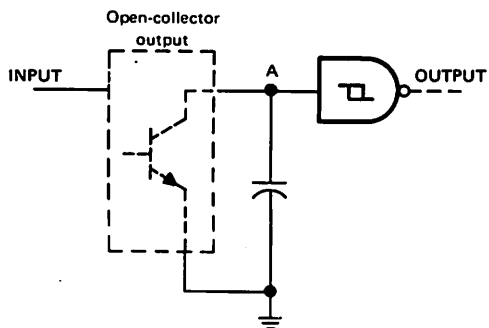
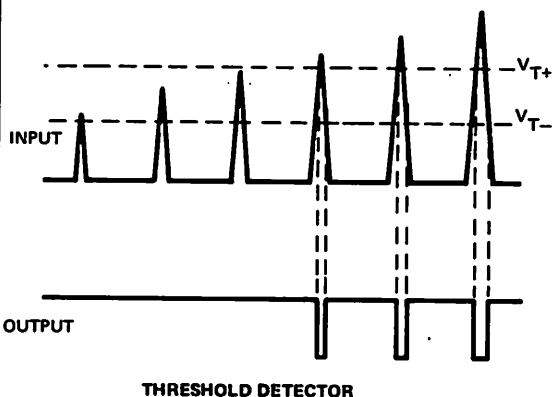
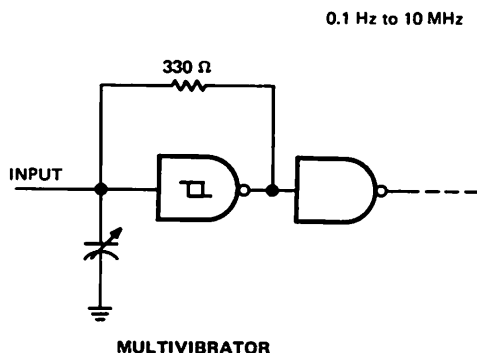
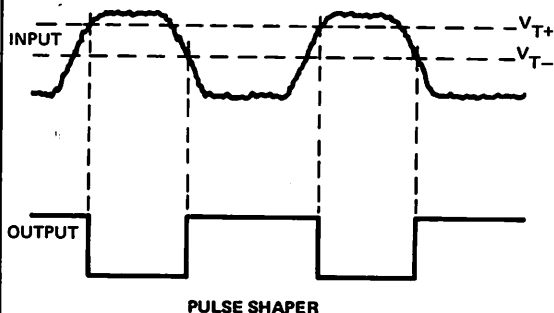
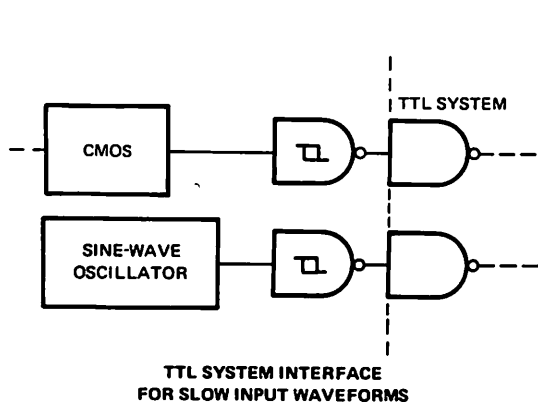
OUTPUT VOLTAGE
vs
INPUT VOLTAGE



† Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 are applicable for SN54LS13, SN54LS14, and SN54LS132 only.

TYPES SN54LS13, SN54LS14, SN74LS13, SN74LS14 SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

TYPICAL APPLICATION DATA



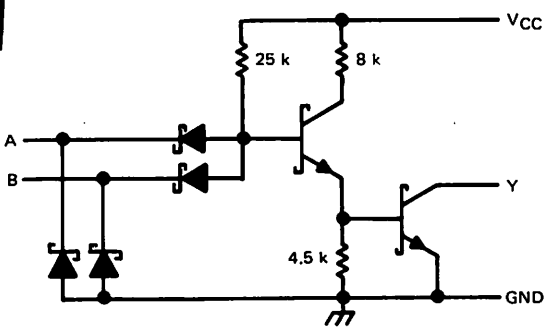
TYPES SN54LS26, SN74LS26

QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

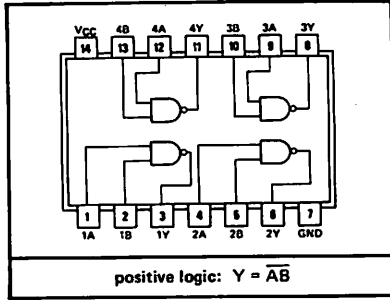
BULLETIN NO. DL S 7412084, MARCH 1974

- Functionally and Mechanically Identical to SN5426/SN7426

schematic (each gate)



SN54LS26 ... J OR W PACKAGE
SN74LS26 ... J OR N PACKAGE
(TOP VIEW)



Resistor values shown are nominal and in ohms.

recommended operating conditions

	SN54LS26			SN74LS26			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			15			15	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS26			SN74LS26			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage				0.7			0.8		V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5		V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IL} = V_{IL \text{ max}}$	$V_{OH} = 12 \text{ V}$		50			50		μA
		$V_{OH} = 15 \text{ V}$		1			1		mA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
		$I_{OL} = 8 \text{ mA}$				0.35	0.5		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20		μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.36			-0.36		mA
I_{CCH} Supply current, outputs high	$V_{CC} = \text{MAX}, \text{All inputs at } 0 \text{ V}$		0.8	1.6		0.8	1.6		mA
I_{CCL} Supply current, outputs low	$V_{CC} = \text{MAX}, \text{All inputs at } 4.5 \text{ V}$		2.4	4.4		2.4	4.4		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$		17	32	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Note 2		15	28	ns

NOTE 2: Load circuit and voltage waveforms are shown on page S-88.

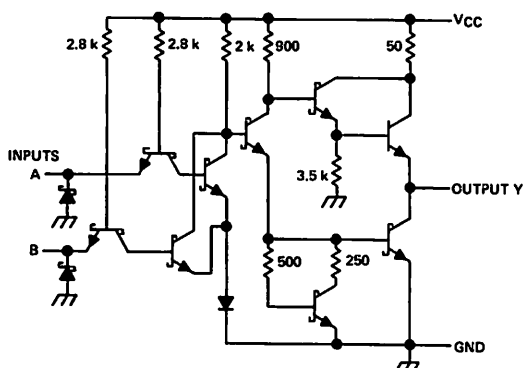
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TEXAS INSTRUMENTS
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TYPES SN54S32, SN74S32
QUADRUPLE 2-INPUT POSITIVE-OR GATES

BULLETIN NO. DL-S 7412079, MARCH 1974

schematic (each gate)

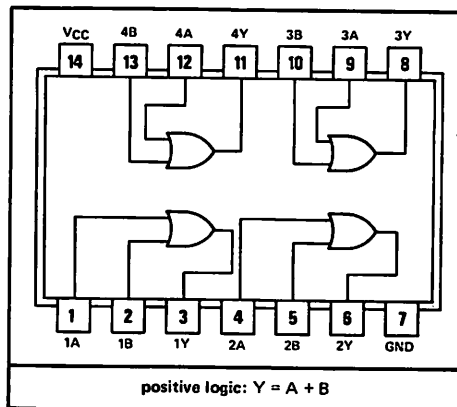


Resistor values shown are nominal and in ohms.

SN54S32 ... J OR W PACKAGE

SN74S32 ... J OR N PACKAGE

(TOP VIEW)

positive logic: $Y = A + B$

recommended operating conditions

	SN54S32			SN74S32			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OH} = -1 \text{ mA}$	SN54S32 2.5	SN74S32 3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 20 \text{ mA}$			0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			50	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.5 \text{ V}$			-2	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	mA
I_{CCH} Supply current, all outputs high	$V_{CC} = \text{MAX}$		18	32	mA
I_{CCL} Supply current, all outputs low	$V_{CC} = \text{MAX}$		38	68	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$R_L = 280 \Omega$, See Note 2	$C_L = 15 \text{ pF}$	4	7	ns
		$C_L = 50 \text{ pF}$	5		
t_{PHL} Propagation delay time, high-to-low-level output		$C_L = 15 \text{ pF}$	4	7	ns
		$C_L = 50 \text{ pF}$	5.5		

NOTES: 1. All voltage values are with respect to network ground terminal.

2. Load circuit and voltage waveforms are shown on page S-87.

TENTATIVE DATA SHEET

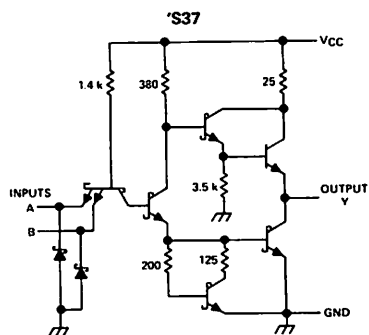
PRINTED IN U.S.A.

TYPES SN54S37, SN54S38, SN74S37, SN74S38
QUADRUPL 2-INPUT POSITIVE-NAND GATES

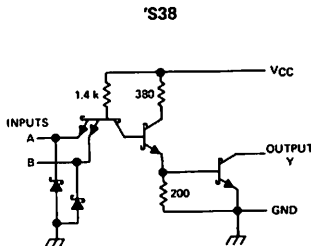
BULLETIN NO. DL-S 7412081, MARCH 1974

- 'S37 has active pullups
- 'S38 has open-collector outputs

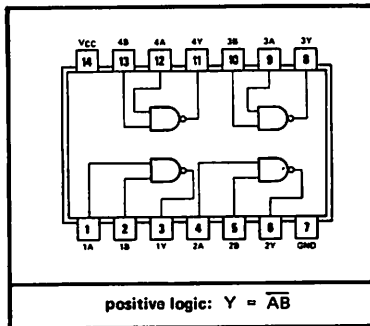
schematics (each gate)



Resistor values shown are nominal and in ohms.

SN54S37, SN54S38 ... J OR W PACKAGE
SN74S37, SN74S38 ... J OR N PACKAGE

(TOP VIEW)



recommended operating conditions

	SN54S37			SN54S38			SN74S37			SN74S38			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}						5.5						5.5	V
High-level output current, I_{OH}			-3						-3				mA
Low-level output current, I_{OL}			60			60			60			60	mA
Operating free-air temperature	-55		125	-55		125	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'S37			'S38			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -3 \text{ mA}$	2.5	3.4					V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$						250	μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 60 \text{ mA}$			0.5			0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			100			100	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-4			-4	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$			-50			-225	mA
I_{CCH} Supply current, all outputs high	$V_{CC} = \text{MAX}$			20			36	mA
I_{CCL} Supply current, all outputs low	$V_{CC} = \text{MAX}$			46			80	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	'S37			'S38			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	$R_L = 93 \Omega$, See Note 2	$C_L = 15 \text{ pF}$	4	6.5	6.5	10		ns
		$C_L = 50 \text{ pF}$	6		9			
t_{PHL} Propagation delay time, high-to-low-level output		$C_L = 15 \text{ pF}$	4	6.5	6.5	10		ns
		$C_L = 50 \text{ pF}$	6		8.5			

NOTES: 1. All voltage values are with respect to network ground terminal.

2. Load circuit and voltage waveforms are shown on page S-87.

TENTATIVE DATA SHEET

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This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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S-55

TTL
SSI

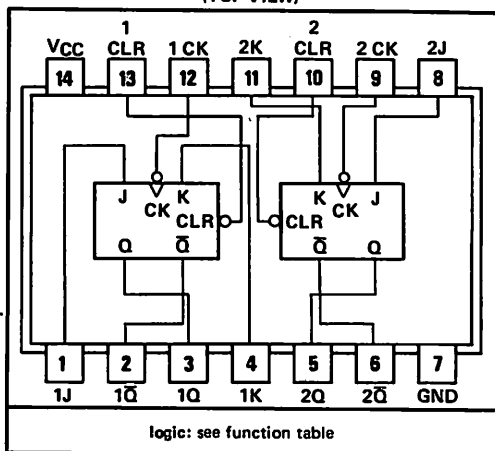
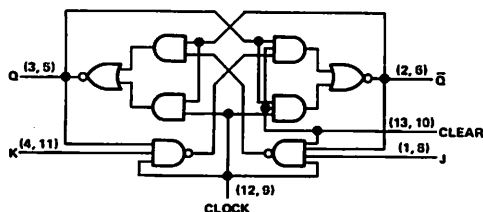
TYPES SN54LS107, SN74LS107 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS

BULLETIN NO. DLS 7412096, MARCH 1974

- Functionally and Mechanically Equivalent to SN54107/SN74107 Master-Slave Flip-Flops

SN54LS107 ... J OR W PACKAGE
SN74LS107 ... J OR N PACKAGE
(TOP VIEW)

functional block diagram (each flip-flop)



description

These monolithic edge-triggered dual J-K flip-flops feature individual J, K, clock, and clear inputs to each flip-flop. A low logic level at the clear input resets the Q output to a low level regardless of the levels at the other inputs. With clear inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table, as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	↓	L	L	Q_0	\bar{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	TOGGLE
H	H	X	X	Q_0	\bar{Q}_0

H = high level (steady state)

L = low level (steady state)

X = irrelevant

↓ = transition from high to low level

Q_0 = the level of Q before the indicated input conditions were established

TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

recommended operating conditions

		SN54LS107			SN74LS107			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Pulse width, t_w	Clock high	20		20				ns
	Clear low	25		25				
Setup time, t_{setup}		20	↓		20	↓		ns
Hold time, t_{hold}		0	↓		0	↓		ns
Operating free-air temperature, T_A		-55		125	0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54LS107, SN74LS107

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS107			SN74LS107			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage			0.7			0.8		V
V _I	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA		-1.5			-1.5		V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I _{OL} = 8 mA					0.35	0.5	
I _I	Input current at maximum input voltage	J or K		0.1			0.1		mA
		Clear		0.3			0.3		
		Clock		0.4			0.4		
I _{IH}	High-level input current	J or K		20			20		µA
		Clear		60			60		
		Clock		80			80		
I _{IL}	Low-level input current	J or K		-0.36			-0.36		mA
		Clear		-0.8			-0.8		
		Clock		-0.72			-0.72		
I _{OS}	Short-circuit output current§	V _{CC} = MAX	-6	-40		-5	-42		mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 2		4	8		4	8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

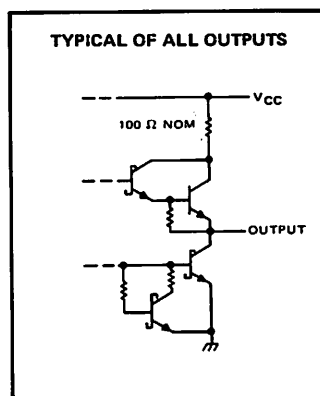
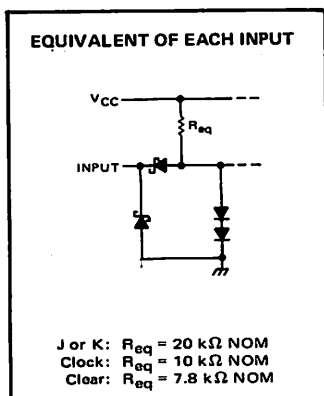
NOTE 2: I_{CC} is measured with outputs open, first with all inputs grounded, and second with J and clear at 4.5 V, K grounded, and clock at a momentary 4.5 V then grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}	Maximum clock frequency	30	45		MHz
t _{PLH}	Propagation delay time, low-to-high-level output from clear or clock		11	20	ns
t _{PHL}	Propagation delay time, high-to-low-level output from clear or clock		15	30	ns

NOTE 3: Load circuit and voltage waveforms are shown on page S-88.

schematics of inputs and outputs



TYPES SN54LS122, SN54LS123, SN74LS122, SN74LS123

SINGLE AND DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

BULLETIN NO. DLS 7412113, MARCH 1974

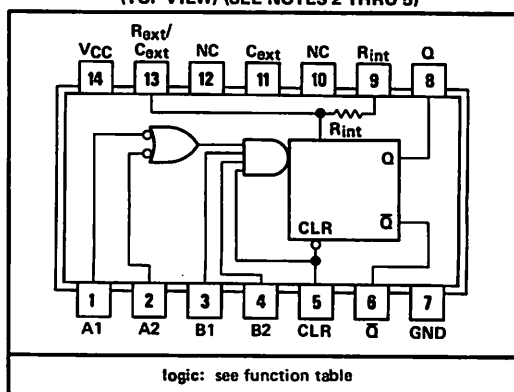
- Functionally and Mechanically Identical to SN54122/SN74122 and SN54123/SN74123
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Low Power Dissipation:
'LS122 ... 30 mW Typical
'LS123 ... 60 mW Typical
- Compensated for V_{CC} and Temperature Variations
- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- 'LS122 Has Internal 10-k Ω Timing Resistor
- Diode-Clamped Inputs
- Compatible for Use with TTL or DTL

'LS122 FUNCTION TABLE
(SEE NOTE 1)

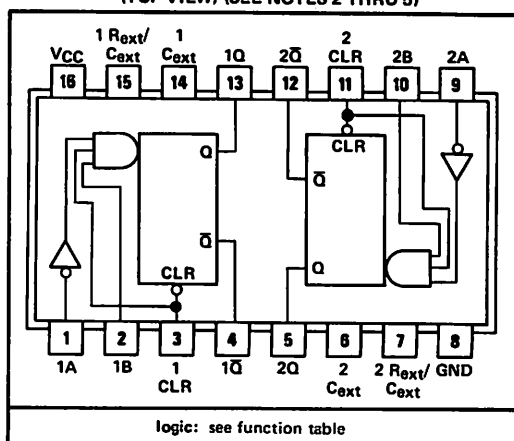
CLEAR	INPUTS				OUTPUTS	
	A1	A2	B1	B2	Q	\bar{Q}
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	\uparrow	H	\downarrow	\uparrow
H	L	X	H	\uparrow	\downarrow	\uparrow
H	X	L	H	H	L	H
H	X	L	\uparrow	H	\downarrow	\uparrow
H	X	L	H	\uparrow	\downarrow	\uparrow
H	H	\downarrow	H	H	\downarrow	\uparrow
H	\downarrow	\downarrow	H	H	\downarrow	\uparrow
H	\downarrow	X	H	H	\downarrow	\uparrow
\uparrow	L	X	H	H	\downarrow	\uparrow
\uparrow	X	L	H	H	\downarrow	\uparrow

'LS123 FUNCTION TABLE
(SEE NOTE 1)

CLEAR	INPUTS		OUTPUTS	
	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	\uparrow	\downarrow	\uparrow
H	\downarrow	\uparrow	\downarrow	\uparrow
\uparrow	L	H	\downarrow	\uparrow

SN54LS122 ... J OR W PACKAGE
SN74LS122 ... J OR N PACKAGE
(TOP VIEW) (SEE NOTES 2 THRU 5)

NC—No internal connection.

SN54LS123 ... J OR W PACKAGE
SN74LS123 ... J OR N PACKAGE
(TOP VIEW) (SEE NOTES 2 THRU 5)

description

The 'LS122 and 'LS123 multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C. Enough Schmitt hysteresis is provided to ensure jitter-free triggering from the B inputs with transition rates as slow as 1 volt per second. Figure 1 illustrates triggering the one-shot with the high-level-active (B) inputs.

- NOTES: 1. H = high level (steady state), L = low level (steady state), \uparrow = transition from low to high level, \downarrow = transition from high to low level, \uparrow = one high-level pulse, \downarrow = one low-level pulse, X = irrelevant (any input, including transitions).
2. To use the internal timing resistor of 'LS122, connect R_{int} to V_{CC} .
3. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
4. For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open circuited.
5. To obtain variable pulse widths, connect external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC} .

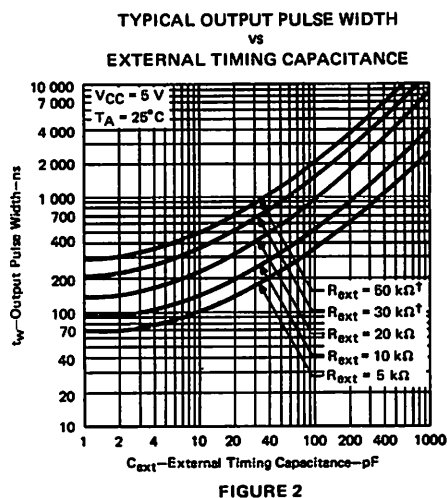
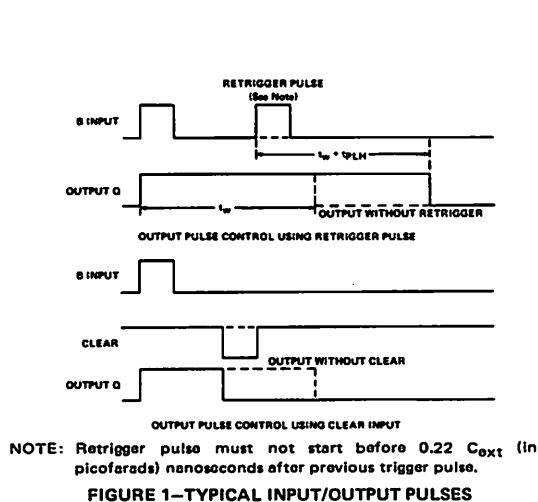
TENTATIVE DATA SHEET

S-58

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TEXAS INSTRUMENTS
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TYPES SN54LS122, SN54LS123, SN74LS122, SN74LS123 SINGLE AND DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR



† These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54LS' circuits.

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. The 'LS122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as:

$$t_w = 0.4 \cdot R_T \cdot C_{ext}$$

where

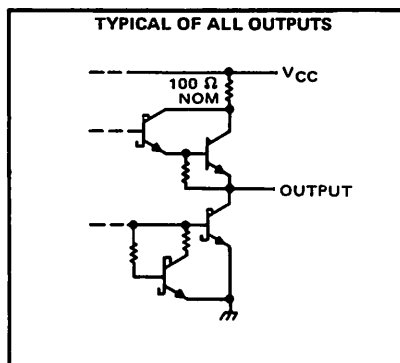
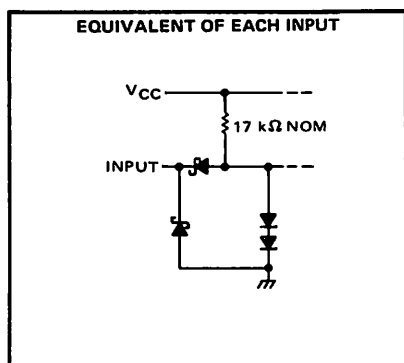
R_T is in $k\Omega$ (either internal or external timing resistor),

C_{ext} is in pF,

t_w is in ns.

For pulse widths when $C_{ext} \leq 1000$ pF, see Figure 2.

schematics of inputs and outputs



TYPES SN54LS122, SN54LS123, SN74LS122, SN74LS123
SINGLE AND DUAL RETRIGGERABLE
MONOSTABLE MULTIVIBRATORS WITH CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS122, SN54LS123	-55°C to 125°C
SN74LS122, SN74LS123	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS122 SN54LS123			SN74LS122 SN74LS123			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	6.5	4.75	5	5.25	V
High-level output current, I_{OH}		-400			-400			μA
Low-level output current, I_{OL}		4			8			mA
Pulse width, t_w	A or B inputs high	40			40			ns
	A or B inputs low	40			40			
	Clear low	40			40			
External timing resistance, R_{ext}		5 225			5 360			k Ω
External capacitance, C_{ext}		No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal		50			50			pF
Operating free-air temperature, T_A		-55 125			0 70			$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS122 SN54LS123			SN74LS122 SN74LS123			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage		0.7			0.8			V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5			-1.5			V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	0.25		0.4	0.25		0.4	V
				$I_{OL} = 8 \text{ mA}$			0.35	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$	0.1			0.1			mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	20			20			μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-0.4			-0.4			mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-15	-100		-15	-100		mA
I_{CC} Supply current (quiescent or triggered)	$V_{CC} = \text{MAX},$ See Note 2	6		11	6		11	mA
		'LS122			'LS122			
		12		20	12		20	
		'LS123			'LS123			

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

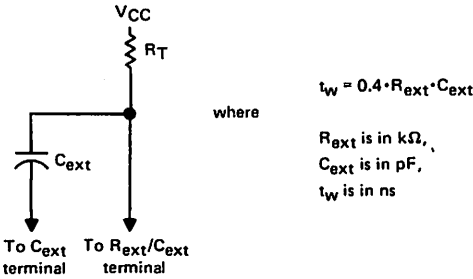
TYPES SN54LS122, SN54LS123, SN74LS122, SN74LS123
SINGLE AND DUAL RETRIGGERABLE
MONOSTABLE MULTIVIBRATORS WITH CLEAR

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	A	Q	Cext = 0, Rext = 5 kΩ, CL = 15 pF, RL = 2 kΩ	22	33	ns	
	B			29	44		
tPHL	A	Q̄		30	45	ns	
	B			37	56		
tPHL	Clear	Q		18	27	ns	
tPLH		Q̄		30	45		
tWQ (min)		A or B		Q	45		68
tWQ	A or B	Q	Cext = 1000 pF, Rext = 10 kΩ, CL = 15 pF, RL = 2 kΩ	3.08	3.42	3.76	μs

[†] t_{PLH} \equiv propagation delay time, low-to-high-level output
 t_{PHL} \equiv propagation delay time, high-to-low-level output
 t_{wQ} \equiv width of pulse at output Q

TYPICAL APPLICATION DATA



TIMING COMPONENT CONNECTIONS

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BULLETIN NO. DL-S 7412025, MARCH 1974

- SN54LS124, SN54S124 . . . J OR W PACKAGE**
SN74LS124, SN74S124 . . . J OR N PACKAGE
(TOP VIEW)



374

TYPES SN54LS124, SN74LS124

DUAL VOLTAGE-CONTROLLED OSCILLATORS

recommended operating conditions

	SN54LS124			SN74LS124			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
Input voltage at frequency control or range input, $V_{I(freq)}$ or $V_{I(rng)}$	0		5	0		5	V
High-level output current, I_{OH}			-1.2			-1.2	mA
Low-level output current, I_{OL}			12			24	mA
Output frequency (enabled), f_o	1			1			Hz
		35			35		MHz
Operating free-air temperature, T_A	-55	125		0	70		°C

NOTE 1: Throughout this data sheet, the symbol V_{CC} is used for the voltage applied to both pins 15 and 16.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS124			SN74LS124			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage at enable					2			2			V
V_{IL}	Low-level input voltage at enable							0.7			0.8	V
V_I	Input clamp voltage at enable		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$					-1.5			-1.5	V
V_{OH}	High-level output voltage		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -1.2 \text{ mA}$			2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OL} = 12 \text{ mA}$				0.25	0.4		0.25	0.4	V
			$I_{OL} = 20 \text{ mA}$							0.35	0.5	
I_I	Input current	Freq control or range	$V_{CC} = \text{MAX}$	$V_I = 5 \text{ V}$			50	250		50	250	µA
				$V_I = 1 \text{ V}$			10	50		10	50	
I_I	Input current at maximum input voltage	Enable	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$					0.1			0.1	mA
I_{IH}	High-level input current	Enable	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$					20			20	µA
I_{IL}	Low-level input current	Enable	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$					-0.4			-0.4	mA
I_{OS}	Short-circuit output current§		$V_{CC} = \text{MAX}$			-30		-100	-25		-110	mA
I_{CC}	Supply current, total into pins 15 and 16		$V_{CC} = \text{MAX},$ See Note 2				22	37		22	37	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the outputs disabled and open.

switching characteristics, $V_{CC} = 5 \text{ V}, R_L = 667 \Omega, C_L = 45 \text{ pF}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_o	Output frequency	$C_{ext} = 2 \text{ pF}$	$V_{I(freq)} = 4 \text{ V}, V_{I(rng)} = 1 \text{ V}$	35	50		MHz
			$V_{I(freq)} = 1 \text{ V}, V_{I(rng)} = 5 \text{ V}$	11	20		
	Output duty cycle	$C_{ext} = 8.3 \text{ pF to } 500 \text{ µF}$			50%		
t_{PHL}	Propagation delay time, high-to-low-level output from enable	$f_o > 1 \text{ Hz}$			30+*		ns

*The delay will typically be 30 ns plus up to one half the period of one cycle (i.e. 30 ns to $30 \text{ ns} + \frac{5 \times 10^8}{f_o(\text{Hz})} \text{ ns}$) depending upon the timing of the enable pulse with respect to the signal generated by the internal oscillator.

TENTATIVE DATA

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TEXAS INSTRUMENTS
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TYPES SN54S124, SN74S124
DUAL VOLTAGE-CONTROLLED OSCILLATORS

recommended operating conditions

	SN54S124			SN74S124			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
Input voltage at frequency control or range input, $V_{I(freq)}$ or $V_{I(rng)}$	1		5	1		5	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Output frequency (enabled), f_o	1			1			Hz
		60			60		MHz
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Throughout this data sheet, the symbol V_{CC} is used for the voltage applied to both pins 15 and 16.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage at enable			2			V
V_{IL}	Low-level input voltage at enable					0.8	V
V_I	Input clamp voltage at enable	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -1 \text{ mA}$	SN54S'	2.5	3.4		V
			SN74S'	2.7	3.4		
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$				0.5	V
I_I	Input current	Freq control or range	$V_{CC} = \text{MAX}$			10	μA
			$V_I = 5 \text{ V}$			50	
I_I	Input current at maximum input voltage	Enable	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	Enable	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50	μA
I_{IL}	Low-level input current	Enable	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2	mA
I_{OS}	Short-circuit output current§		$V_{CC} = \text{MAX}$	-40		-100	mA
I_{CC}	Supply current, total into pins 15 and 16		$V_{CC} = \text{MAX}, \text{ See Note 2}$			105	mA
			$V_{CC} = \text{MAX}, T_A = 125^\circ\text{C}, \text{ See Note 2}$			110	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the outputs disabled and open.

switching characteristics, $V_{CC} = 5 \text{ V}, R_L = 280 \Omega, C_L = 15 \text{ pF}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f _O	Output frequency	C _{ext} = 2 pF	V _I (freq) = 4 V, V _I (rng) = 1 V	60	85		MHz
			V _I (freq) = 1 V, V _I (rng) = 5 V	25	40		
Output duty cycle		C _{ext} = 8.3 pF to 500 μF			50%		
t _{PHL}	Propagation delay time, high-to-low-level output from enable	f _O = 1 Hz to 20 MHz			1.4		s
		f _O > 20 MHz			f _O (Hz)		
					70		ns

TYPES SN54LS124, SN54S124, SN74LS124, SN74S124 DUAL VOLTAGE-CONTROLLED OSCILLATORS

TYPICAL APPLICATION DATA

free-running oscillator

Free-running oscillators can be implemented for most systems by setting the output frequency of the VCO with either a capacitor or a crystal. If excitation is provided with a capacitor the frequency control and/or range inputs can be used to vary the output frequency.

If excited with a crystal, low-frequency response (≤ 1 MHz) can be improved if a relatively small capacitor (5 to 15 pF) is paralleled with the crystal. When operated at the fundamental frequency of a crystal, the frequency control input should be low (≈ 1 V) and the range input should be high (4 V to 5 V) for maximum stability over temperature and supply voltage variations.

phase-locked loops

A basic crystal-controlled phase-locked loop is illustrated in Figure A. This application can be used for implementation of:

- A highly stable fixed-frequency clock generator.
- A highly stable fixed- or variable-frequency synthesizer.
- A highly efficient "slave-clock" system for synchronizing off-card, remote, or data-interfacing clock systems

With fixed division rates for both M and N, the output frequency (f_o) will be stable at $f_o = \frac{N}{M} f_1$. Obviously, either M or N, or both, could be programmable counters in which case the output frequency (f_o) will be a variable frequency dependent on the instantaneous value of $\frac{N}{M} f_1$.

The crystal-controlled VCO can be operated up to 60 MHz with an accuracy that is dependent on the crystal. At the higher frequencies, response of the phase comparator can become a limiting factor and one of the following approaches may be necessary to extend the operating frequency range.

- Frequencies $\frac{f_1}{M}$ and $\frac{f_o}{N}$ can be divided equally by the same constant (K) also shown in Figure A. The constant can be any value greater than unity ($K > 1$), and should be selected to yield frequency ranges that can be handled adequately by the phase-comparator and filter. The output frequency (f_o) retains the same relationship as previously explained because now:

$$f_o = \frac{KN}{KM} f_1 = \frac{N}{M} f_1$$

- In another method, the comparison of $\frac{f_1}{M}$ and $\frac{f_o}{N}$ can be performed with either an SN54LS85/SN74LS85 or SN54S85/SN74S85. The resultant $A > B$ and $A < B$ outputs from the 'LS85 or 'S85 permit the detector to be simplified to a charge-pump circuit. See Figure B.

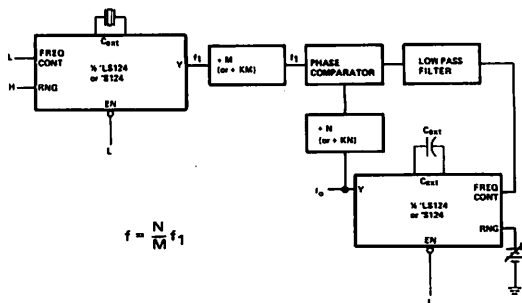


FIGURE A—PHASE-LOCKED LOOP

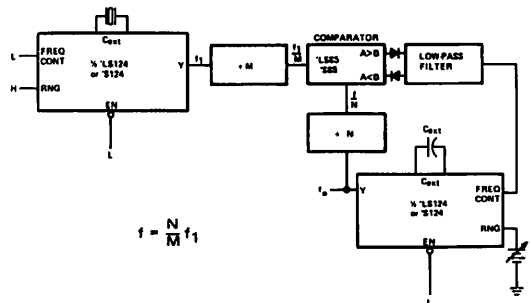


FIGURE B—HIGH-FREQUENCY PHASE-LOCKED LOOP

TYPES SN54S124, SN74S124
DUAL VOLTAGE-CONTROLLED OSCILLATORS

TYPICAL CHARACTERISTICS ('S124 only)

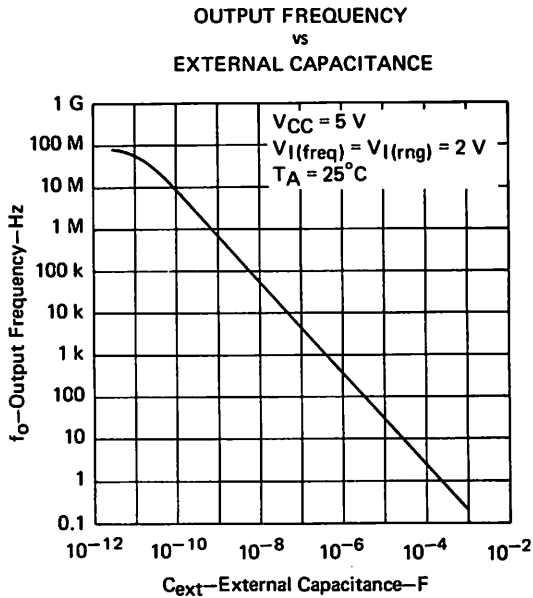


FIGURE 1

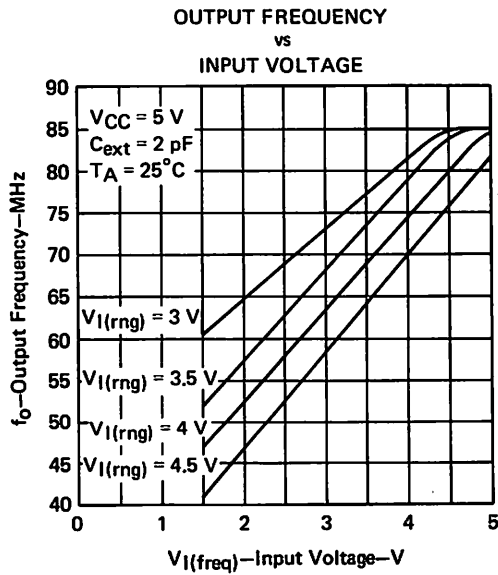


FIGURE 2

TYPES SN54LS132, SN74LS132
SCHMITT-TRIGGER POSITIVE-NAND GATES
WITH TOTEM-POLE OUTPUTS
BULLETIN NO. DL-S 7412112, MARCH 1974

- Operation from Very Slow Transitions
- Temperature-Compensated Threshold Levels
- Temperature-Compensated Hysteresis, Typically 0.8 V
- High Noise Immunity

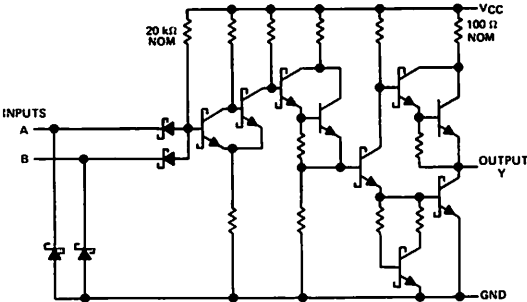
description

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The hysteresis or backlash, which is the difference between the two threshold levels, is typically 800 millivolts.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

For typical characteristics and typical application data, see the SN54LS13/SN74LS13 data sheet, page S-49.

schematic (each gate)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS132	-55°C to 125°C
SN74LS132	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS132			SN74LS132			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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TYPES SN54LS132, SN74LS132

SCHMITT-TRIGGER POSITIVE-NAND GATES

WITH TOTEM-POLE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS132			SN74LS132			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage	$V_{CC} = 5\text{ V}$			$V_{CC} = 5\text{ V}$			V
V_{T-}	Negative-going threshold voltage	$V_{CC} = 5\text{ V}$			$V_{CC} = 5\text{ V}$			V
$V_{T+} - V_{T-}$	Hysteresis	$V_{CC} = 5\text{ V}$			$V_{CC} = 5\text{ V}$			V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18\text{ mA}$			$V_{CC} = \text{MIN}, I_I = -18\text{ mA}$			V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, I_{OH} = -400\text{ }\mu\text{A}, V_I = 0.6\text{ V}$			$V_{CC} = \text{MIN}, I_{OH} = -400\text{ }\mu\text{A}, V_I = 0.6\text{ V}$			V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, I_{OL} = 4\text{ mA}$			$V_{CC} = \text{MIN}, I_{OL} = 4\text{ mA}$			V
		$V_I = 2\text{ V}, I_{OL} = 8\text{ mA}$			$V_I = 2\text{ V}, I_{OL} = 8\text{ mA}$			
I_{T+}	Input current at positive-going threshold	$V_{CC} = 5\text{ V}, V_I = V_{T+}$			$V_{CC} = 5\text{ V}, V_I = V_{T+}$			mA
I_{T-}	Input current at negative-going threshold	$V_{CC} = 5\text{ V}, V_I = V_{T-}$			$V_{CC} = 5\text{ V}, V_I = V_{T-}$			mA
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7\text{ V}$			$V_{CC} = \text{MAX}, V_I = 7\text{ V}$			mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{ V}$			$V_{CC} = \text{MAX}, V_I = 2.7\text{ V}$			μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{ V}$			$V_{CC} = \text{MAX}, V_I = 0.4\text{ V}$			mA
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$			$V_{CC} = \text{MAX}$			mA
I_{CCH}	Supply current, all outputs high	$V_{CC} = \text{MAX}, V_I = 0\text{ V}$			$V_{CC} = \text{MAX}, V_I = 0\text{ V}$			mA
I_{CCL}	Supply current, all outputs low	$V_{CC} = \text{MAX}, V_I = 4.5\text{ V}$			$V_{CC} = \text{MAX}, V_I = 4.5\text{ V}$			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

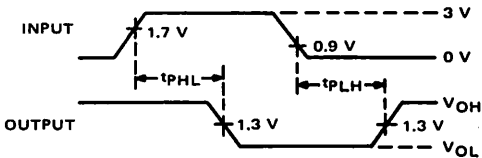
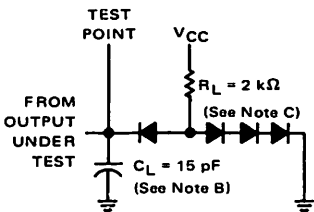
‡ All typical values are at $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output		15	22	ns

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- The input waveform is supplied by a generator with the following characteristics:
 $Z_{out} = 50\text{ }\Omega$ and $PRR \leq 1\text{ MHz}$, $t_r \leq 15\text{ ns}$, $t_f \leq 6\text{ ns}$.
 - C_L includes probe and jig capacitance.
 - All diodes are 1N916 or 1N3064.

- SN54221, SN54LS221 . . . J OR W PACKAGE
SN74221, SN74LS221 . . . J OR N PACKAGE
(TOP VIEW)



TYPE	TYPICAL POWER DISSIPATION	MAXIMUM OUTPUT PULSE LENGTH
SN54221	130 mW	21 s
SN74221	130 mW	28 s
SN54LS221	23 mW	49 s
SN74LS221	23 mW	70 s

description

The '221 and 'LS221 are monolithic dual multivibrators with performance characteristics virtually identical to those of the '121. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.





Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the above table by choosing appropriate timing components. With $R_{ext} = 2\text{ k}\Omega$ and $C_{ext} = 0$, an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.



Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μ F) and more than one decade of timing resistance (2 k Ω to 30 k Ω for the SN54221, 2 k Ω to 40 k Ω for the SN74221, 2 k Ω to 70 k Ω for the SN54LS221, and 2 k Ω to 100 k Ω for the SN74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_{w(out)} = C_{ext}R_{ext} \ln 2 \approx 0.7 C_{ext}R_{ext}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μ F and timing resistance as low as 1.4 k Ω may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is

**FUNCTION TABLE
(EACH MONOSTABLE)**

INPUTS			OUTPUTS	
CLEAR	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		

Also see description and switching characteristics

Also see description and switching characteristics

H = high level (steady state)  = one high-level pulse
L = low level (steady state)  = one low-level pulse
↑ = transition from low to high level X = irrelevant
↓ = transition from high to low level

TYPES SN54221, SN54LS221, SN74221, SN74LS221

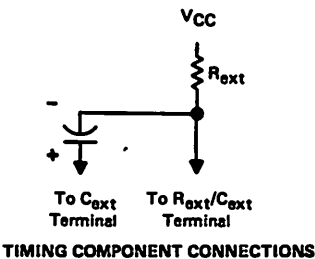
DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

description (continued)

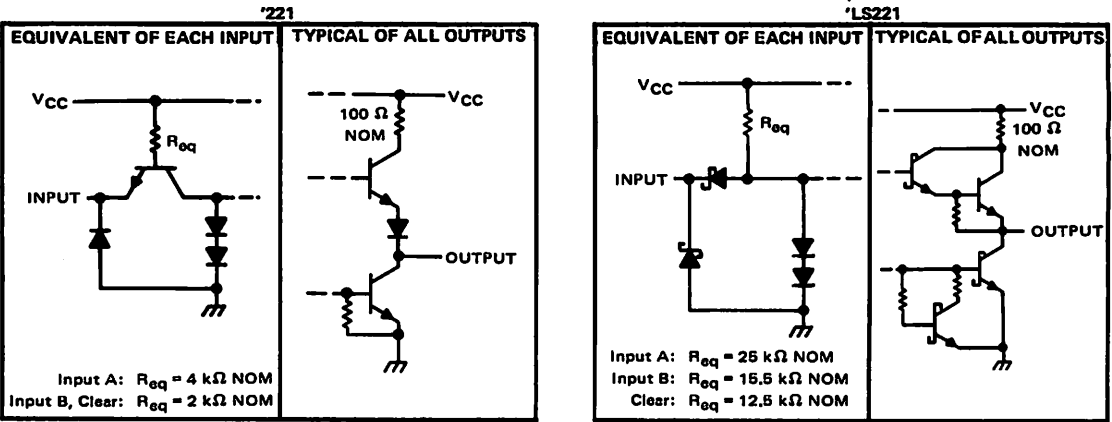
held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T . Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

The variance in output pulse width from device to device is typically less than $\pm 0.5\%$ for given external timing components. An example of this distribution for the '221 is shown in Figure 2. Variations in output pulse width versus supply voltage and temperature for the '221 are shown in Figure 3 and 4, respectively.

Pin assignments for these devices are identical to those of the SN54123/SN74123 or SN54LS123/SN74LS123 so that the '221 or 'LS221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext} .



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: SN54221, SN74221	5.5 V
SN54LS221, SN74LS221	7 V
Operating free-air temperature range: SN54221, SN54LS221	-55°C to 125°C
SN74221, SN74LS221	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

TYPES SN54221, SN74221

DUAL MONOSTABLE MULTIVIBRATORS

WITH SCHMITT-TRIGGER INPUTS

recommended operating conditions

		SN54221			SN74221			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-800			-800			μ A
Low-level output current, I_{OL}		16			16			mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input, B	1			1			V/s
	Logic input, A	1			1			V/ μ s
Input pulse width	A or B, $t_{w(in)}$	50			50			ns
	Clear, $t_{w(clear)}$	20			20			ns
Clear-inactive-state setup time, t_{setup}		15			15			ns
External timing resistance, R_{ext}		1.4			1.4			k Ω
External timing capacitance, C_{ext}		0			0			1000 μ F
Output duty cycle	$R_{ext} = 2$ k Ω	67			67			%
	$R_{ext} = \text{MAX } R_{ext}$	90			90			%
Operating free-air temperature, T_A		-55			125			0 70 $^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{T+} Positive-going threshold voltage at A input	$V_{CC} = \text{MIN}$		1.4	2	V
V_{T-} Negative-going threshold voltage at A input	$V_{CC} = \text{MIN}$	0.8	1.4		V
V_{T+} Positive-going threshold voltage at B input	$V_{CC} = \text{MIN}$		1.55	2	V
V_{T-} Negative-going threshold voltage at B input	$V_{CC} = \text{MIN}$	0.8	1.35		V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12$ mA			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -800$ μ A	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 16$ mA		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5$ V			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4$ V	Input A		40	μ A
		Input B, Clear		80	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4$ V	Input A		-1.6	mA
		Input B, Clear		-3.2	
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	SN54221	-20	-55	mA
		SN74221	-18	-55	
I_{CC} Supply current	$V_{CC} = \text{MAX}$	Quiescent	26	50	mA
		Triggered	46	80	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5$ V, $T_A = 25^{\circ}$ C.

[§]Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^{\circ}$ C

PARAMETER [¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	$C_L = 15$ pF, $R_L = 400$ Ω , See Figure 1 and Note 2	$C_{ext} = 80$ pF, $R_{ext} = 2$ k Ω		45	70	ns
	B	Q				35	55	
t_{PHL}	A	\bar{Q}				50	80	ns
	B	\bar{Q}				40	65	
t_{PHL}	Clear	Q					27	ns
t_{PLH}	Clear	\bar{Q}					40	ns
$t_{w(out)}$	A or B	Q or \bar{Q}		$C_{ext} = 80$ pF, $R_{ext} = 2$ k Ω	70	110	150	ns
				$C_{ext} = 0$, $R_{ext} = 2$ k Ω	20	30	50	
				$C_{ext} = 100$ pF, $R_{ext} = 10$ k Ω	650	700	750	ms
				$C_{ext} = 1$ μ F, $R_{ext} = 10$ k Ω	6.5	7	7.5	

[¶] t_{PLH} \equiv Propagation delay time, low-to-high-level output

t_{PHL} \equiv Propagation delay time, high-to-low-level output

$t_{w(out)}$ \equiv Output pulse width

NOTE 2: Load circuit is shown on page S-87.

TYPES SN54LS221, SN74LS221
DUAL MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS

recommended operating conditions

		SN54LS221			SN74LS221			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-400			-400			μ A
Low-level output current, I_{OL}		4			8			mA
Rate of rise or fall of input pulse, dv/dt	Schmitt, B	1			1			V/ μ s
	Logic input, A	1			1			V/ μ s
Input pulse width	A or B, $t_{w(in)}$	40			40			ns
	Clear, $t_{w(clear)}$	40			40			ns
Clear-inactive-state setup time, t_{setup}		15			15			ns
External timing resistance, R_{ext}		1.4			1.4			k Ω
External timing capacitance, C_{ext}		0			0			μ F
Output duty cycle	$R_T = 2\text{ k}\Omega$	67			67			%
	$R_T = \text{MAX } R_{ext}$	90			90			%
Operating free-air temperature, T_A		-55			0			$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS221		SN74LS221		UNIT			
			MIN	TYP‡	MAX	MIN		TYP‡	MAX	
V _{T+}	Positive-going threshold voltage at A input	V _{CC} = MIN	1.0		2	1.0		2	V	
V _{T−}	Negative-going threshold voltage at A input	V _{CC} = MIN	0.7	1.0		0.8	1.0		V	
V _{T+}	Positive-going threshold voltage at B input	V _{CC} = MIN	1.0		2	1.0		2	V	
V _{T−}	Negative-going threshold voltage at B input	V _{CC} = MIN	0.7	0.9		0.8	0.9		V	
V _I	Input clamp voltage	V _{CC} = MIN, I _I = −18 mA	−1.5			−1.5			V	
V _{OH}	High-level output voltage	V _{CC} = MIN, I _{OH} = −400 μA	2.5	3.5		2.7	3.5		V	
V _{OL}	Low-level output voltage	V _{CC} = MIN	I _{OL} = 4 mA	0.25		0.4	0.25		0.4	V
			I _{OL} = 8 mA			0.35		0.5		
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V	0.1			0.1			mA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V	20			20			μA	
I _{IL}	Low-level input current	Input A	−0.36			−0.36			mA	
		Input B	−0.44			−0.44				
		Clear	−0.54			−0.54				
I _{OS}	Short-circuit output current‡	V _{CC} = MAX	−15	−100		−15	−100		mA	
I _{CC}	Supply current	V _{CC} = MAX	Quiescent	4.7		11	4.7		11	mA
			Triggered	19		27	19		27	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

TENTATIVE DATA

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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TYPES SN54LS221, SN74LS221

DUAL MONOSTABLE MULTIVIBRATORS

WITH SCHMITT-TRIGGER INPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
tPLH	A	Q	CL = 15 pF, RL = 2 kΩ, See Figure 1 and Note 3	Cext = 80 pF, Rext = 2 kΩ	45	70	ns	
	B	Q			35	55		
tPHL	A	Q̄			50	80	ns	
	B	Q̄			40	65		
tPHL	Clear	Q			27	ns		
tPLH	Clear	Q̄			40	ns		
tw(out)	A or B	Q or Q̄		Cext = 80 pF, Rext = 2 kΩ	70	110	150	ns
				Cext = 0, Rext = 2 kΩ	20	30	50	
			Cext = 100 pF, Rext = 10 kΩ	650	700	750		
			Cext = 1 μF, Rext = 10 kΩ	6.5	7	7.5	ms	

[†] t_{PLH} \equiv Propagation delay time, low-to-high-level output
 t_{PHL} \equiv Propagation delay time, high-to-low-level output
 $t_{w(out)}$ \equiv Output pulse width

NOTE 3: Load circuit is shown on page S-88.

TENTATIVE DATA

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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TYPES SN54221, SN54LS221, SN74221, SN74LS221 **DUAL MONOSTABLE MULTIVIBRATORS** **WITH SCHMITT-TRIGGER INPUTS**

PARAMETER MEASUREMENT INFORMATION

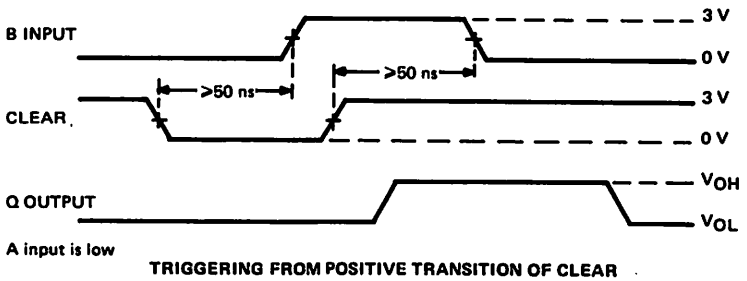
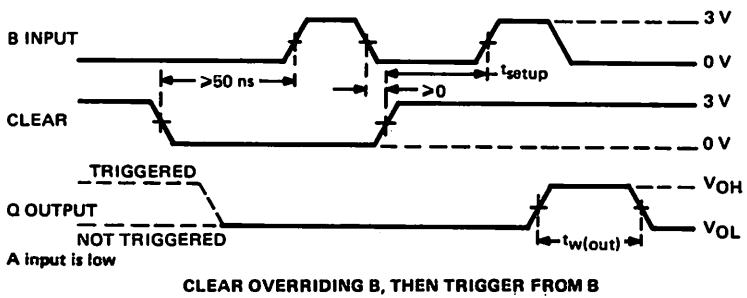
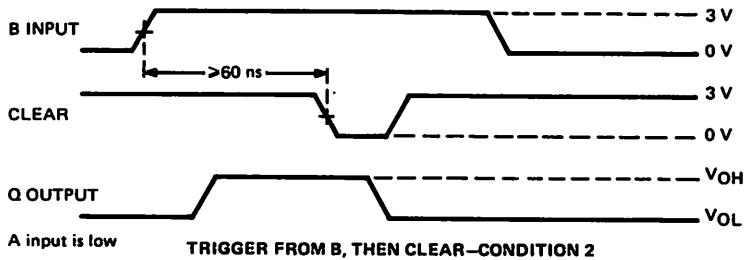
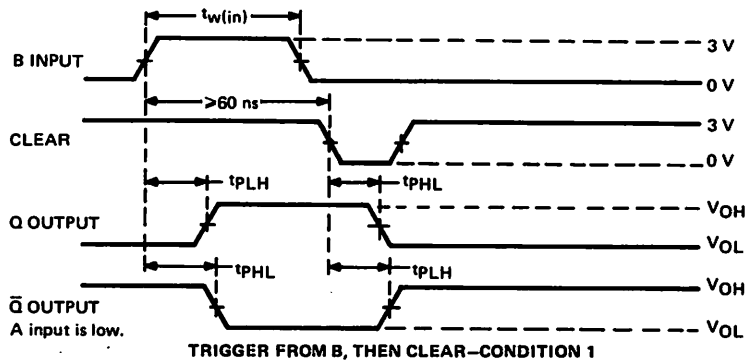
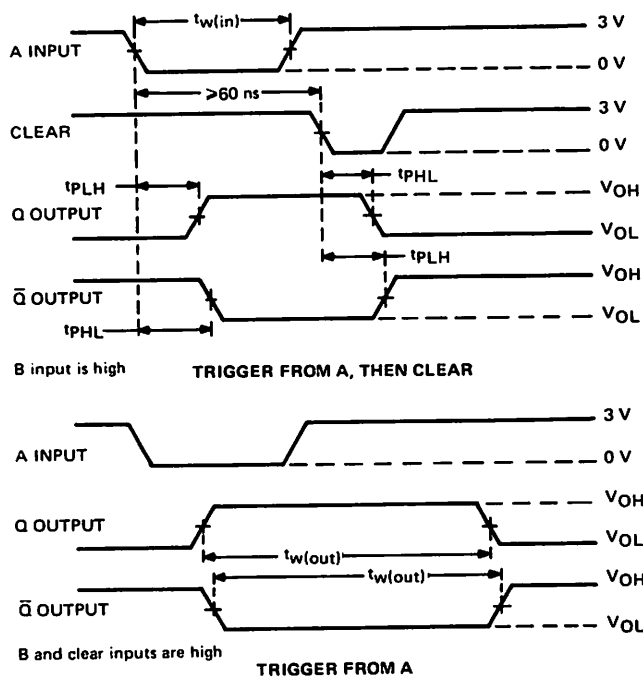


FIGURE 1—SWITCHING CHARACTERISTICS

TYPES SN54221, SN54LS221, SN74221, SN74LS221 **DUAL MONOSTABLE MULTIVIBRATORS** **WITH SCHMITT-TRIGGER INPUTS**

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by generators having the following characteristics: $PRR < 1\text{ MHz}$, $Z_{out} \approx 50\ \Omega$; for '221, $t_r < 7\text{ ns}$, $t_f < 7\text{ ns}$, for 'LS221, $t_r < 15\text{ ns}$, $t_f < 6\text{ ns}$.
 B. All measurements are made between the 1.5 V points of the indicated transitions for the '221 or between the 1.3 V points for the 'LS221.

FIGURE 1—SWITCHING CHARACTERISTICS (CONTINUED)

TYPES SN54221, SN74221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

TYPICAL CHARACTERISTICS ('221 ONLY)[†]

DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

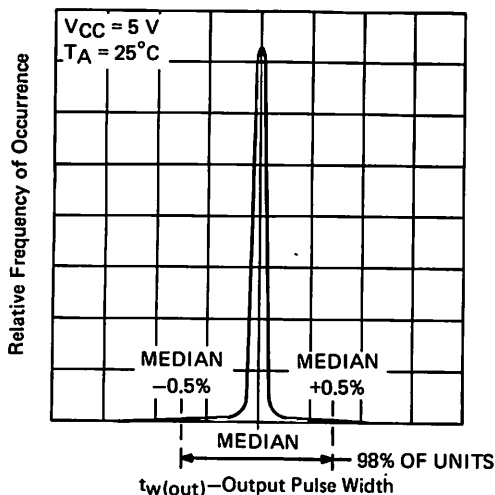


FIGURE 2

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

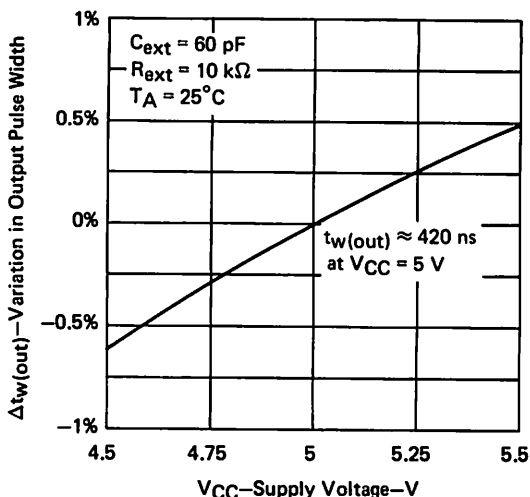


FIGURE 3

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE

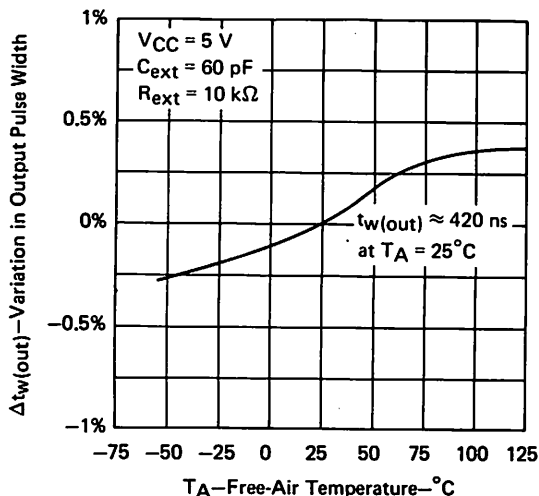


FIGURE 4

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

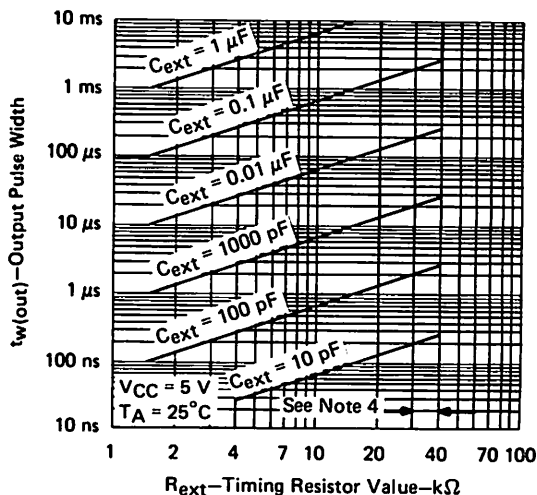


FIGURE 5

NOTE 4: These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54221.

[†]Data for temperatures below 0°C and above 70°C, and for supply voltages below 4.75 V and above 5.25 V are applicable for the SN54221 only.

TYPES SN54265, SN74265 **QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS**

BULLETIN NO. DLS 7412077, MARCH 1974

FOR SYMMETRICAL GENERATION OF COMPLEMENTARY TTL SIGNALS

- Switching Time Skew of the Complementary Outputs Is Typically 0.5 ns . . . Guaranteed to be No More than 3 ns at Rated Loading
- Full Fan-Out to 20 High-Level and 10 Low-Level 54/74 Loads
- Active Pull-Down Provides Square Transfer Characteristic

description

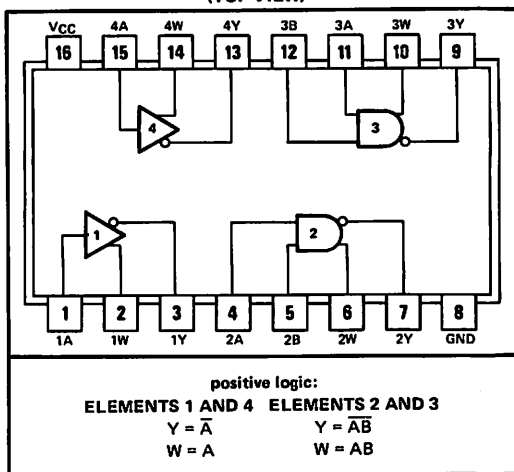
The SN54265 and SN74265 circuits feature complementary outputs from each logic element, which have virtually symmetrical switching time delays from the triggering input. They are designed specifically for use in applications such as:

- Symmetrical clock/clock generators
- Complementary input circuit for decoders and code converters
- Switch debouncing
- Differential line driver

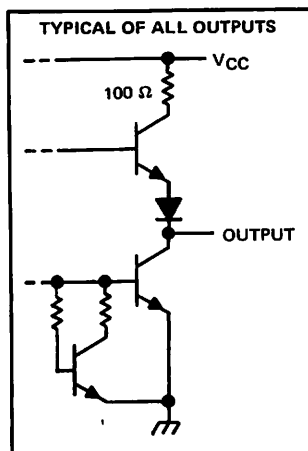
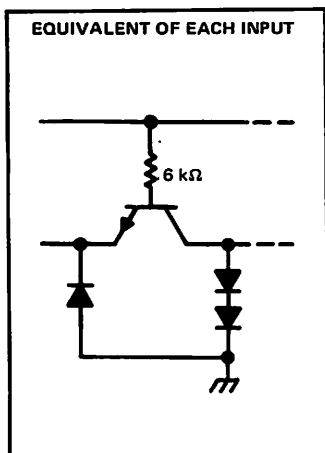
Examples of these four functions are illustrated in the typical application data.

The SN54265 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74265 is characterized for operation from 0°C to 70°C .

SN54265 . . . J OR W PACKAGE
SN74265 . . . J OR N PACKAGE
(TOP VIEW)



schematics of inputs and outputs



TYPES SN54265, SN74265
QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Table with 2 columns: Parameter and Value. Parameters include Supply voltage (VCC), Input voltage, Interemitter voltage, Operating free-air temperature range, and Storage temperature range.

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, the rating applies between inputs 2A and 2B and between inputs 3A and 3B.

recommended operating conditions

Table with 4 columns: Parameter, SN54265 (MIN, NOM, MAX), SN74265 (MIN, NOM, MAX), and UNIT. Parameters include Supply voltage, High-level output current, Low-level output current, and Operating free-air temperature.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Table with 5 columns: PARAMETER, TEST CONDITIONS, MIN, TYP, MAX, and UNIT. Parameters include input/output voltages, clamp voltage, output voltages, input/output currents, short-circuit output current, and supply current.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at VCC = 5 V, TA = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: ICC is measured with all outputs open and all inputs grounded.

switching characteristics, VCC = 5 V, TA = 25°C

Table with 6 columns: PARAMETER, FROM (INPUT), TO (OUTPUT), TEST CONDITIONS, MIN, TYP, MAX, and UNIT. Parameters include propagation delay times for low-to-high and high-to-low level outputs.

tPLH ≡ Propagation delay time, low-to-high-level output.
tPHL ≡ Propagation delay time, high-to-low-level output.
tPXX(W) - tPXX(Y) ≡ Difference in indicated propagation delay times at the W and Y outputs, respectively.
NOTE 4: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54265, SN74265

QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

TYPICAL CHARACTERISTICS†

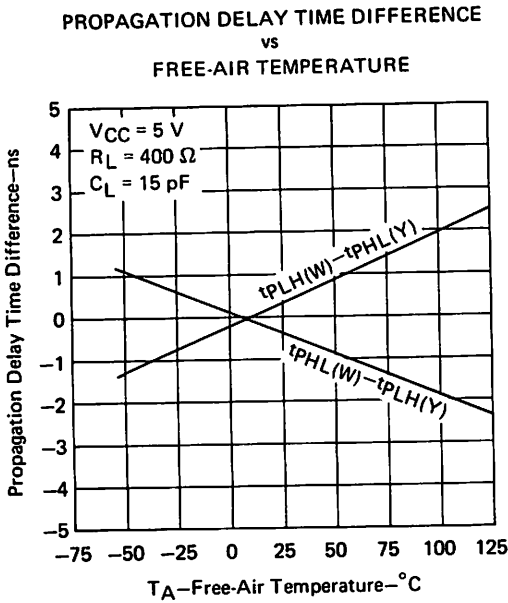


FIGURE 1

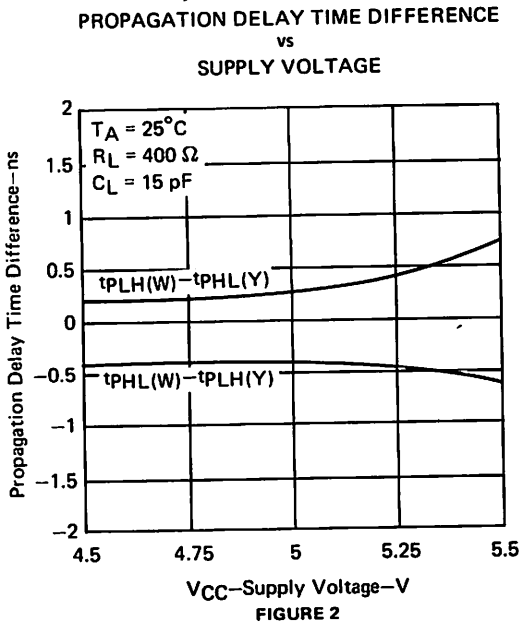


FIGURE 2

PROPAGATION DELAY TIME DIFFERENCE vs LOAD CAPACITANCE

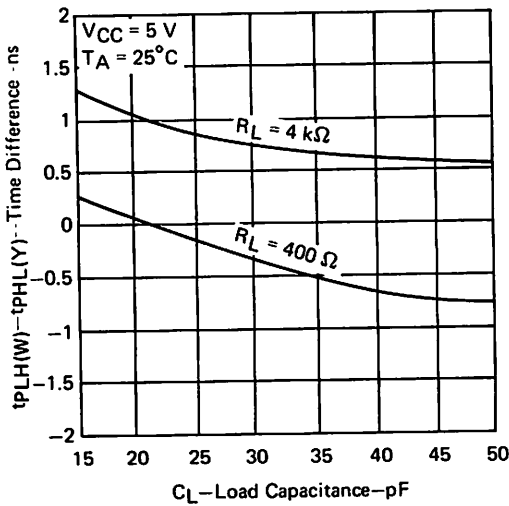


FIGURE 3

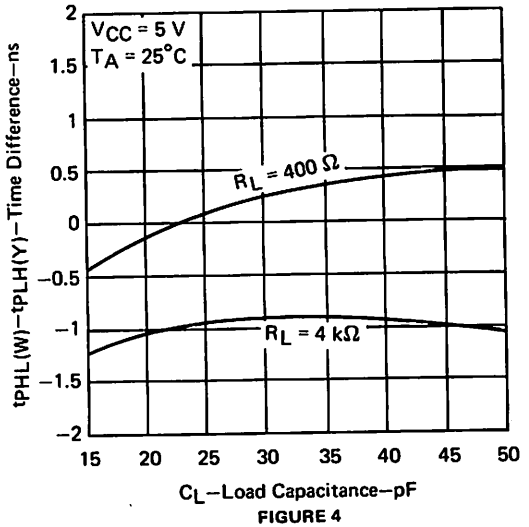


FIGURE 4

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable for SN54265 only.

TYPES SN54265, SN74265

QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

TYPICAL APPLICATION DATA

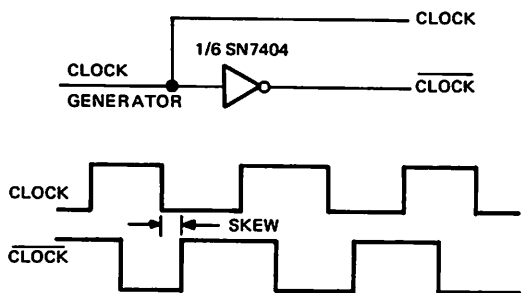


FIGURE A - TYPICAL CLOCK/ $\overline{\text{CLOCK}}$ GENERATOR CIRCUIT

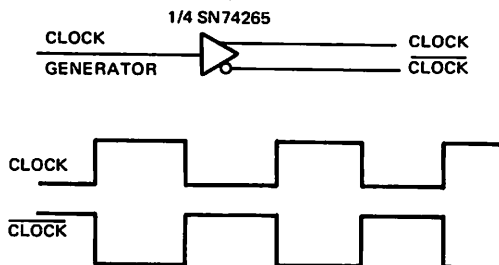


FIGURE B - SKEWLESS CLOCK/ $\overline{\text{CLOCK}}$ GENERATOR CIRCUIT

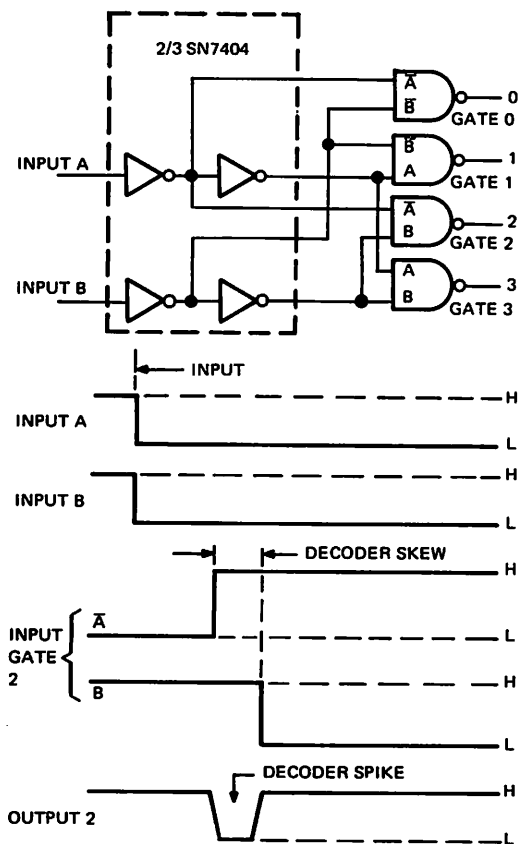


FIGURE C - TYPICAL DECODER/CODE CONVERTER

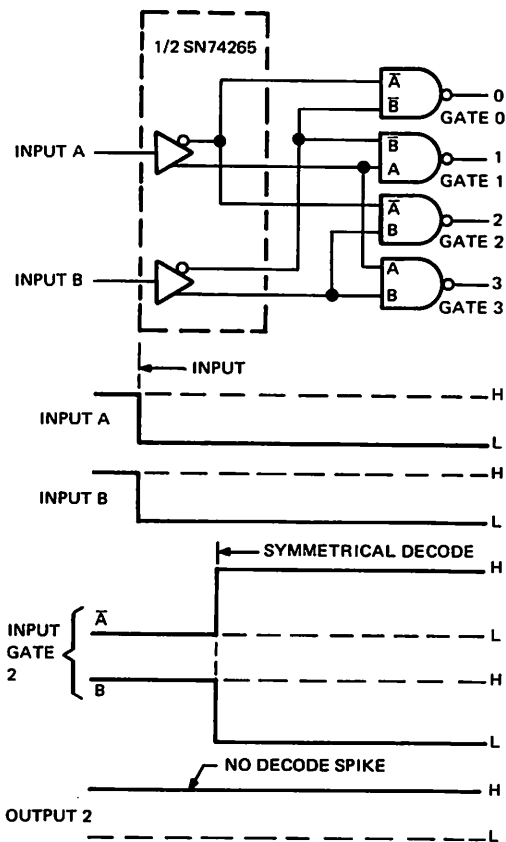


FIGURE D - SYMMETRICAL DECODER/CODE CONVERTER

TYPES SN54265, SN74265 QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

TYPICAL APPLICATION DATA

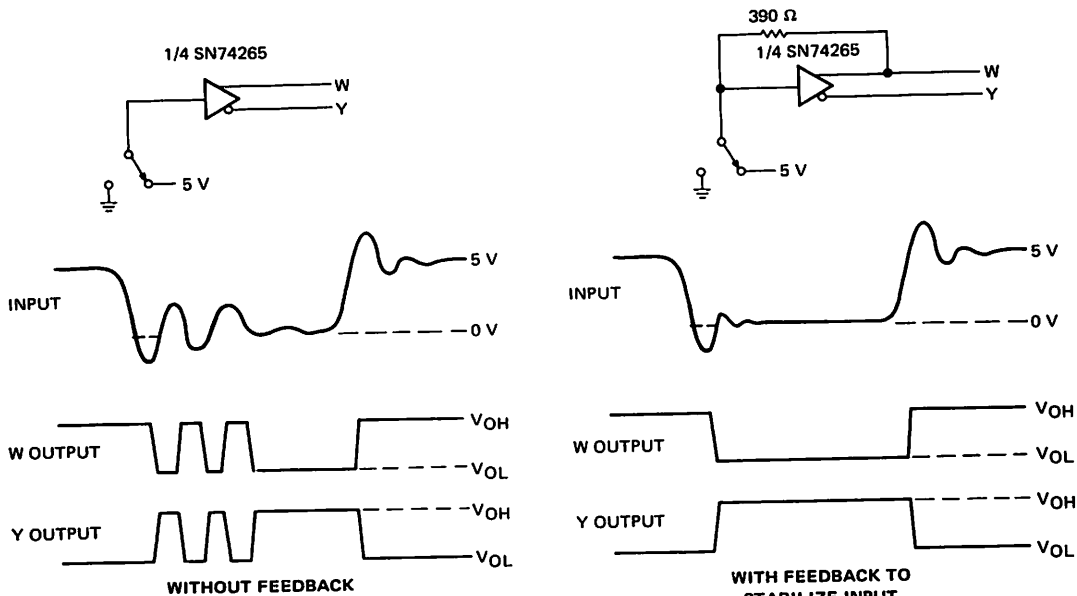


FIGURE E – SWITCH DEBOUNCER

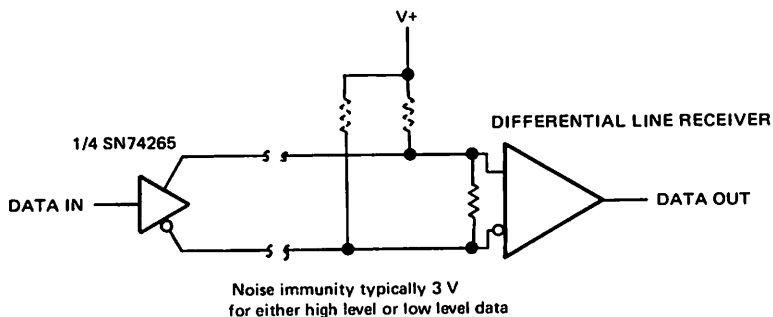


FIGURE F – DIFFERENTIAL LINE DRIVER

TTL
SSI

TYPES SN54LS279, SN74LS279 QUADRUPLE \bar{S} - \bar{R} LATCHES

BULLETIN NO. DL-S 7412086, MARCH 1974

- Functionally and Mechanically Identical to SN54279/SN74279
- Features Low Power Dissipation of 19 mW Typical

FUNCTION TABLE
(EACH LATCH)

INPUTS		OUTPUT
\bar{S}^\dagger	\bar{R}	Q
H	H	Q_0
L	H	H
H	L	L
L	L	H^*

H = high level

L = low level

Q_0 = the level of Q before the indicated input conditions were established.

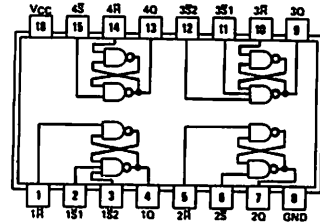
*This output level is pseudo stable: that is, it may not persist when the \bar{S} and \bar{R} inputs return to their inactive (high) level.

† For latches with double \bar{S} inputs:

H = both \bar{S} inputs high

L = one or both \bar{S} inputs low

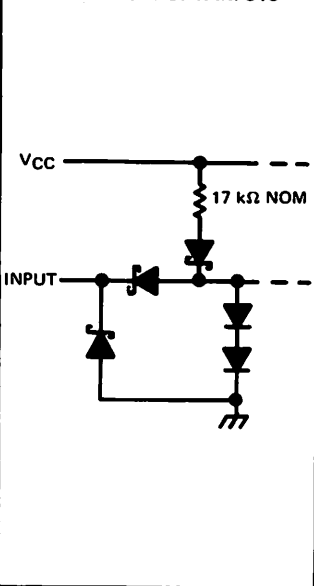
SN54SL279 ... J OR W PACKAGE
SN74LS279 ... J OR N PACKAGE
(TOP VIEW)



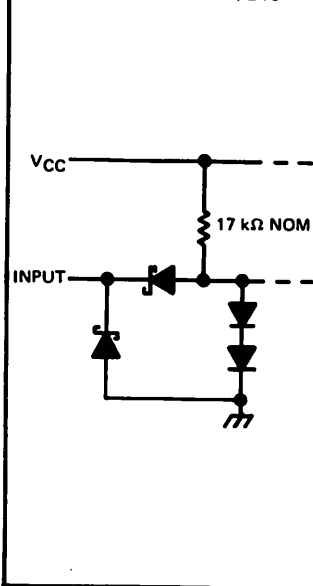
logic: see function table

schematics of inputs and outputs

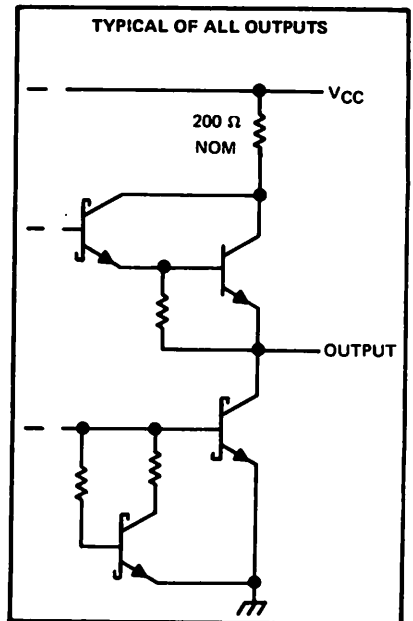
EQUIVALENT OF \bar{R} INPUTS



EQUIVALENT OF \bar{S} INPUTS



TYPICAL OF ALL OUTPUTS



TENTATIVE DATA SHEET

S-82 This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES SN54LS279, SN74LS279
QUADRUPLE \bar{S} - \bar{R} LATCHES

recommended operating conditions

	SN54LS279			SN74LS279			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS279			SN74LS279			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL} \text{ max}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL} \text{ max}$	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25 0.4	0.25 0.4 0.35 0.5			V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-6		-40	-5		-42	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		3.8	7		3.8	7	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all \bar{R} inputs grounded, all \bar{S} inputs at 4.5 V, and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output from \bar{S} input	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Note 3		12	22	ns
t_{PHL} Propagation delay time, high-to-low-level output from \bar{S} input			9	15	
t_{PHL} Propagation delay time, high-to-low-level output from \bar{R} input			15	27	

NOTE 3: Load circuit and voltage waveforms are shown on page S-88.

TYPES SN54365, SN54366, SN54367, SN54368, SN74365, SN74366, SN74367, SN74368 HEX BUS DRIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7412117, MARCH 1974

- Bus Buffers/Drivers with 3-State Outputs
- Can Be Used to Drive Bus Line Directly

'365

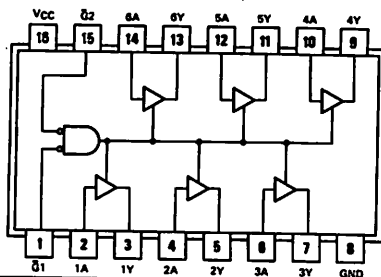
- True Data
- Gated Enable Inputs for X-Y Coincident Bus Control

'365
FUNCTION TABLE
(EACH DRIVER)

INPUTS				OUTPUT
\bar{G}_1	\bar{G}_2	A	Y	
H	X	X	Z	
X	H	X	Z	
L	L	H	H	
L	L	L	L	

H = high level, L = low level,
X = irrelevant, Z = high-impedance

SN54365 ... J OR W PACKAGE
SN74365 ... J OR N PACKAGE
(TOP VIEW)



'366

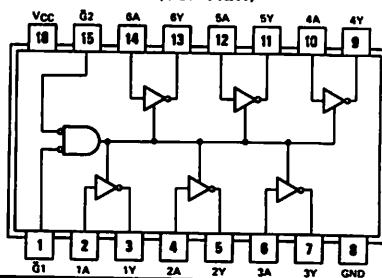
- Inverted Data
- Gated Enable Inputs for X-Y Coincident Bus Control

'366
FUNCTION TABLE
(EACH DRIVER)

INPUTS				OUTPUT
\bar{G}_1	\bar{G}_2	A	Y	
H	X	X	Z	
X	H	X	Z	
L	L	H	L	
L	L	L	H	

H = high level, L = low level,
X = irrelevant, Z = high-impedance

SN54366 ... J OR W PACKAGE
SN74366 ... J OR N PACKAGE
(TOP VIEW)



'367

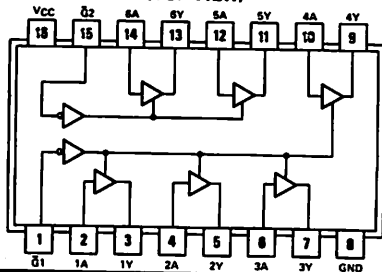
- True Data
- 4-Line and 2-Line Enable Inputs Can Be Organized for 4-Bit Bytes or Digit Control

'367
FUNCTION TABLE
(EACH DRIVER)

INPUTS			OUTPUT
\bar{G}	A	Y	
H	X	Z	
L	H	H	
L	L	L	

H = high level, L = low level,
X = irrelevant, Z = high-impedance

SN54367 ... J OR W PACKAGE
SN74367 ... J OR N PACKAGE
(TOP VIEW)



'368

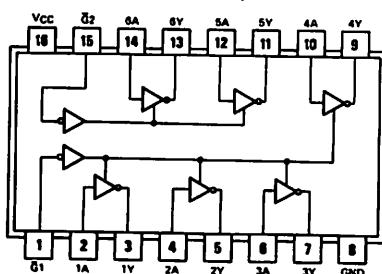
- Inverted Data
- 4-Line and 2-Line Enable Inputs Can Be Organized for 4-Bit Bytes or Digit Control

'368
FUNCTION TABLE
(EACH DRIVER)

INPUTS			OUTPUT
\bar{G}	A	Y	
H	X	Z	
L	H	L	
L	L	H	

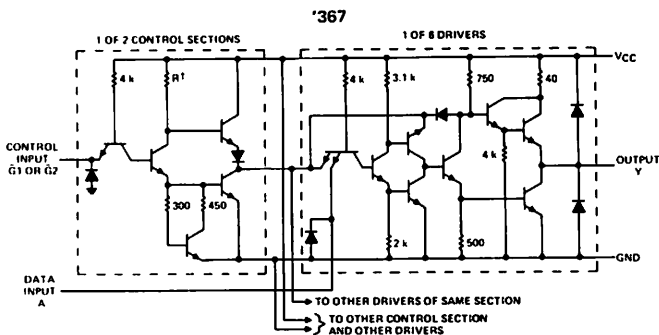
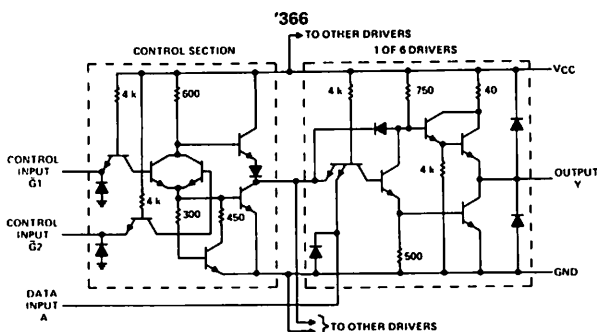
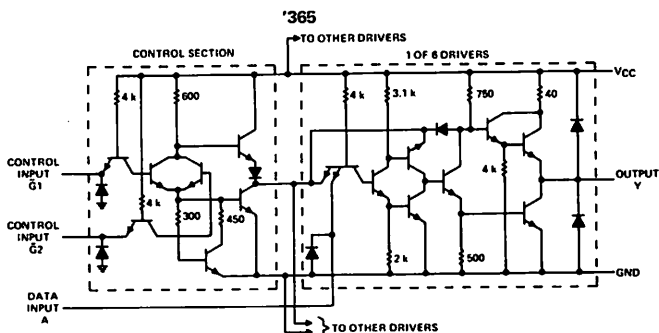
H = high level, L = low level,
X = irrelevant, Z = high-impedance

SN54368 ... J OR W PACKAGE
SN74368 ... J OR N PACKAGE
(TOP VIEW)

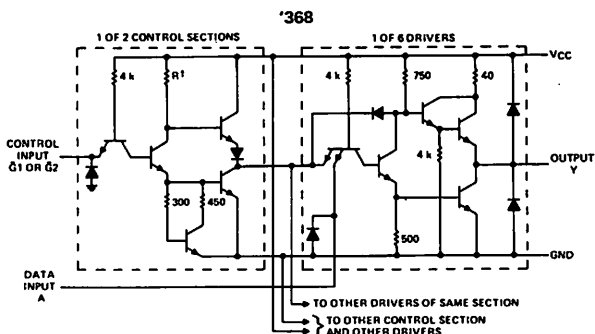


TYPES SN54365, SN54366, SN54367, SN54368, SN74365, SN74366, SN74367, SN74368 HEX BUS DRIVERS WITH 3-STATE OUTPUTS

schematics



[†] R is 900 Ω for the control section associated with \bar{G}_1 and 600 Ω for the control section associated with \bar{G}_2 .



[†] R is 900 Ω for the control section associated with \bar{G}_1 and 600 Ω for the control section associated with \bar{G}_2 .

Resistor values shown are nominal and in ohms.

TYPES SN54365, SN54366, SN54367, SN54368, SN74365, SN74366, SN74367, SN74368 HEX BUS DRIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

	SN54365, SN54366 SN54367, SN54368			SN74365, SN74366 SN74367, SN74368			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-2			-5.2	mA
Low-level output current, I_{OL}			32			32	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4	3.1		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 32 \text{ mA}$			0.4	V
V_O	Output clamp voltage	$V_{CC} = 0 \text{ V}, I_O = 12 \text{ mA}$			1.5	V
		$I_O = -12 \text{ mA}$			-1.5	
I_{OZH}	Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V},$ $V_O = 2.4 \text{ V}$			40	µA
I_{OZL}	Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V},$ $V_O = 0.4 \text{ V}$			-40	µA
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_{IH} = 2.4 \text{ V}$			40	µA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$ Both \bar{G} inputs at 2 V			-40	µA
		$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$ Both \bar{G} inputs at 0.4 V			-1.6	mA
		$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-130	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$			65	mA
					85	
					59	77

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

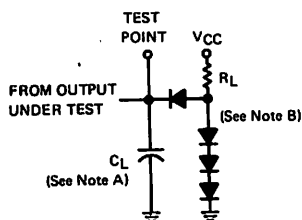
switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS°	'365, '367		'366, '368		UNIT
		MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output		16		17	ns
t_{PHL}	Propagation delay time, high-to-low-level output		22		16	ns
t_{ZH}	Output enable time to high level		35		35	ns
t_{ZL}	Output enable time to low level		37		37	ns
t_{HZ}	Output disable time from high level		11		11	ns
t_{LZ}	Output disable time from low level		27		27	ns

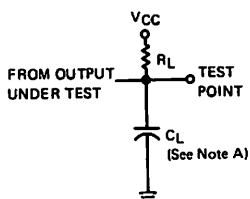
° Load circuit and voltage waveforms are shown on page S-87.

SERIES 54/74, 54H/74H, 54S/74S, AND SPECIFIED[†] SERIES 54L/74L DEVICES

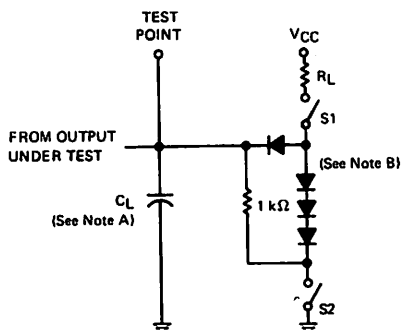
PARAMETER MEASUREMENT INFORMATION



**LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS**

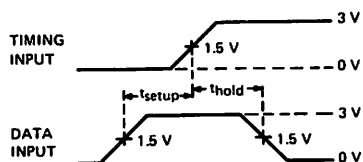


**LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS**

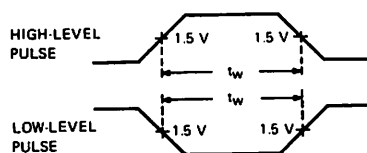


**LOAD CIRCUIT FOR
THREE-STATE OUTPUTS**

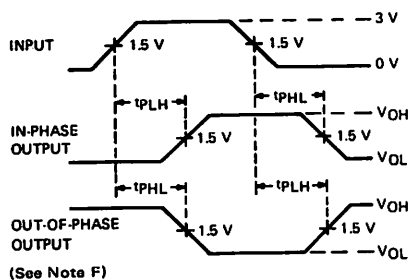
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.



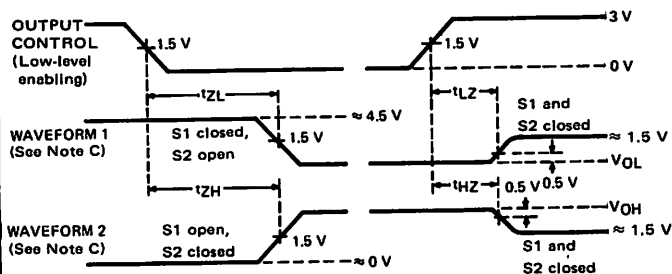
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE WIDTHS**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS**

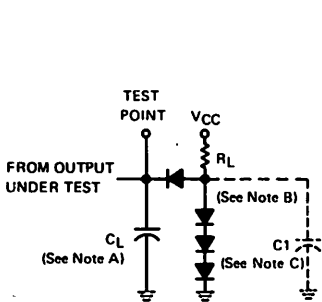
NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_{out} \approx 50 \Omega$ and:
For Series 54/74 and 54H/74H, $t_r \leq 7$ ns, $t_f \leq 7$ ns;
For Specified[†] Series 54L/74L devices: $t_r \leq 10$ ns, $t_f \leq 10$ ns;
For Series 54S/74S, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

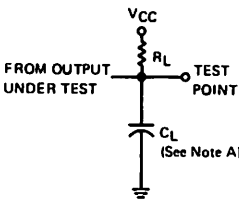
[†] 'L42, 'L43, 'L44, 'L46, 'L47, 'L75, 'L77, 'L96, 'L121, 'L122, 'L123, 'L153, 'L154, 'L167, 'L164

SERIES 54LS/74LS AND MOST† SERIES 54L/74L DEVICES

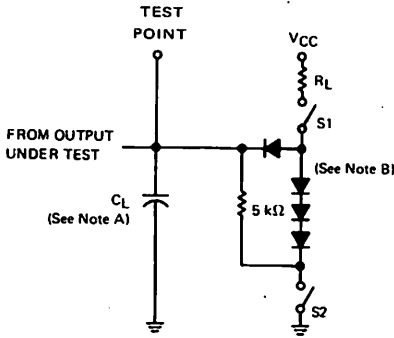
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS

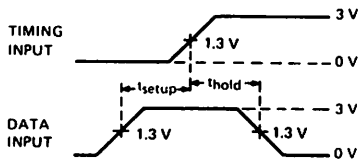


LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS

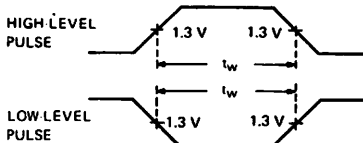


LOAD CIRCUIT FOR
THREE-STATE OUTPUTS

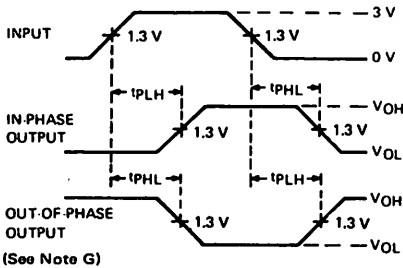
- NOTES
- A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N916 or 1N3064.
 - C. C_1 (30 pF) is used for testing Series 54L/74L devices only.



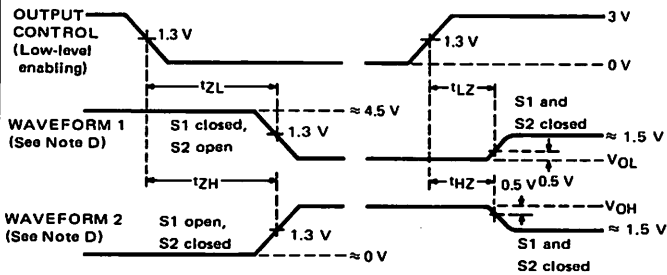
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

- NOTES:
- D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 - F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_{out} \approx 50 \Omega$ and:
 - For Series 54L/74L gates and inverters, $t_r = 60$ ns, $t_f = 60$ ns;
 - For Series 54L/74L flip-flops and MSI, $t_r < 25$ ns, $t_f < 25$ ns;
 - For Series 54LS/74LS, $t_r < 15$ ns, $t_f < 6$ ns.
 - G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

†Except 'L42, 'L43, 'L44, 'L46, 'L47, 'L75, 'L77, 'L96, 'L121, 'L122, 'L123, 'L153, 'L154, 'L157, 'L164

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54/74 Family

MSI/LSI Circuits

TTL
MSI

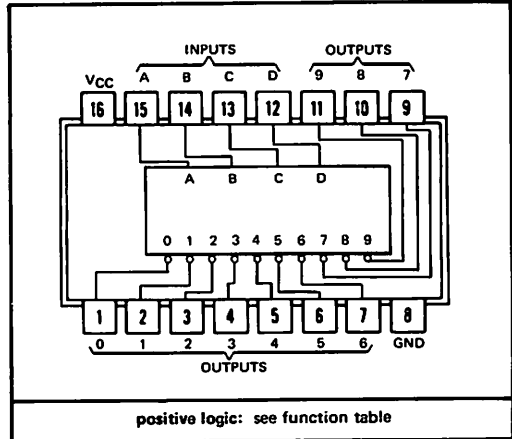
**TYPES SN5442A THRU SN5444A, SN54L42 THRU SN54L44,
SN54LS42, SN7442A THRU SN7444A,
SN74L42 THRU SN74L44, SN74LS42
4-LINE-TO-10-LINE DECODERS (1-OF-10)**

BULLETIN NO. DL-S 7411861, MARCH 1974

'42A, 'L42, 'LS42 ... BCD-TO-DECIMAL
'43A, 'L43 ... EXCESS-3-TO-DECIMAL
'44A, 'L44 ... EXCESS-3-GRAY-TO-DECIMAL

- All Outputs Are High for Invalid Input Conditions
- Also for Application as
4-Line-to-16-Line Decoders
3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

SN5442A THRU SN5444A, SN54LS42 ... J OR W PACKAGE
SN54L42 THRU SN54L44 ... J PACKAGE
SN7442A THRU SN7444A,
SN74L42 THRU SN74L44, SN74LS42 ... J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A, 'L42, and 'LS42 BCD-to-decimal decoders, the '43A and 'L43 excess-3-to-decimal decoders, and the '44A and 'L44 excess-3-gray-to-decimal decoders feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. D-c noise margins are typically one volt.

Series 54, 54L, and 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74, 74L, and 74LS circuits are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

NO.	'42A, 'L42, 'LS42 BCD INPUT				'43A, 'L43 EXCESS-3-INPUT				'44A, 'L44 EXCESS-3-GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	L	H	L	H	H	H	L	H	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H
5	L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	L	H	H	H	H	H
6	L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	L	H	H	H	H
7	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H
8	H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H
9	H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	L	H
INVALID	H	L	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

TYPES SN5442A, SN5443A, SN5444A, SN7442A, SN7443A, SN7444A

4-LINE-TO-10-LINE DECODERS (1-OF-10)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54' Circuits	-55°C to 125°C
SN74' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5442A SN5443A SN5444A			SN7442A SN7443A SN7444A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-300	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5442A SN5443A SN5444A			SN7442A SN7443A SN7444A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage			0.8			0.8		V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$		-1.5			-1.5		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		28	41		28	56	mA

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	$C_L = 15 \text{ pF}, R_L = 400 \Omega, \text{ See Note 3}$		14	25	ns
t_{PHL} Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic			17	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic			10	25	ns
t_{PLH} Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic			17	30	ns

NOTE 3: Load circuits and waveforms are shown on page S-87.

TYPES SN54L42, SN54L43, SN54L44, SN74L42, SN74L43, SN74L44
4-LINE-TO-10-LINE DECODERS (1-OF-10)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54L' Circuits	-55°C to 125°C
SN74L' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54L42 SN54L43 SN54L44			SN74L42 SN74L43 SN74L44			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			8			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 8 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.8	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-9		-28	mA
I_{CC} Supply Current	$V_{CC} = \text{MAX},$ See Note 2				mA
				SN54L' 14 22 SN74L' 14 28	

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open and inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	$C_L = 15 \text{ pF},$ $R_L = 800 \Omega,$ See Note 3	10	44	60	ns
t_{PHL} Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic			46	70	ns
t_{PLH} Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic		10	34	50	ns
t_{PLH} Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic			52	70	ns

NOTE 3: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54LS42, SN74LS42
4-LINE-TO-10-LINE DEODERS (1-OF-10)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS42	-55°C to 125°C
SN74LS42	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS42			SN74LS42			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS42			SN74LS42			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage			0.7			0.8		V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$ $V_{IL} = V_{IL \text{ max}}, I_{OL} = 8 \text{ mA}$	0.25	0.4		0.25	0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20		μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4			-0.4		mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-6	-40		-5	-42		mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2		7	13		7	13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.
§Not more than one output should be shorted at a time.
NOTE 2. I_{CC} is measured with all outputs open and inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Note 4		14	25	ns
t_{PHL} Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic			17	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic			10	25	ns
t_{PLH} Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic			17	30	ns

NOTE 4: Load circuit and voltage waveforms are shown on page S-88.

TENTATIVE DATA

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TYPES SN5446A, '47A, '48, '49, SN54L46, 'L47, SN54LS47, 'LS48, 'LS49, SN7446A, '47A, '48, SN74L46, 'L47, SN74LS47, 'LS48, 'LS49 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

BULLETIN NO. DL-S 7411811, MARCH 1974

'46A, '47A, 'L46, 'L47, 'LS47
feature

'48, 'LS48
feature

'49, 'LS49
feature

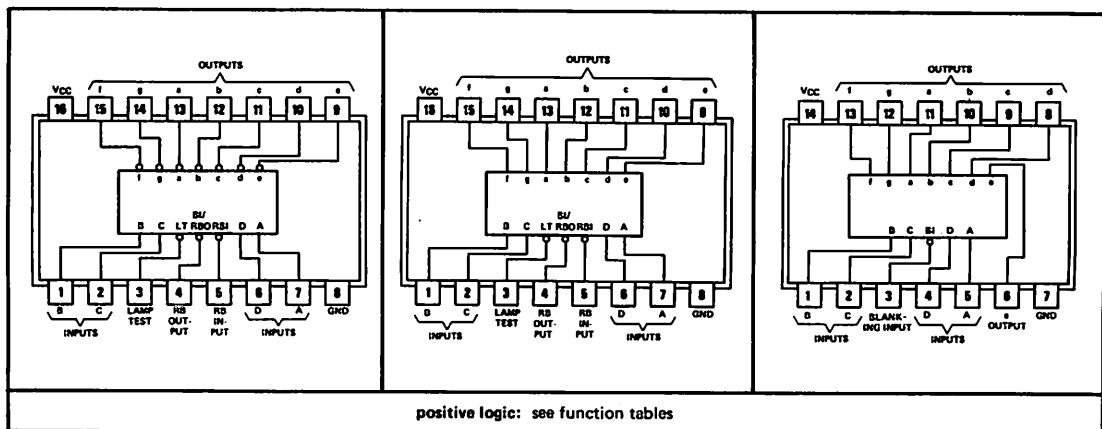
- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- Open-Collector Outputs
- Blanking Input
- All Circuit Types Feature Lamp Intensity Modulation Capability

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN5446A	low	open-collector	40 mA	30 V	320 mW	J, W
SN5447A	low	open-collector	40 mA	15 V	320 mW	J, W
SN5448	high	2-k Ω pull-up	6.4 mA	5.5 V	265 mW	J, W
SN5449	high	open-collector	10 mA	5.5 V	165 mW	W
SN54L46	low	open-collector	20 mA	30 V	160 mW	J
SN54L47	low	open-collector	20 mA	15 V	160 mW	J
SN54LS47	low	open-collector	12 mA	15 V	35 mW	J, W
SN54LS48	high	2-k Ω pull-up	2 mA	5.5 V	125 mW	J, W
SN54LS49	high	open-collector	4 mA	5.5 V	40 mW	J, W
SN7446A	low	open-collector	40 mA	30 V	320 mW	J, N
SN7447A	low	open-collector	40 mA	15 V	320 mW	J, N
SN7448	high	2-k Ω pull-up	6.4 mA	5.5 V	265 mW	J, N
SN74L46	low	open-collector	20 mA	30 V	160 mW	J, N
SN74L47	low	open-collector	20 mA	15 V	160 mW	J, N
SN74LS47	low	open-collector	24 mA	15 V	35 mW	J, N
SN74LS48	high	2-k Ω pull-up	6 mA	5.5 V	125 mW	J, N
SN74LS49	high	open-collector	8 mA	5.5 V	40 mW	J, N

'46A, '47A, 'L46, 'L47, 'LS47
(TOP VIEW)

'48, 'LS48
(TOP VIEW)

'49, 'LS49
(TOP VIEW)



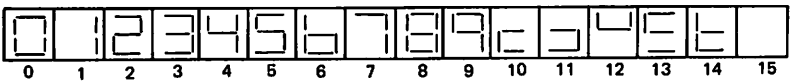
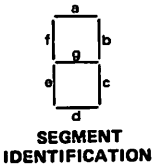
TYPES SN5446A, '47A, '48, '49, SN54L46, 'L47, SN54LS47, 'LS48, 'LS49, SN7446A, '47A, '48, SN74L46, 'L47, SN74LS47, 'LS48, 'LS49 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

description

The '46A, 'L46, '47A, 'L47, and 'LS47 feature active-low outputs designed for driving common-anode VLEDs or incandescent indicators directly, and the '48, '49, 'LS48, 'LS49 feature active-high outputs for driving lamp buffers or common-cathode VLEDs. All of the circuits except '49 and 'LS49 have full ripple-blanking input/output controls and a lamp test input. The '49 and 'LS49 circuits incorporate a direct blanking input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

The '46A, '47A, '48, 'L46, 'L47, 'LS47, and 'LS48 circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. All types (including the '49 and 'LS49) contain an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

The SN54246/SN74246 through '249 and the SN54LS247/SN74LS247 through 'LS249 compose the 6 and the 9 with tails and have been designed to offer the designer a choice between two indicator fonts. The SN54249/SN74249 and SN54LS249/SN74LS249 are 16-pin versions of the 14-pin SN5449 and 'LS49. Included in the '249 circuit and 'LS249 circuits are the full functional capability for lamp test and ripple blanking, which is not available in the '49 or 'LS49 circuit.



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

'46A, '47A, 'L46, 'L47, 'LS47 FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

- NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input (RBI) and Inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

**TYPES SN5446A, '47A, '48, '49, SN54L46, 'L47, SN54LS47, 'LS48, 'LS49,
SN7446A, '47A, '48, SN74L46, 'L47, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

**'48, 'LS48
FUNCTION TABLE**

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	L	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	L	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high, if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).

4. When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

**'49, 'LS49
FUNCTION TABLE**

DECIMAL OR FUNCTION	INPUTS					OUTPUTS							NOTE
	D	C	B	A	BI	a	b	c	d	e	f	g	
0	L	L	L	L	H	H	H	H	H	H	H	L	1
1	L	L	L	H	H	L	H	H	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	
3	L	L	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	L	H	L	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	L	L	L	L	L	L	L	L	2

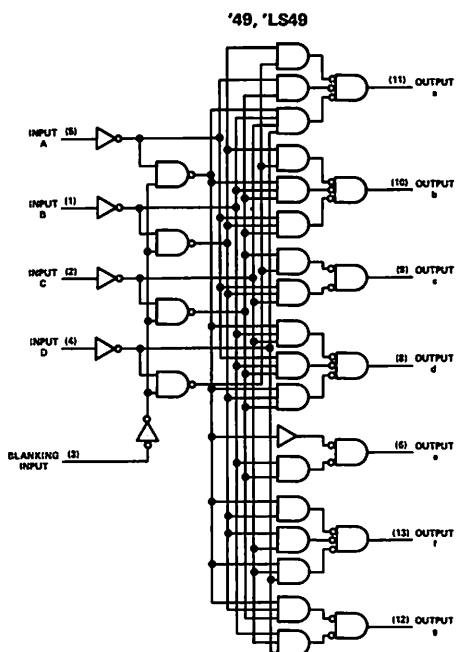
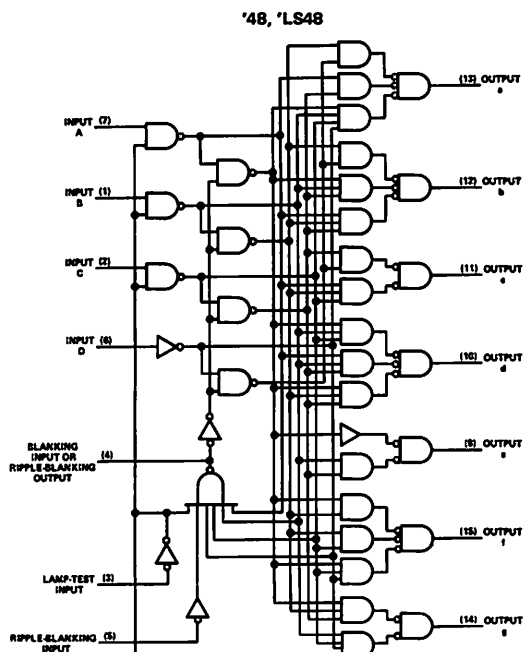
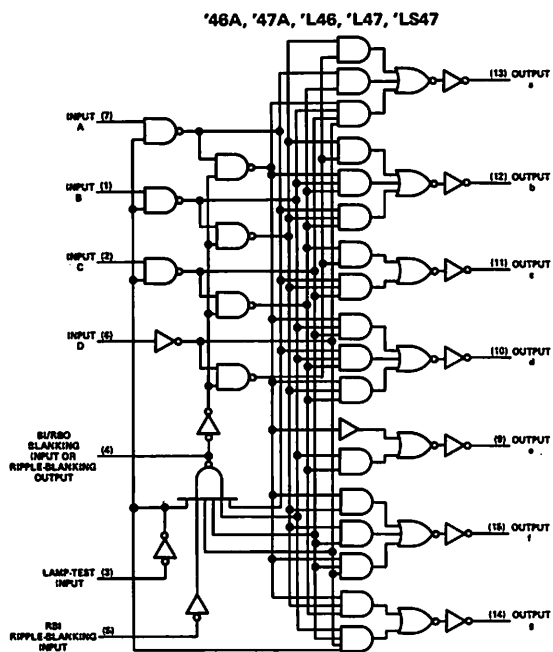
H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired.

2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

TYPES SN5446A, '47A, '48, '49, SN54L46, 'L47, SN54LS47, 'LS48, 'LS49, SN7446A, '74A, '48, SN74L46, 'L47, SN74LS47, 'LS48, 'LS49 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

functional block diagrams

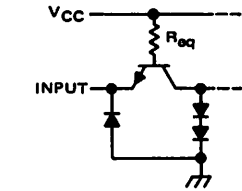


TYPES SN5446A, '47A, '48, '49, SN54L46, 'L47, SN7446A, '47A, '48, SN74L46, 'L47 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

schematics of inputs and outputs

'46A, '47A, '48, '49, 'L46, 'L47

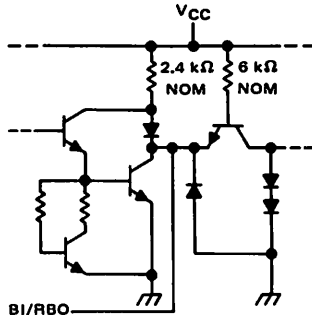
EQUIVALENT OF EACH INPUT
EXCEPT BI/RBO



SN54'/SN74': $R_{eq} = 6\text{ k}\Omega$ NOM
SN54L'/SN74L': $R_{eq} = 8\text{ k}\Omega$ NOM

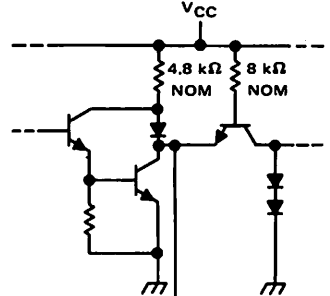
'46A, '47A, '48

EQUIVALENT OF BI/RBO



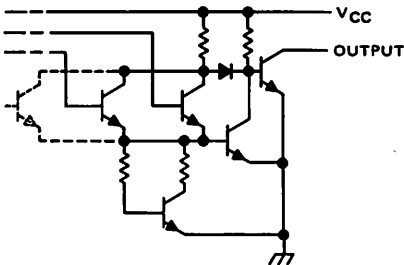
'L46, 'L47

EQUIVALENT OF BI/RBO



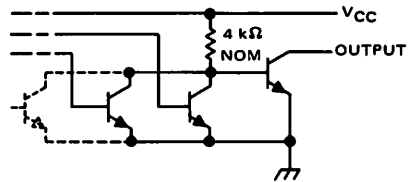
'46A, '47A

TYPICAL OF OUTPUTS
a THRU g



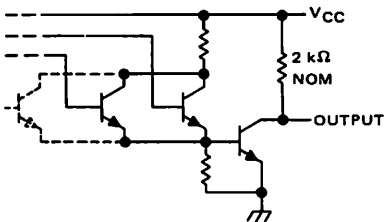
'L46, 'L47

TYPICAL OF OUTPUTS
a THRU g



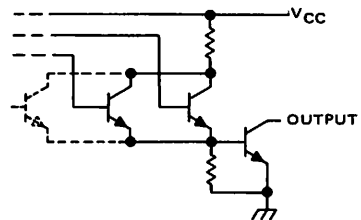
'48

TYPICAL OF OUTPUTS
a THRU g



'49

TYPICAL OF ALL OUTPUTS

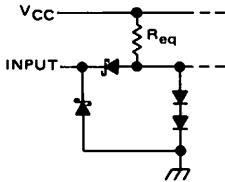


TYPES SN54LS47, 'LS48, 'LS49, SN74LS47, 'LS48, 'LS49 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

schematics of inputs and outputs

'LS47, 'LS48, 'LS49

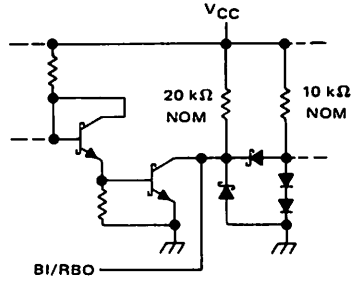
EQUIVALENT OF EACH INPUT
EXCEPT BI/RBO



LT and RBI ('LS47, 'LS48): $R_{eq} = 20\text{ k}\Omega$ NOM
BI ('LS49): $R_{eq} = 20\text{ k}\Omega$ NOM
A, B, C, and D: $R_{eq} = 25\text{ k}\Omega$ NOM

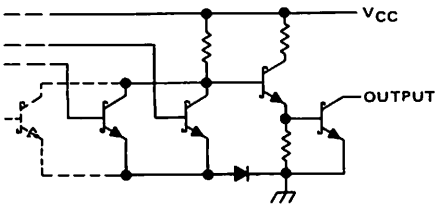
'LS47, 'LS48, 'LS49

EQUIVALENT OF BI/RBO



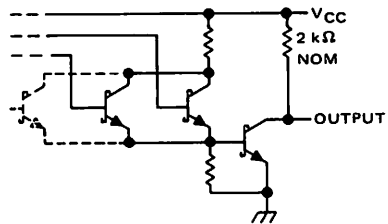
'LS47

TYPICAL OF OUTPUTS
a THRU g



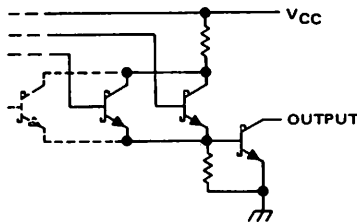
'LS48

TYPICAL OF OUTPUTS
a THRU g



'LS49

TYPICAL OF OUTPUTS
a THRU g



TYPES SN5446A, SN5447A, SN7446A, SN7447A
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

REVISED MARCH 1974

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN5446A, SN5447A	-55°C to 125°C
SN7446A, SN7447A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5446A			SN5447A			SN7446A			SN7447A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			30			15			30			15	V
On-state output current, $I_{O(on)}$	a thru g			40			40			40			40	mA
High-level output current, I_{OH}	BI/RBO			-200			-200			-200			-200	μA
Low-level output current, I_{OL}	BI/RBO			8			8			8			8	mA
Operating free-air temperature, T_A		-55		125	-55		125	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -200 \text{ μA}$		2.4	3.7		V
V_{OL}	Low-level output voltage	BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 8 \text{ mA}$			0.27	0.4	V
$I_{O(off)}$	Off-state output current	a thru g	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{O(off)} = \text{MAX}$				250	μA
$V_{O(on)}$	On-state output voltage	a thru g	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{O(on)} = 40 \text{ mA}$			0.3	0.4	V
I_I	Input current at maximum input voltage	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$				40	μA
I_{IL}	Low-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				-1.6	mA
		BI/RBO					-4	
I_{OS}	Short-circuit output current	BI/RBO	$V_{CC} = \text{MAX}$				-4	mA
I_{CC}	Supply current		$V_{CC} = \text{MAX},$ See Note 2	SN54'		64	85	mA
				SN74'		64	103	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	$C_L = 15 \text{ pF}, R_L = 120 \text{ Ω},$ See Note 3			100		ns
t_{on}	Turn-on time from A input				100		
t_{off}	Turn-off time from RBI input				100		ns
t_{on}	Turn-on time from RBI input				100		

NOTE 3: Load circuit and voltage waveforms are shown on page S-87; t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL} .

TYPES SN54L46, SN54L47, SN74L46, SN74L47

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Peak output current ($t_W \leq 1$ ms, duty cycle $\leq 10\%$)	200 mA
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54L46, SN54L47	-55°C to 125°C
SN74L46, SN74L47	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54L46			SN54L47			SN74L46			SN74L47			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			30			15			30			15	V
On-state output current, $I_{O(on)}$	a thru g			20			20			20			20	mA
High-level output current, I_{OH}	BI/RBO			-100			-100			-100			-100	μA
Low-level output current, I_{OL}	BI/RBO			4			4			4			4	mA
Operating free-air temperature, T_A		-55		125	-55		125	0		70	0		70	$^\circ\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS [†]		MIN	TYP [‡]	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	Any input except BI/RBO	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -100 \mu\text{A}$		2.4	3.4		V
V_{OL}	Low-level output voltage	BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 4 \text{ mA}$			0.2	0.4	V
$I_{O(off)}$	Off-state output current	a thru g	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{O(off)} = \text{MAX}$				250	μA
$V_{O(on)}$	On-state output voltage	a thru g	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{O(on)} = 20 \text{ mA}$			0.3	0.4	V
I_I	Input current at maximum input voltage	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$				20	μA
I_{IL}	Low-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				-0.8	mA
		BI/RBO					-2	
I_{OS}	Short-circuit output current	BI/RBO	$V_{CC} = \text{MAX}$				-2	mA
I_{CC}	Supply current		$V_{CC} = \text{MAX},$ See Note 2	SN54L'		32	43	mA
				SN74L'		32	52	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	$C_L = 15 \text{ pF}, R_L = 280 \Omega,$ See Note 3				200	ns
t_{on}	Turn-on time from A input					200	
t_{off}	Turn-off time from RBI input					200	ns
t_{on}	Turn-on time from RBI input					200	

NOTE 3: Load circuit and voltage waveforms are shown on page S-87; t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL} .

TYPES SN54LS47, SN74LS47

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Peak output current ($t_W \leq 1$ ms, duty cycle $\leq 10\%$)	200 mA
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54LS47	-55°C to 125°C
SN74LS47	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS47			SN74LS47			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g	15			15			V
On-state output current, $I_{O(on)}$	a thru g	12			24			mA
High-level output current, I_{OH}	BI/RBO	-50			-50			μA
Low-level output current, I_{OL}	BI/RBO	1.6			3.2			mA
Operating free-air temperature, T_A		-55			0			$^\circ\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS47			SN74LS47			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage		0.7			0.8			V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5			-1.5			V
V_{OH}	High-level output voltage	BI/RBO $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -50 \mu\text{A}$	2.4	4.2		2.4	4.2		V
V_{OL}	Low-level output voltage	BI/RBO $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 1.6 \text{ mA}$ $I_{OL} = 3.2 \text{ mA}$	0.25	0.4		0.25	0.4		V
$I_{O(off)}$	Off-state output current	a thru g $V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{O(off)} = 15 \text{ V}$	250			250			μA
$V_{O(on)}$	On-state output voltage	a thru g $V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{O(on)} = 12 \text{ mA}$ $I_{O(on)} = 24 \text{ mA}$	0.25	0.4		0.25	0.4		V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$	0.1			0.1			mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	20			20			μA
I_{IL}	Low-level input current	Any input except BI/RBO BI/RBO $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-0.36			-0.36			mA
I_{OS}	Short-circuit output current	BI/RBO $V_{CC} = \text{MAX}$	-0.3	-2		-0.3	-2		mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2	7	13		7	13		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input				100	
t_{on}	Turn-on time from A input	$C_L = 15 \text{ pF}, R_L = 665 \Omega,$ See Note 4			100	ns
t_{off}	Turn-off time from RBI input				100	
t_{on}	Turn-on time from RBI input				100	ns
					100	

NOTE 4: Load circuit and voltage waveforms are shown on page S-88. t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL} .

TENTATIVE DATA

S-104

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TEXAS INSTRUMENTS
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TYPES SN5448, SN7448

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

REVISED MARCH 1974

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN5448	-55°C to 125°C
SN7448	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5448			SN7448			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	a thru g			-400			-400	μ A
	BI/RBO			-200			-200	
Low-level output current, I_{OL}	a thru g			6.4			6.4	mA
	BI/RBO			8			8	
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	a thru g	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$		2.4	4.2		V
		BI/RBO			2.4	3.7		
I_O	Output current	a thru g	$V_{CC} = \text{MIN}, V_O = 0.85 \text{ V},$ Input conditions as for V_{OH}		-1.3	-2		mA
V_{OL}	Low-level output voltage		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = \text{MAX}$		0.27	0.4		V
I_I	Input current at maximum input voltage	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$				40	μ A
I_{IL}	Low-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				-1.6	mA
		BI/RBO					-4	
I_{OS}	Short-circuit output current	BI/RBO	$V_{CC} = \text{MAX}$				-4	mA
I_{CC}	Supply current		$V_{CC} = \text{MIN},$ See Note 2	SN5448		53	76	mA
				SN7448		53	90	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}, R_L = 1 \text{ k}\Omega,$ See Note 5			100		ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input				100		
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input				100		ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input				100		

NOTE 5: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54LS48, SN74LS48
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS48	-55°C to 125°C
SN74LS48	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS48			SN74LS48			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	a thru g	-100			-100			μA
	BI/RBO	-50			-50			
Low-level output current, I_{OL}	a thru g	2			6			mA
	BI/RBO	1.6			3.2			
Operating free-air temperature, T_A		-55			0			$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS48		SN74LS48		UNIT
				MIN	TYP‡	MAX	MIN	
V_{IH}	High-level input voltage			2			2	V
V_{IL}	Low-level input voltage					0.7		V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.5		V
V_{OH}	High-level output voltage	a thru g and BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = \text{MAX}$	2.4	4.2		2.4	V
I_O	Output current	a thru g	$V_{CC} = \text{MIN}, V_O = 0.85 \text{ V},$ Input conditions as for V_{OH}	-1.3	-2		-1.3	mA
V_{OL}	Low-level output voltage	a thru g	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 2 \text{ mA}$	0.25	0.4		0.25	V
			$I_{OL} = 6 \text{ mA}$				0.35	
	BI/RBO		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 1.6 \text{ mA}$	0.25	0.4		0.25	V
			$I_{OL} = 3.2 \text{ mA}$				0.35	
I_I	Input current at maximum input voltage	Any input except BI/BRO	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1		mA
I_{IH}	High-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20		μA
I_{IL}	Low-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.36		mA
		BI/RBO				-1		
I_{OS}	Short-circuit output current	BI/RBO	$V_{CC} = \text{MAX}$	-0.3	-2	-0.3	-2	mA
I_{CC}	Supply current		$V_{CC} = \text{MAX},$ See Note 2		25	38		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}, R_L = 4 \text{ k}\Omega,$				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input	See Note 6				100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input	$C_L = 15 \text{ pF}, R_L = 6 \text{ k}\Omega,$				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input	See Note 6				100	

NOTE 6: Load circuit and voltage waveforms are shown on page S-88.

TENTATIVE DATA

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TEXAS INSTRUMENTS
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TYPE SN5449
BCD-TO-SEVEN-SEGMENT DECODER/DRIVER

REVISED MARCH 1974

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Current forced into any output in the off state	1 mA
Operating free-air temperature range	-55°C to 125°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5449			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output voltage, V_{OH}			5.5	V
Low-level output current, I_{OL}			10	mA
Operating free-air temperature, T_A	-55		125	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5449			UNIT
			MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.6	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -10 \text{ mA}$			-1.5	V
I_{OH}	High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$			250	μA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 10 \text{ mA}$		0.27	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		33	47	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input	$C_L = 15 \text{ pF}, R_L = 667 \Omega,$		100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input	See Note 5		100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input			100	

NOTE 5: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54LS49, SN74LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	7 V
Input voltage	7 V
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54LS49	-55°C to 125°C
SN74LS49	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS49			SN74LS49			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, VCC	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, VOH			5.5			5.5	V
Low-level output current, IOL			4			8	mA
Operating free-air temperature, TA	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS49			SN74LS49			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IH}	High-level input voltage		2			2			V	
V _{IL}	Low-level input voltage				0.7			0.8	V	
V _I	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V	
I _{OH}	High-level output current	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, V _{OH} = 5.5 V			250			250	µA	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 4 mA		0.25	0.4	0.25		0.4	V
		I _{OL} = 8 mA				0.35		0.5		
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			1			1	mA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V			20			20	µA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.36			-0.36	mA	
I _{CC}	Supply current	V _{CC} = MAX, See Note 2			8	15		8	15	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at VCC = 5 V, TA = 25°C.

NOTE 2: ICC is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPHL Propagation delay time, high-to-low-level output from A input	CL = 15 pF, RL = 2 kΩ,			100	ns
tPLH Propagation delay time, low-to-high-level output from A input	See Note 6			100	
tPHL Propagation delay time, high-to-low-level output from RBI input	CL = 15 pF, RL = 6 kΩ,			100	ns
tPLH Propagation delay time, low-to-high-level output from RBI input	See Note 6			100	

NOTE 6: Load circuit and voltage waveforms are shown on page S-88.

TENTATIVE DATA

PRINTED IN U.S.A.

TYPES SN5475, SN5477, SN54L75, SN54L77, SN54LS75, SN54LS77, SN7475, SN74L75, SN74L77, SN74LS75 4-BIT BISTABLE LATCHES

BULLETIN NO. DL-S 7411851, MARCH 1974

logic

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	\bar{Q}
L	H	L	H
H	H	H	L
X	L	Q_0	\bar{Q}_0

H = high level, L = low level, X = Irrelevant

Q_0 = the level of Q before the high-to-low transition of G

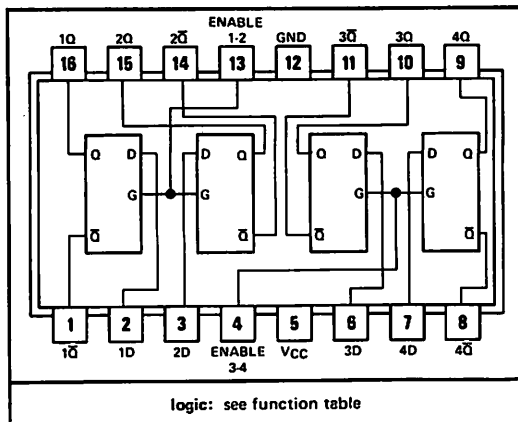
description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The '75, 'L75, and 'LS75 feature complementary Q and \bar{Q} outputs from a 4-bit latch, and are available in various 16-pin packages. For higher component density applications, the '77, 'L77, and 'LS77 4-bit latches are available in 14-pin flat packages.

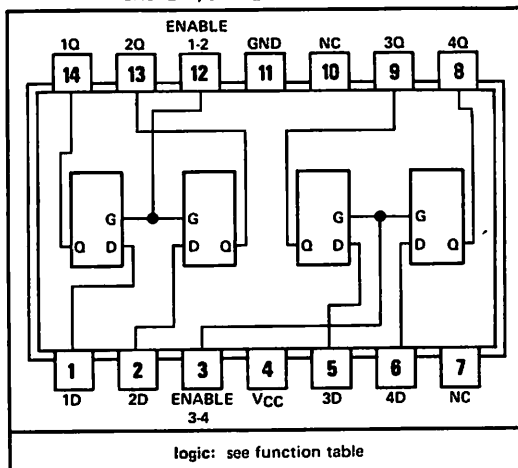
These circuits are completely compatible with all popular TTL or DTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Series 54, 54L, and 54LS devices are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74, 74L, and 74LS devices are characterized for operation from 0°C to 70°C .

SN5475, SN54LS75 ... J OR W PACKAGE
SN54L75 ... J PACKAGE
SN7475, SN74L75, SN74LS75 ... J OR N PACKAGE
(TOP VIEW)



logic: see function table

SN5477, SN54LS77 ... W PACKAGE
SN54L77, SN74L77 ... T PACKAGE



logic: see function table

NC—No Internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

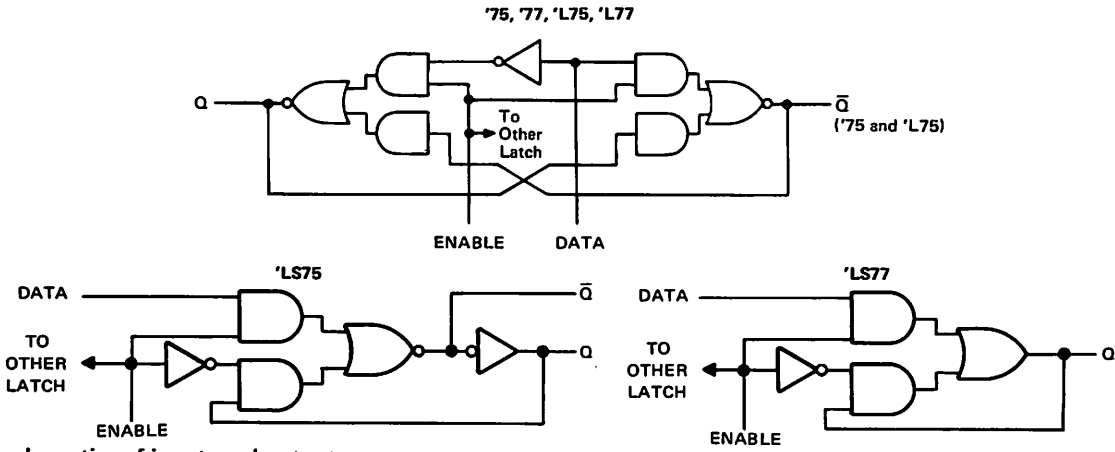
Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '75, 'L75, '77, 'L77	5.5 V
'LS75, 'LS77	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54', SN54L', SN54LS' Circuits	-55°C to 125°C
SN74', SN74L', SN74LS' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor.

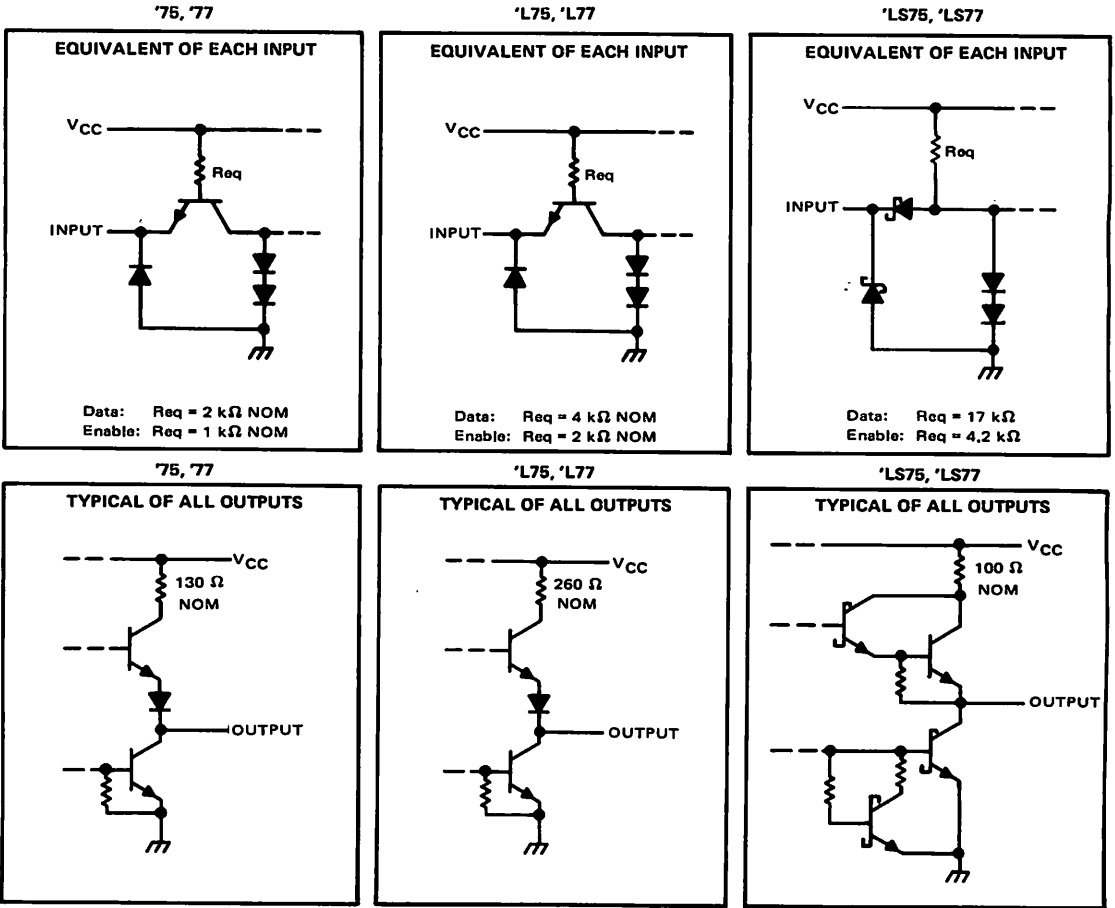
TYPES SN5475, SN5477, SN54L75, SN54L77, SN54LS75, SN54LS77, SN7475, SN74L75, SN74L77, SN74LS75

4-BIT BISTABLE LATCHES

functional block diagrams (each latch)



schematics of inputs and outputs



TYPES SN5475, SN5477, SN7475

4-BIT BISTABLE LATCHES

REVISED MARCH 1974

recommended operating conditions

	SN5475, SN5477			SN7475			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			16			16	mA
Width of enabling pulse, t_w	20			20			ns
Setup time, t_{setup}	20			20			ns
Hold time, t_{hold}	5			5			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$			0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$	D input			80	μ A
			G input			160	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	D input			-3.2	mA
			G input			-6.4	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	SN54*	-20		-57	mA
			SN74*	-18		-57	
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 3	SN54*		32	46	mA
			SN74*		32	53	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER [◇]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	Q	$C_L = 15 \text{ pF},$ $R_L = 400 \Omega,$ See Figure 1	16	30	ns	
t_{PHL}				14	25		
t_{PLH}^{\ddagger}	D	\bar{Q}		24	40	ns	
t_{PHL}^{\ddagger}		7		15			
t_{PLH}	G	Q		16	30	ns	
t_{PHL}				7	15		
t_{PLH}^{\ddagger}	G	\bar{Q}		16	30	ns	
t_{PHL}^{\ddagger}				7	15		

[◇] $t_{PLH} \equiv$ propagation delay time, low-to-high-level output

$t_{PHL} \equiv$ propagation delay time, high-to-low-level output

[‡] These parameters are not applicable for the SN5477.

TYPES SN54L75, SN54L77, SN74L75, SN74L77
4-BIT BISTABLE LATCHES

REVISED MARCH 1974

recommended operating conditions

Table with 8 columns: Parameter, SN54L75, SN54L77 (MIN, NOM, MAX), SN74L75, SN74L77 (MIN, NOM, MAX), UNIT. Rows include Supply voltage, VCC; High-level output current, IOH; Low-level output current, IOL; Width of enabling pulse, tw; Setup time, tsetup; Hold time, thold; Operating free-air temperature, TA.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Table with 6 columns: PARAMETER, TEST CONDITIONS†, MIN, TYP‡, MAX, UNIT. Rows include VIH, VIL, VI, VOH, VOL, II, IiH, IiL, IOS, ICC.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at VCC = 5 V, TA = 25°C.
§Nor more than one output should be shorted at a time.
NOTE 3: ICC is tested with all inputs grounded and all outputs open.

switching characteristics, VCC = 5 V, TA = 25°C

Table with 7 columns: PARAMETER°, FROM (INPUT), TO (OUTPUT), TEST CONDITIONS, MIN, TYP, MAX, UNIT. Rows include tPLH, tPHL, tPLH¶, tPHL¶.

°tPLH ≡ propagation delay time, low-to-high-level output
¶tPHL ≡ propagation delay time, high-to-low-level output
¶ These parameters are not applicable for the SN54L77 and SN74L77.

TYPES SN54LS75, SN54LS77, SN74LS75 4-BIT BISTABLE LATCHES

recommended operating conditions

	SN54LS75 SN54LS77			SN74LS75			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Width of enabling pulse, t_W	20			20			ns
Setup time, t_{setup}	20			20			ns
Hold time, t_{hold}	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS75 SN54LS77			SN74LS75			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}, I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			0.4			0.4	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			20			20	μ A
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$			80			80	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$			-0.4			-0.4	mA
				-1.6			-1.6	mA
								mA
				-6			-42	mA
								mA
				6.3			12	mA
				6.9			13	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER [◇]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS75			'LS77			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	D	Q	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ See Figure 1}$	15	27		11	19		ns
t_{PHL}	D	Q		9	17		9	17		ns
t_{PLH}	D	\bar{Q}		12	20					ns
t_{PHL}	D	\bar{Q}		7	15					ns
t_{PLH}	G	Q		15	27		10	18		ns
t_{PHL}	G	Q		14	25		10	18		ns
t_{PLH}	G	\bar{Q}		16	30					ns
t_{PHL}	G	\bar{Q}		7	15					ns

[◇] $t_{PLH} \equiv$ propagation delay time, low-to-high-level output

$t_{PHL} \equiv$ propagation delay time, high-to-low-level output

TENTATIVE DATA

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

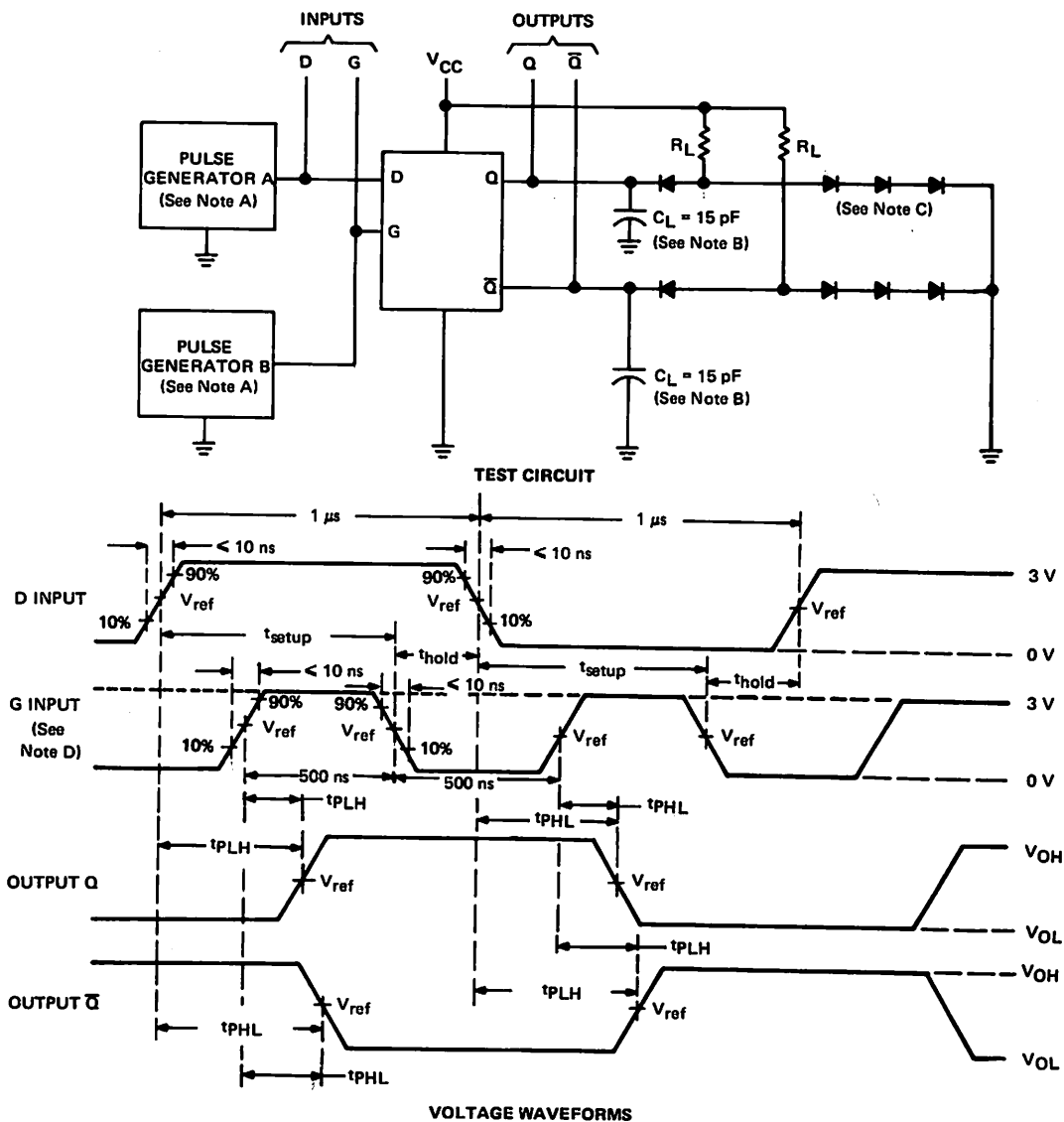
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S-113

TYPES SN5475, SN5477, SN54L75, SN54L77, SN54LS75, SN54LS77, SN7475, SN74L75, SN74L77, SN74LS75 4-BIT BISTABLE LATCHES

PARAMETER MEASUREMENT INFORMATION

switching characteristics†



- NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50 \Omega$; for pulse generator A, $PRR \leq 500 \text{ kHz}$; for pulse generator B, $PRR \leq 1 \text{ MHz}$. Positions of D and G input pulses are varied with respect to each other to verify setup times.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064.
- D. When measuring propagation delay times from the D input, the corresponding G input must be held high.
- E. For '75, '77, 'L75, and 'L77, $V_{ref} = 1.5 \text{ V}$; for 'LS75 and 'LS77, $V_{ref} = 1.3 \text{ V}$.
- †Complementary \bar{Q} outputs are on the '75, 'L75, and 'LS75 only.

FIGURE 1

TYPES SN5483A, SN54LS83A, SN7483A, SN74LS83A
4-BIT BINARY FULL ADDERS WITH FAST CARRY

BULLETIN NO. DL-S 7411853, MARCH 1974

- Full-Carry Look-Ahead across the Four Bits
- Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry
- SN54283/SN74283 and SN54LS283/SN74LS283 Are Recommended For New Designs as They Feature Supply Voltage and Ground on Corner Pins to Simplify Board Layout

TYPE	TYPICAL ADD TIMES		TYPICAL POWER DISSIPATION PER 4-BIT ADDER
	TWO 8-BIT WORDS	TWO 16-BIT WORDS	
'83A	23 ns	43 ns	310 mW
'LS83A	25 ns	45 ns	95 mW

description

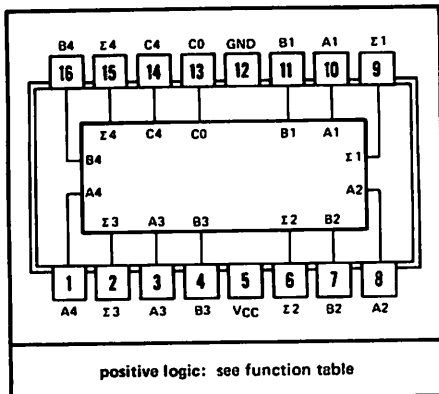
These improved full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Designed for medium-speed applications, the circuits utilize transistor-transistor logic that is compatible with most other TTL families and other saturated low-level logic families.

Series 54 and 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C , and Series 74 and 74LS circuits are characterized for operation from 0°C to 70°C .

SN5483A, SN54LS83A . . . J OR W PACKAGE
SN7483A, SN74LS83A . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

FUNCTION TABLE

INPUT		OUTPUT							
		WHEN $C_0 = L$				WHEN $C_0 = H$			
		WHEN $C_2 = L$		WHEN $C_2 = H$		WHEN $C_2 = L$		WHEN $C_2 = H$	
A1	B1	A2	B2	Z1	Z2	C2	Z1	Z2	C2
A3	B3	A4	B4	Z3	Z4	C4	Z3	Z4	C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	L	L	L	L	L	H
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	L	H	H	L	H
H	L	L	H	L	L	H	L	L	H
L	H	L	H	L	L	H	L	L	H
H	H	L	H	L	L	H	L	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	L	L	H	L	L	H
L	H	H	H	L	L	H	L	L	H
H	H	H	H	L	L	H	H	L	H

H = high level, L = low level

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Z1 and Z2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Z3, Z4, and C4.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '83A	5.5 V
'LS83A	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5483A, SN54LS83A	-55°C to 125°C
SN7483A, SN74LS83A	0°C to 70°C
Storage temperature range	-65°C to 150°C

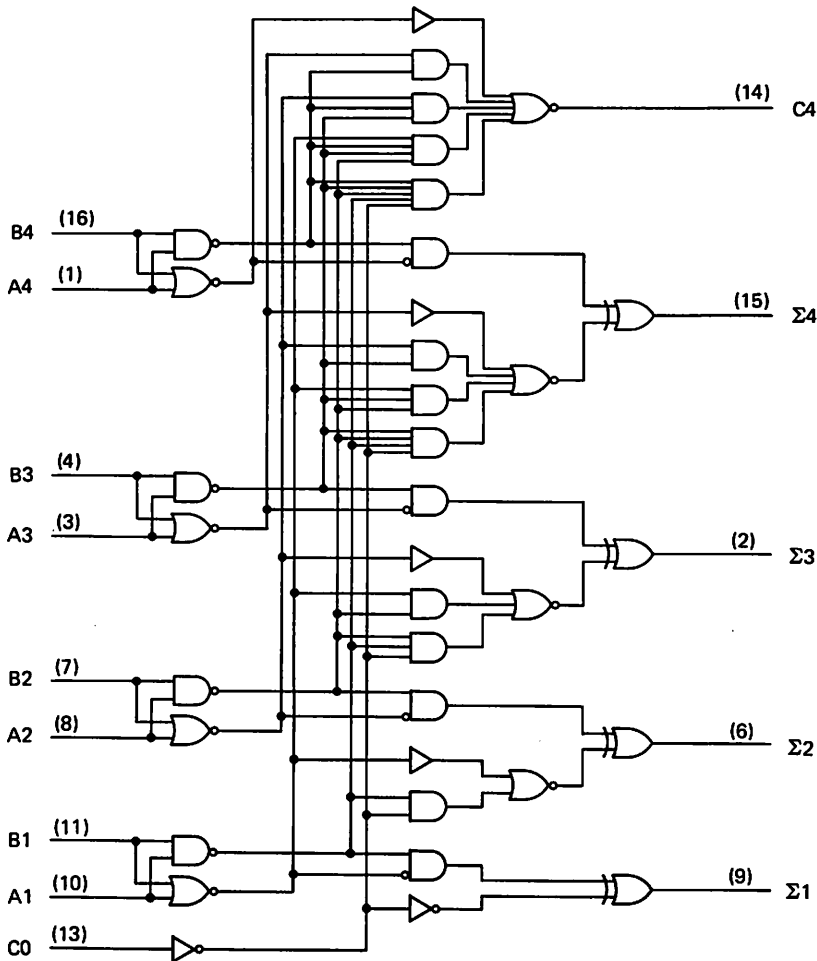
NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '83A only between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4.

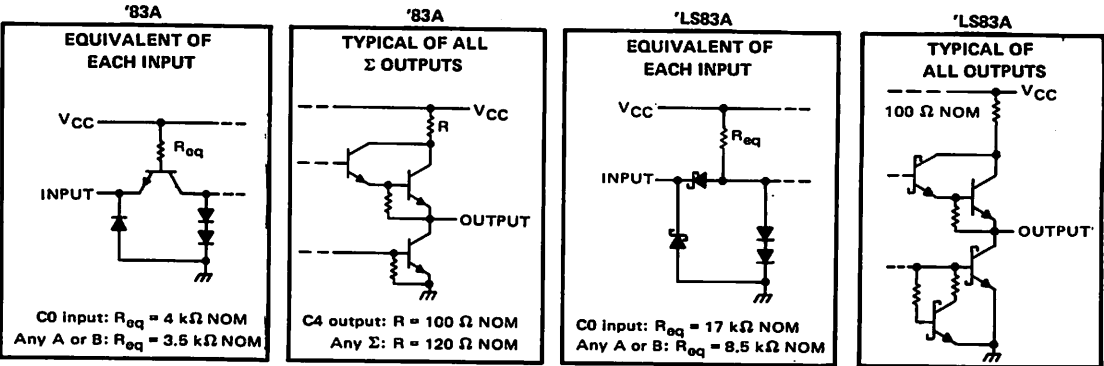
TYPES SN5483A, SN54LS83A, SN7483A, SN74LS83A

4-BIT BINARY FULL ADDERS WITH FAST CARRY

functional block diagram



schematics of inputs and outputs



TYPES SN5483A, SN7483A

4-BIT BINARY FULL ADDERS WITH FAST CARRY

recommended operating conditions

		SN5483A			SN7483A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Any output except C4	-800			-800			μ A
	Output C4	-400			-400			μ A
Low-level output current, I_{OL}	Any output except C4	16			16			mA
	Output C4	8			8			mA
Operating free-air temperature, T_A		-55	125		0	70		$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5483A			SN7483A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage		0.8			0.8			V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$	-1.5			-1.5			V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = \text{MAX}$	0.2	0.4		0.2	0.4		V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1			1			mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$	40			40			μ A
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-1.6			-1.6			mA
I_{OS}	Short-circuit output current§	Any output except C4	-20	-55		-18	-55		mA
		Output C4	-20	-70		-18	-70		
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ All 8 low, other inputs at 4.5 V	56			56			mA
		Outputs open, All inputs at 4.5 V	66	99		66	110		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Only one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

switching characteristics, VCC = 5 V, I _A = 25 mA							
PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	C0	Any Σ	C _L = 15 pF, R _L = 400 Ω, See Note 3	14	21	ns	
t _{PHL}				12	21		
t _{PLH}	A _i or B _i	Σ _i		16	24	ns	
t _{PHL}				16	24		
t _{PLH}	C0	C4	C _L = 15 pF, R _L = 780 Ω, See Note 3	9	14	ns	
t _{PHL}				11	16		
t _{PLH}	A _i or B _i	C4		9	14	ns	
t _{PHL}				11	16		

¶ t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

NOTE 3: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54LS83A, SN74LS83A

4-BIT BINARY FULL ADDERS WITH FAST CARRY

recommended operating conditions

	SN54LS83A			SN74LS83A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS83A			SN74LS83A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.4	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$ $V_{IL} = V_{IL \text{ max}}, I_{OL} = 8 \text{ mA}$	0.25	0.4		0.25	0.4		V
I_I	Input current at maximum input voltage	Any A or B			0.2			0.2	mA
		C0			0.1			0.1	
I_{IH}	High-level input current	Any A or B			40			40	μ A
		C0			20			20	
I_{IL}	Low-level input current	Any A or B			-0.8			-0.8	mA
		C0			-0.4			-0.4	
I_{OS}	Short-circuit output current §	$V_{CC} = \text{MAX}$	-6		-40	-5		-42	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ Outputs open							mA
		All inputs grounded	22		39	22		39	
		All B low, other inputs at 4.5 V	19		34	19		34	
		All inputs at 4.5 V	19		34	19		34	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Only one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	C0	Any Σ	C _L = 15 pF, See Note 4	R _L = 2 kΩ,		16	24	ns
t _{PHL}						15	24	
t _{PLH}	A _i or B _i	Σ _i				15	24	ns
t _{PHL}						15	24	
t _{PLH}	C0	C4				11	17	ns
t _{PHL}						11	17	
t _{PLH}	A _i or B _i	C4				11	17	ns
t _{PHL}						12	17	

¶ $t_{PLH} \equiv$ Propagation delay time, low-to-high-level output

$t_{PHL} \equiv$ Propagation delay time, high-to-low-level output

Note 4: Load circuit and voltage waveforms are shown on page S-88.

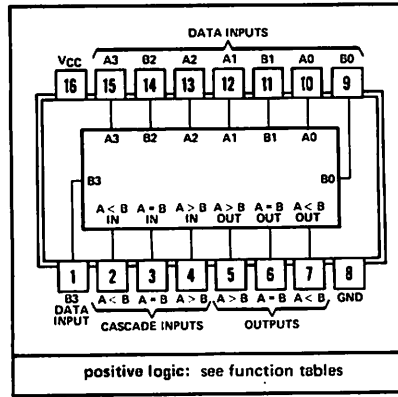
TYPES SN5485, SN54L85, SN54LS85, SN54S85, SN7485, SN74L85, SN74LS85, SN74S85 4-BIT MAGNITUDE COMPARATORS

BULLETIN NO. DL-S 7411810, MARCH 1974

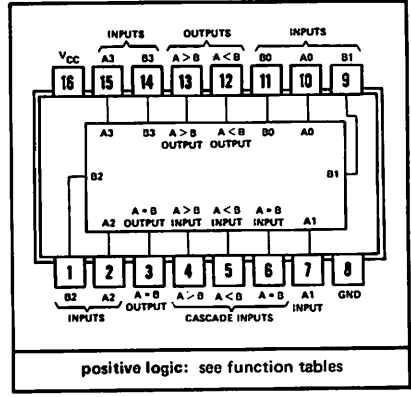
SN5485, SN54LS85, SN54S85 . . . J OR W PACKAGE
SN7485, SN74LS85, SN74S85 . . . J OR N PACKAGE
(TOP VIEW)

SN54L85 . . . J PACKAGE
SN74L85 . . . J OR N PACKAGE
(TOP VIEW)

TYPE	TYPICAL POWER DISSIPATION	TYPICAL DELAY (4-BIT WORDS)
'85	275 mW	23 ns
'L85	20 mW	90 ns
'LS85	52 mW	24 ns
'S85	365 mW	11 ns



positive logic: see function tables



positive logic: see function tables

description

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The $A > B$, $A < B$, and $A = B$ outputs of a stage handling less-significant bits are connected to the corresponding $A > B$, $A < B$, and $A = B$ inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the $A = B$ input and in addition for the 'L85, low-level voltages applied to the $A > B$ and $A < B$ inputs. The cascading paths of the '85, 'LS85, and 'S85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

FUNCTION TABLES

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

'85, 'LS85, 'S85

A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

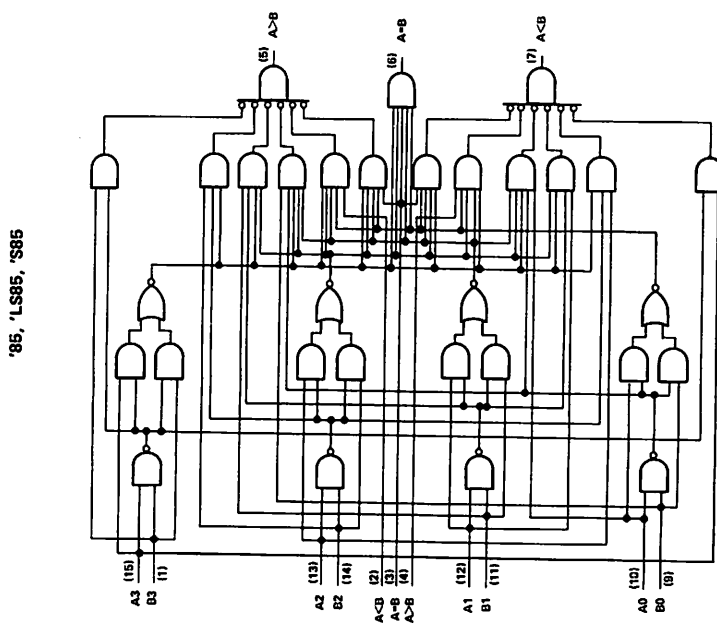
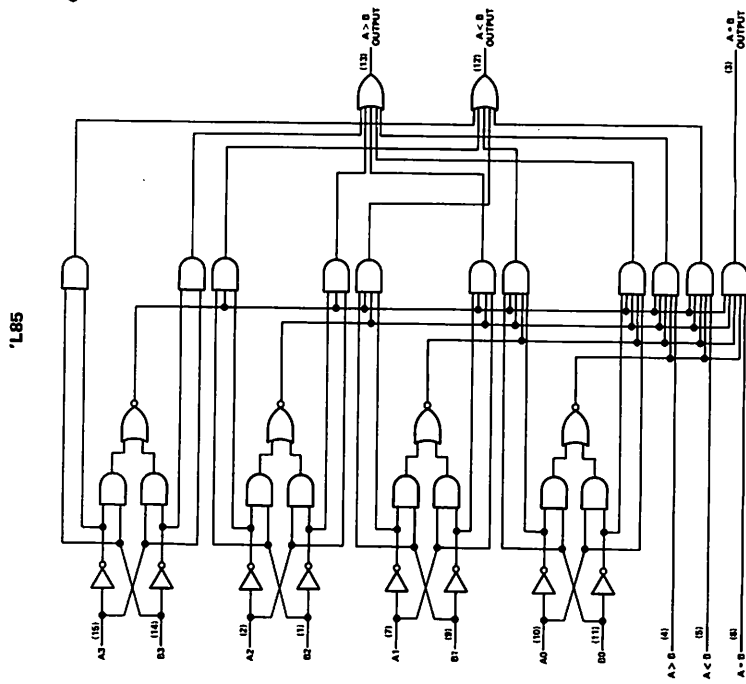
'L85

A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

H = high level, L = low level, X = irrelevant

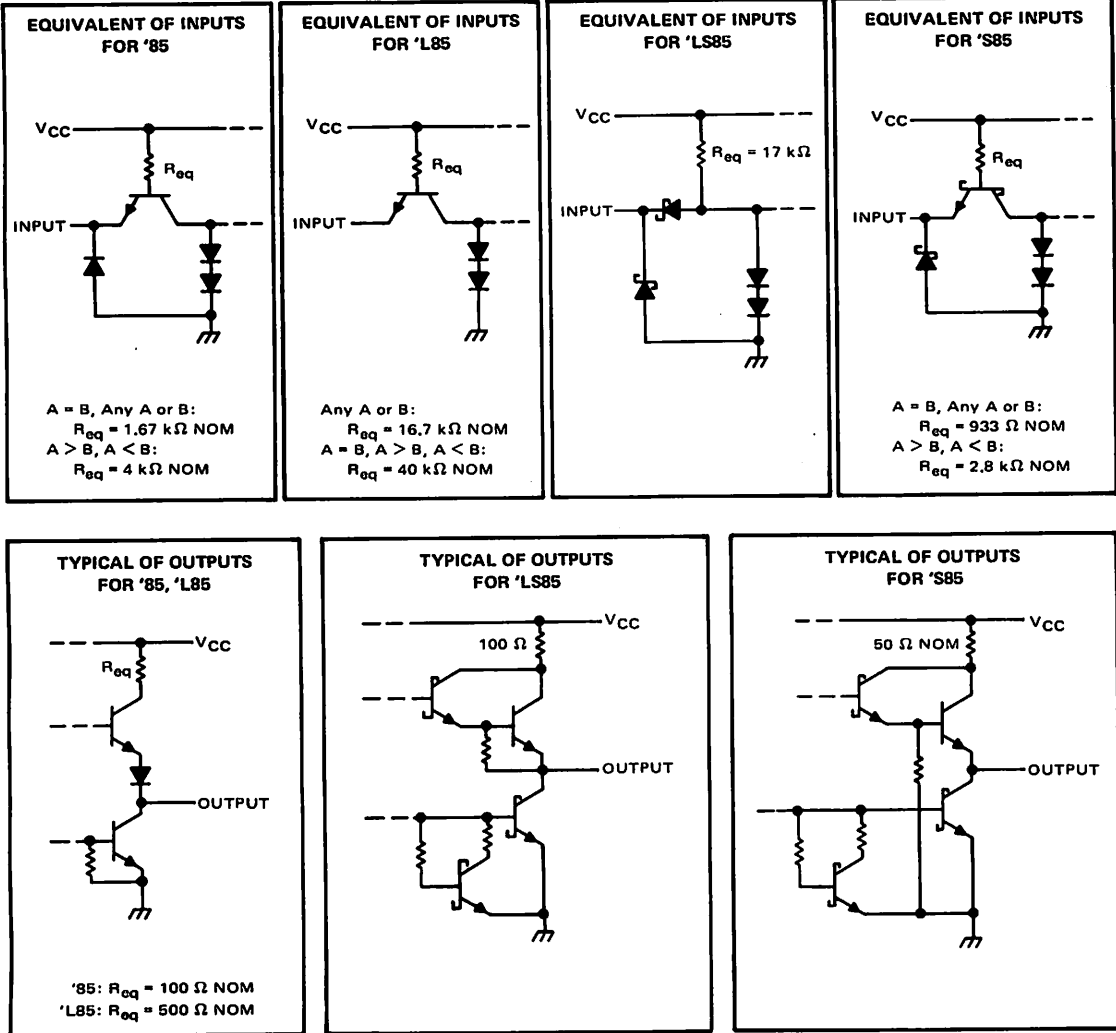
**TYPES SN5485, SN54L85, SN54LS85, SN54S85,
SN7485, SN74L85, SN74LS85, SN74S85
4-BIT MAGNITUDE COMPARATORS**

functional block diagrams



TYPES SN5485, SN54L85, SN54LS85, SN54S85, SN7485, SN74L85, SN74LS85, SN74S85 4-BIT MAGNITUDE COMPARATORS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54' SN54S'	SN54L'	SN54LS'	SN74' SN74S'	SN74L'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	8	7	7	8	7	V
Input voltage (see Note 2)	5.5	5.5	7	5.5	5.5	7	V
Interemitter voltage (see Note 3)	5.5			5.5			V
Operating free-air temperature range	-55 to 125			0 to 70			°C
Storage temperature range	-65 to 150			-65 to 150			°C

- NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
 2. Input voltages for 'L85 must be zero or positive with respect to network ground terminal.
 3. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies to each A input in conjunction with its respective B input of the '85 and 'S85.

TYPES SN5485, SN7485

4-BIT MAGNITUDE COMPARATORS

recommended operating conditions

	SN5485			SN7485			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN},$ $I_I = -12 \text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN},$ $V_{IL} = 0.8 \text{ V},$ $I_{OH} = -400 \mu\text{A}$	$V_{IH} = 2 \text{ V},$ $I_{OH} = -400 \mu\text{A}$	2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN},$ $V_{IL} = 0.8 \text{ V},$ $I_{OL} = 16 \text{ mA}$	$V_{IH} = 2 \text{ V},$ $I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX},$ $V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	$A < B, A > B$ inputs all other inputs	$V_{CC} = \text{MAX},$ $V_I = 2.4 \text{ V}$			40 120	μ A
I_{IL}	Low-level input current	$A < B, A > B$ inputs all other inputs	$V_{CC} = \text{MAX},$ $V_I = 0.4 \text{ V}$			-1.6 -4.8	mA
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}, V_O = 0$	SN5485 SN7485	-20 -18		-55 -55	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 4			55	88	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}.$

§Not more than one output should be shorted at a time.

NOTE 4: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	$A < B, A > B$	1	$C_L = 15 \text{ pF},$ $R_L = 400 \Omega,$ See Note 5		7		ns
			2			12		
			3			17	26	
		$A = B$	4			23	35	
t_{PHL}	Any A or B data input	$A < B, A > B$	1			11		ns
			2			15		
			3			20	30	
		$A = B$	4			20	30	
t_{PLH}	$A < B$ or $A = B$	$A > B$	1			7	11	ns
t_{PHL}	$A < B$ or $A = B$	$A > B$	1			11	17	ns
t_{PLH}	$A = B$	$A = B$	2			13	20	ns
t_{PHL}	$A = B$	$A = B$	2			11	17	ns
t_{PLH}	$A > B$ or $A = B$	$A < B$	1			7	11	ns
t_{PHL}	$A > B$ or $A = B$	$A < B$	1			11	17	ns

¶ t_{PLH} \equiv propagation delay time, low-to-high-level output

t_{PHL} \equiv propagation delay time, high-to-low-level output.

NOTE 5: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54L85, SN74L85

4-BIT MAGNITUDE COMPARATORS

recommended operating conditions

	SN54L85			SN74L85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-100			-200	μ A
Low-level output current, I_{OL}			2			3.6	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.7	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.7 \text{ V}, I_{OH} = \text{MAX}$	SN54L85 SN74L85	2.4 2.4	3.3 3.2		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.7 \text{ V}, I_{OL} = \text{MAX}$	SN54L85 SN74L85		0.15 0.2	0.3 0.4	V
I_I	Input current at maximum input voltage	$A < B, A > B, \text{ or } A = B$ A or B inputs	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			100 300	μ A
I_{IH}	High-level input current	$A < B, A < B, \text{ or } A = B$ A or B inputs	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			10 30	μ A
I_{IL}	Low-level input current	$A < B, A > B, \text{ or } A = B$ A or B inputs	$V_{CC} = \text{MAX}, V_I = 0.3 \text{ V}$			-0.18 -0.54	mA
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$		-3		-15	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 6}$	Condition A Condition B		4.0 3.2	7.7 7.2	mA

†for conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 6: With all outputs open, I_{CC} is measured for Condition A with all inputs at 4.5 V, and for Condition B with all inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	Any A or B	Any	CL = 50 pF, RL = 4 kΩ, See Note 7	90	150		ns
tPHL				75	150		
tPLH	A > B, A < B, or A = B	Any		75	150		ns
tPHL				55	100		

¶ t_{PLH} \equiv propagation delay time, low-to-high-level output

t_{PHL} \equiv propagation delay time, high-to-low-level output

NOTE 7: Load circuit and voltage waveforms are shown on page S-88.

TYPES SN54LS85, SN74LS85
4-BIT MAGNITUDE COMPARATORS

recommended operating conditions

	SN54LS85			SN74LS85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS85			SN74LS85			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I	Input current at maximum input voltage	A < B, A > B inputs	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1	mA
		all other inputs			0.3			0.3	
I_{IH}	High-level input current	A < B, A > B inputs	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20	μ A
		all other inputs			60			60	
I_{IL}	Low-level input current	A < B, A > B inputs	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4			-0.4	mA
		all other inputs			-1.2			-1.2	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-6		-40	-5		-42	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 4		10.4	20		10.4	20	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 4: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER†	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Note 5		14		ns
			2			19		
		A = B	3			24	36	
			4			23	35	
t_{PHL}	Any A or B data input	A < B, A > B	1			11		ns
			2			15		
		A = B	3			20	30	
			4			20	30	
t_{PLH}	A < B or A = B	A > B	1			14	22	ns
t_{PHL}	A < B or A = B	A > B	1			11	17	ns
t_{PLH}	A = B	A = B	2			13	20	ns
t_{PHL}	A = B	A = B	2			11	17	ns
t_{PLH}	A > B or A = B	A < B	1			14	22	ns
t_{PHL}	A > B or A = B	A < B	1			11	17	ns

† $t_{PLH} \equiv$ propagation delay time, low-to-high-level output

$t_{PHL} \equiv$ propagation delay time, high-to-low-level output

NOTE 7: Load circuit and voltage waveforms are shown on page S-88.

TYPES SN54S85, SN74S85

4-BIT MAGNITUDE COMPARATORS

recommended operating conditions

	SN54S85			SN74S85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	SN54S85 2.5	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$	SN74S85 2.7	3.4		V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1		mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		50		µA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$		-2		mA
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 4}$		73	115	mA
		$V_{CC} = \text{MAX}, T_A = 125^\circ\text{C}, \text{ See Note 4}$			110	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 4: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	$C_L = 15 \text{ pF}, R_L = 280 \Omega, \text{ See Note 5}$		5		ns
			2			7.5		
			3			10.5	16	
		A = B	4			12	18	
t_{PHL}	Any A or B data input	A < B, A > B	1			5.5		ns
			2			7		
			3			11	16.5	
		A = B	4			11	16.5	
t_{PLH}	A < B or A = B	A > B	1			5	7.5	ns
t_{PHL}	A < B or A = B	A > B	1			5.5	8.5	ns
t_{PLH}	A = B	A = B	2			7	10.5	ns
t_{PHL}	A = B	A = B	2			5	7.5	ns
t_{PLH}	A > B or A = B	A < B	1			5	7.5	ns
t_{PHL}	A > B or A = B	A < B	1			5.5	8.5	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 5: Load circuit and voltage waveforms are shown on page S-87.

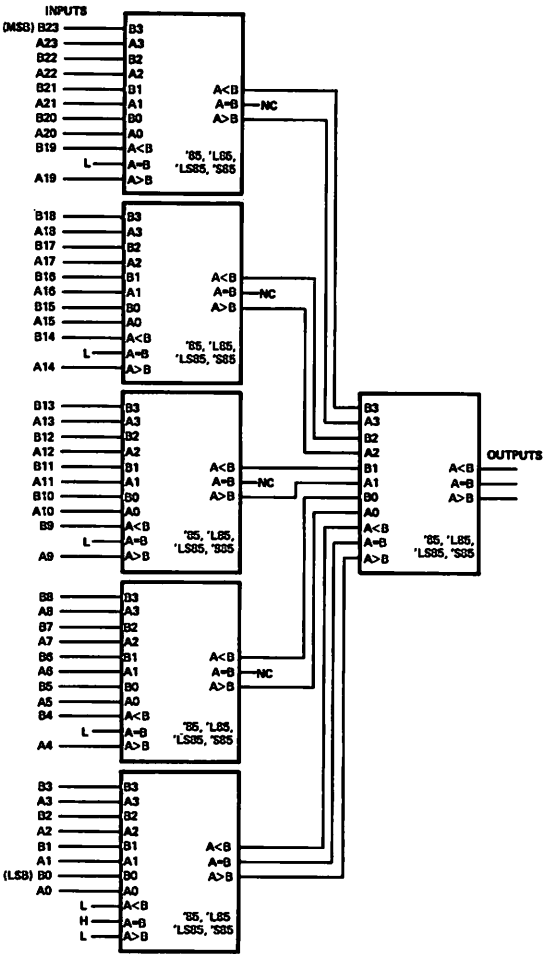
TYPES SN5485, SN54L85, SN54LS85, SN54S85, SN7485, SN74L85, SN74LS85, SN74S85 4-BIT MAGNITUDE COMPARATORS

TYPICAL APPLICATION DATA

COMPARISON OF TWO N-BIT WORDS

This application demonstrates how these magnitude comparators can be cascaded to compare longer words. The example illustrated shows the comparison of two 24-bit words; however, the design is expandable to n-bits. As an example, one comparator can be used with five of the 24-bit comparators illustrated to expand the word length to 120-bits. Typical comparison times for various word lengths using the '85, 'L85, 'LS85, or 'S85 are:

WORD LENGTH	NUMBER OF PKGS	'85	'L85	'LS85	'S85
1-4 bits	1	23 ns	90 ns	24 ns	11 ns
5-24 bits	2-6	46 ns	180 ns	48 ns	22 ns
25-120 bits	8-31	69 ns	270 ns	72 ns	33 ns



COMPARISON OF TWO 24-BIT WORDS

**TYPES SN5490A, SN5492A, SN5493A, SN54L90, SN54L93,
SN54LS90, SN54LS92, SN54LS93, SN7490A, SN7492A, SN7493A,
SN74L90, SN74L93, SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS**

BULLETIN NO. DL-S 7411807, MARCH 1974

'90A, 'L90, 'LS90 ... DECADE COUNTERS

'92A, 'LS92 ... DIVIDE-BY-TWELVE COUNTERS

'93A, 'L93, 'LS93 ... 4-BIT BINARY COUNTERS

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'L90	20 mW
'LS90	45 mW
'92A, '93A	130 mW
'LS92, 'LS93	45 mW
'L93	16 mW

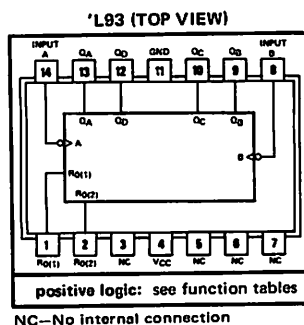
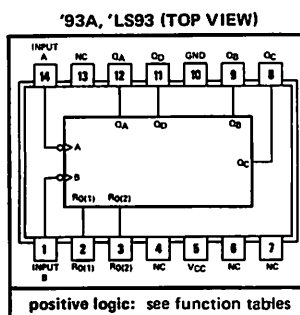
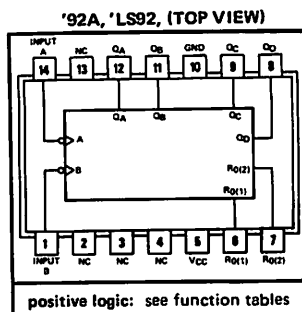
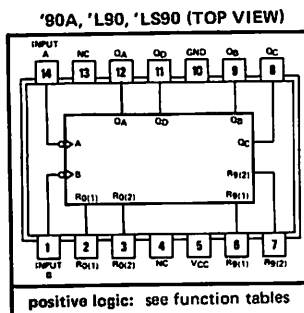
description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, 'L90, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, 'L93, and 'LS93.

All of these counters have a gated zero reset and the '90A, 'L90, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, 'L90, or 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A .

SN54', SN54LS' ... J OR W PACKAGE
SN54L', SN74L' ... J, N, OR T PACKAGE
SN74', SN74LS' ... J OR N PACKAGE



TYPES SN5490A, '92A, '93A, SN54L90, 'L93, SN54LS90, 'LS92, 'LS93, SN7490A, '92A, '93A, SN74L90, 'L93, SN74LS90, 'LS92, 'LS93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

'90A, 'L90, 'LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'L90, 'LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'92A, 'LS92
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'93A, 'L93, 'LS93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

'90A, 'L90, 'LS90
RESET/COUNT FUNCTION TABLE

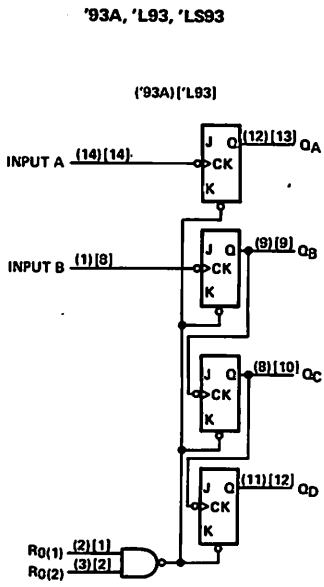
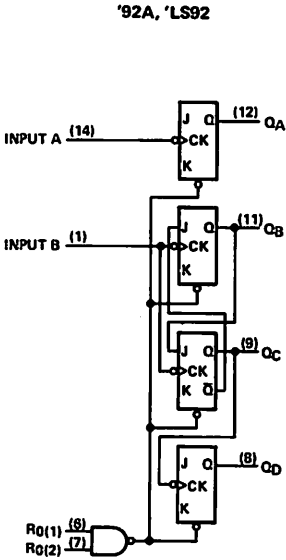
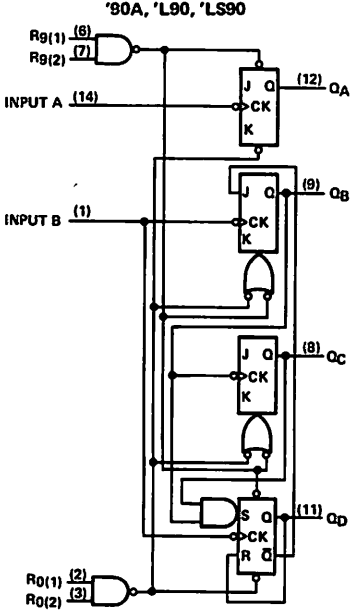
RESET INPUTS				OUTPUT			
R ₀ (1)	R ₀ (2)	R ₉ (1)	R ₉ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'92A, 'LS92, '93A, 'L93, 'LS93
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

- NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

functional block diagrams

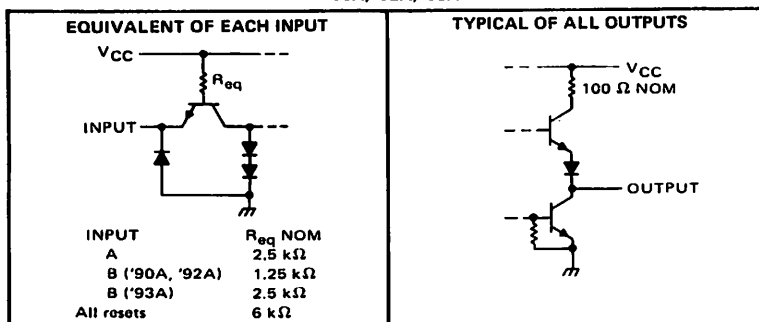


The J and K inputs shown without connection are for reference only and are functionally at a high level.

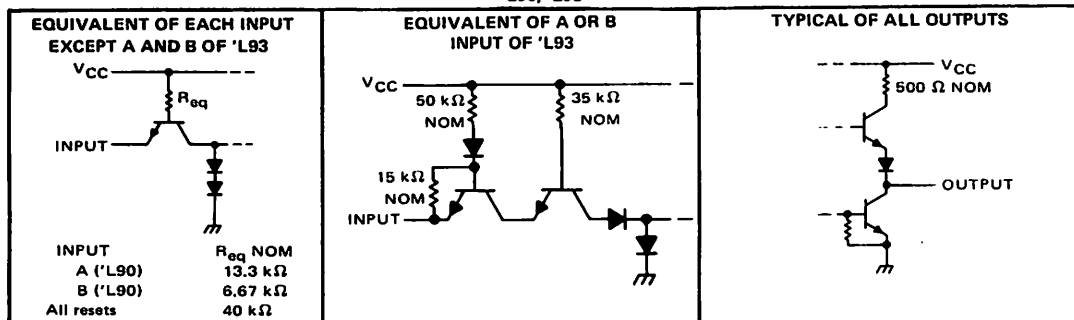
TYPES SN5490A, '92A, '93A, SN54L90, 'L93, SN54LS90, 'LS92, 'LS93, SN7490A, '92A, '93A, SN74L90, 'L93, SN74LS90, 'LS92, 'LS93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

schematics of inputs and outputs

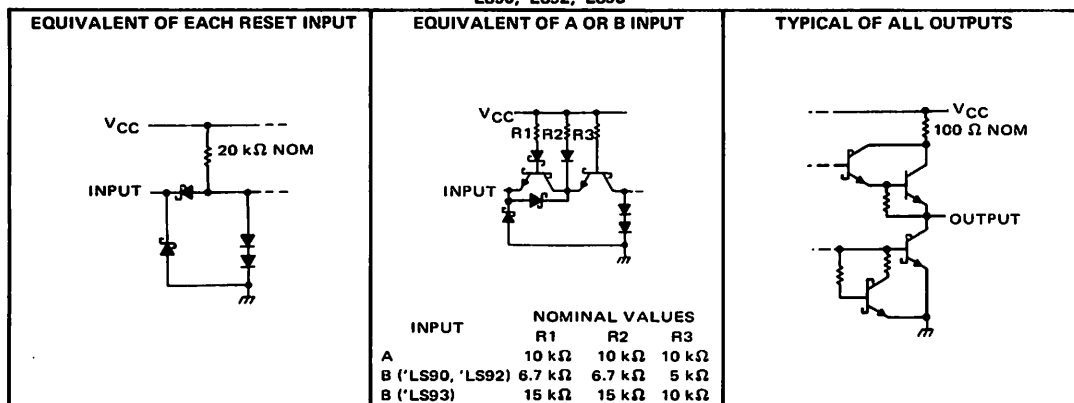
'90A, '92A, '93A



'L90, 'L93



'LS90, 'LS92, 'LS93



TYPES SN5490A, SN5492A, SN5493A, SN7490A, SN7492A, SN7493A

DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5490A, SN5492A, SN5493A	-55°C to 125°C
SN7490A, SN7492A, SN7493A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_O inputs, and for the '90A circuit, it also applies between the two R_B inputs.

recommended operating conditions

		SN5490A, SN5492A SN5493A			SN7490A, SN7492A SN7493A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-800			-800			μ A
Low-level output current, I_{OL}		16			16			mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup time, t_{setup}		25			25			ns
Operating free-air temperature, T_A		-55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'90A			'92A			'93A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				-1.5			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}^{\S}$			0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1			1			1	mA
I_{IH}	High-level input current	Any reset				40			40			40	μ A
		A input	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			80			80			80	
		B input				120			120			80	
I_{IL}	Low-level input current	Any reset				-1.6			-1.6			-1.6	mA
		A input	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-3.2			-3.2			-3.2	
		B input				-4.8			-4.8			-3.2	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	SN54'	-20	-57	-20	-57	-20	-57	-20	-57	-20	mA
			SN74'	-18	-57	-18	-57	-18	-57	-18	-57	-57	
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 3}$		29	42		26	39		26	39		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.
§ Not more than one output should be shorted at a time.
¶ QA outputs are tested at $I_{OL} = 16 \text{ mA}$ plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.
NOTE 3: I_{CC} is measured with all outputs open, both R_O inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

TYPES SN5490A, SN5492A, SN5493A, SN7490A, SN7492A, SN7493A
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'90A			'92A			'93A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	A	Q _A	C _L = 15 pF, R _L = 400 Ω, See Figure 1	32	42		32	42		32	42		MHz
	B	Q _B		16			16			16			
t _{PLH}	A	Q _A		10	16		10	16		10	16		ns
t _{PHL}				12	18		12	18		12	18		
t _{PLH}	A	Q _D		32	48		32	48		46	70		ns
t _{PHL}				34	50		34	50		46	70		
t _{PLH}	B	Q _B		10	16		10	16		10	16		ns
t _{PHL}				14	21		14	21		14	21		
t _{PLH}	B	Q _C		21	32		10	16		21	32		ns
t _{PHL}				23	35		14	21		23	35		
t _{PLH}	B	Q _D		21	32		21	32		34	51		ns
t _{PHL}				23	35		23	35		34	51		
t _{PHL}	Set-to-0	Any		26	40		26	40		26	40		ns
t _{PLH}	Set-to-9	Q _A , Q _D		20	30								ns
t _{PHL}		Q _B , Q _C		26	24								

† f_{\max} \equiv maximum count frequency

t_{PLH} \equiv propagation delay time, low-to-high-level output

t_{PHL} \equiv propagation delay time, high-to-low-level output

TYPES SN54L90, SN54L93, SN74L90, SN74L93

DECADE AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4)	8 V
Input voltage (see Note 5)	5.5 V
Operating free-air temperature range: SN54L90, SN54L93	-55°C to 125°C
SN74L90, SN74L93	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 4. Voltage values are with respect to network ground terminal.
5. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN54L90, SN54L93			SN74L90, SN74L93			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Count frequency, f_{count}	0		3	0		3	MHz
High-level output current, I_{OH}			-100			-200	μ A
Low-level output current, I_{OL}			2			3.6	mA
Width of input count pulse, $t_w(count)$	200			200			ns
Width of reset pulse, $t_w(reset)$	200			200			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'L90		'L93		UNIT		
				MIN	TYP‡	MAX	MIN		TYP‡	MAX
V _{IH}	High-level input voltage			2			2		V	
V _{IL}	Low-level input voltage					0.7			0.7	V
V _{OH}	High-level output voltage	SN54L'	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.7 V, I _{OH} = MAX	2.4	3.3		2.4	3.3		V
		SN74L'		2.4	3.2		2.4	3.2		
V _{OL}	Low-level output voltage	SN54L'	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.7 V, I _{OL} = MAX¶		0.15	0.3		0.15	0.3	V
		SN74L'			0.2	0.4		0.2	0.4	
I _I	Input current at maximum input voltage	Any reset input	V _{CC} = MAX, V _I = 5.5 V				100		100	μA
		A input					300		200	
		B input					600		200	
I _{IH}	High-level input current	Any reset input	V _{CC} = MAX, V _I = 2.4 V				10		10	μA
		A input					30		20	
		B input					60		20	
I _{IL}	Low-level input current	Any reset input	V _{CC} = MAX, V _I = 0.3 V				−0.18		−0.18	mA
		A input					−0.54		−0.36	
		B input					−1.08		−0.36	
I _{OS}	Short-circuit output current§		V _{CC} = MAX	−3		−15	−3		−15	mA
I _{CC}	Supply current		V _{CC} = MAX, See Note 3		4	7.2		3.2	6.6	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

¶Q_A outputs are tested at $I_{OL} = \text{MAX}$ plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_Q inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	'L90			'L93			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Maximum count frequency		3	6		3	6		MHz
t_{PLH}	Propagation delay time, low-to-high-level Q _D output from input A	$C_L = 50 \text{ pF}, R_L = 4 \text{ k}\Omega$, See Figure 1	230	340		280	450		ns
t_{PHL}	Propagation delay time, high-to-low-level Q _D output from input A		230	340		280	450		ns

TYPES SN54LS90, SN54LS92, SN54LS93, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4)	7 V
Input voltage: R inputs	7 V
A and B inputs	5.5 V
Operating free-air temperature range: SN54LS' Circuits	-55°C to 125°C
SN74LS' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 4: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS90 SN54LS92 SN54LS93			SN74LS90 SN74LS92 SN74LS93			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-400 [†]			-400			μA
Low-level output current, I_{OL}		4			8			mA
Count frequency, f_{count} (see Figure 1)	A input	0	32		0	32		MHz
	B input	0	16		0	16		
Pulse width, t_W	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup time, t_{setup}		25			25			ns
Operating free-air temperature, T_A		-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]		SN54LS90 SN54LS92			SN74LS90 SN74LS92			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}^{\S}$		0.25	0.4		0.25	0.4		V
		$I_{OL} = 8 \text{ mA}^{\S}$					0.35	0.5		
I_I	Input current at maximum input voltage	Any reset	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
		A input	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			0.4			0.4	
		B input				0.8			0.8	
I_{IH}	High-level input current	Any reset				20			20	μA
		A input	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			80			80	
		B input				160			160	
I_{IL}	Low-level output current	Any reset	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
		A input				-2.4			-2.4	
		B input				-3.2			-3.2	
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$		-6		-40	-5		-42	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 3	'LS90		9	15		9	15	mA
			'LS92		9	15		9	15	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§]Not more than one output should be shorted at a time.

[¶]Outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_O inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

TENTATIVE DATA

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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**TYPES SN54LS90, SN54LS92, SN54LS93,
SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS93			SN74LS93			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _I	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max							V
		I _{OL} = 4 mA¶		0.25	0.4		0.25	0.4	
		I _{OL} = 8 mA¶					0.35	0.5	
I _I	Input current at maximum input voltage	Any reset			0.1			0.1	mA
		A or B input			0.4			0.4	
I _{IH}	High-level input current	Any reset			20			20	µA
		A or B input			80			80	
I _{IL}	Low-level output current	Any reset			-0.4			-0.4	mA
		A input			-2.4			-2.4	
		B input			-1.6			-1.6	
I _{OS}	Short-circuit output current§	V _{CC} = MAX	-6		-40	-6		-42	mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 3		9	15		9	15	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

¶Q_A outputs are tested at specified I_{OL} plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS90		'LS92		'LS93		UNIT
				MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	
f _{max}	A	Q _A	C _L = 15 pF, R _L = 2 kΩ See Figure 1	32	42	32	42	32	42	MHz
	B	Q _B		16		16		16		
t _{PLH}	A	Q _A		10	16	10	16	10	16	ns
t _{PHL}	A	Q _A		12	18	12	18	12	18	
t _{PLH}	A	Q _D		32	48	32	48	46	70	ns
t _{PHL}	A	Q _D		34	50	34	50	46	70	
t _{PLH}	B	Q _B		10	16	10	16	10	16	ns
t _{PHL}	B	Q _B		14	21	14	21	14	21	
t _{PLH}	B	Q _C		21	32	10	16	21	32	ns
t _{PHL}	B	Q _C		23	35	14	21	23	35	
t _{PLH}	B	Q _D		21	32	21	32	34	51	ns
t _{PHL}	B	Q _D		23	35	23	35	34	51	
t _{PHL}	Set-to-0	Any		26	40	26	40	26	40	ns
t _{PLH}	Set-to-9	Q _A , Q _D		20	30					ns
t _{PHL}	Set-to-9	Q _B , Q _C		26	24					

¶f_{max} = maximum count frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

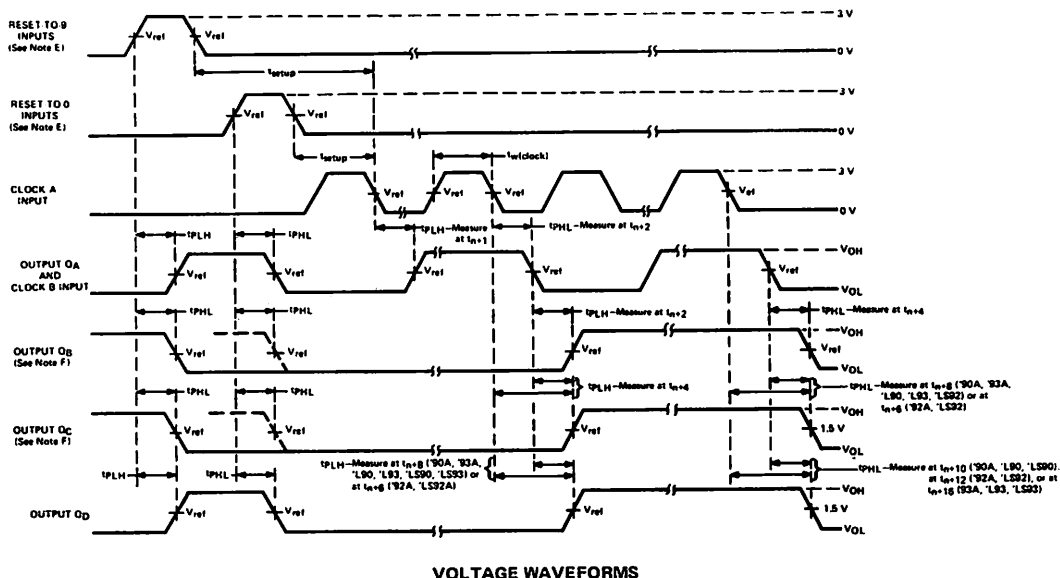
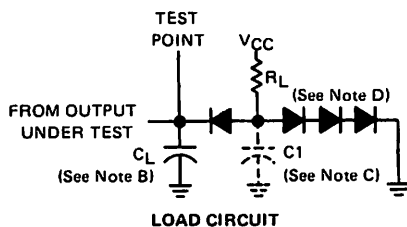
TENTATIVE DATA

S-134 This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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TYPES SN5490A, SN5492A, SN5493A, SN54L90, SN54L93, SN54LS90, SN54LS92, SN54LS93, SN7490A, SN7492A, SN7493A, SN74L90, SN74L93, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

PARAMETER MEASUREMENT INFORMATION



- NOTES:**
- Input pulses are supplied by a generator having the following characteristics:
for '90A, '92A, '93A, $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
for 'L90, 'L93, $t_r \leq 15$ ns, $t_f \leq 15$ ns, PRR = 500 kHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
for 'LS90, 'LS92, 'LS93, $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
 - C_L includes probe and jig capacitance.
 - C_1 (30 pF) is applicable for testing 'L90 and 'L93.
 - All diodes are 1N916 or 1N3064.
 - Each reset input is tested separately with the other reset at 4.5 V.
 - Reference waveforms are shown with dashed lines.
 - For '90A, '92A, and '93A; $V_{ref} = 1.5$ V. For 'L90, 'L93, 'LS90, 'LS92, and 'LS93; $V_{ref} = 1.3$ V.

FIGURE 1

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S-135

TYPES SN5491A, SN54L91, SN54LS91, SN7491A, SN74L91, SN74LS91 8-BIT SHIFT REGISTERS

BULLETIN NO. DL-S 7411854, MARCH 1974

MSI TTL SHIFT REGISTERS for applications in

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

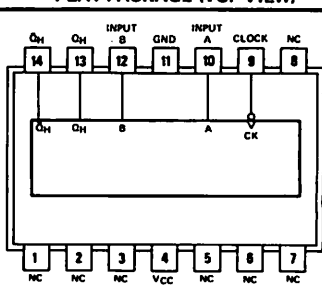
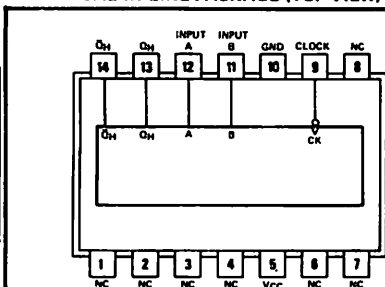
SN5491A, SN54LS91 ... J PACKAGE
SN54L91, SN7491A, SN74L91, SN74LS91 ... J OR N PACKAGE
DUAL-IN-LINE PACKAGE (TOP VIEW)

SN5491A, SN54LS91 ... W PACKAGE
SN54L91, SN74L91 ... T PACKAGE
FLAT PACKAGE (TOP VIEW)

FUNCTION TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+8}	
A	B	Q_H	\bar{Q}_H
H	H	H	L
L	X	L	H
X	L	L	H

H = high, L = low,
X = irrelevant
 t_n = Reference bit time,
clock low
 t_{n+8} = Bit time after 8
low-to-high
clock transitions.



positive logic: see function table

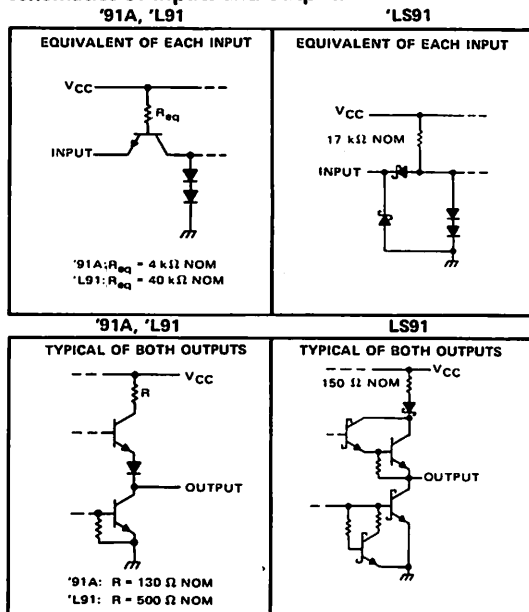
NC—No internal connection

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'91A	18 MHz	175 mW
'L91	6.5 MHz	17.5 mW
'LS91	18 MHz	60 mW

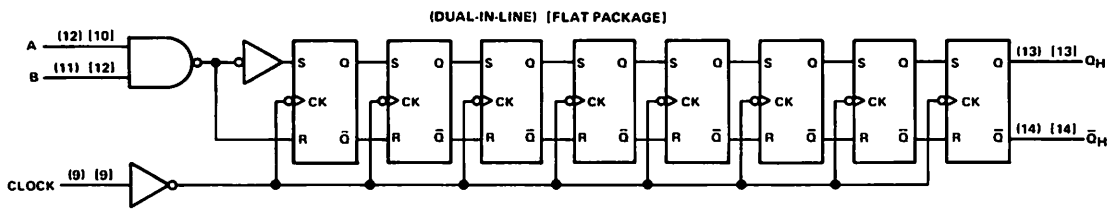
description

These monolithic serial-in, serial-out, 8-bit shift registers utilize transistor-transistor logic (TTL) circuits and are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

schematics of inputs and outputs



functional block diagram



TYPES SN5491A, SN7491A

8-BIT SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5491A	-55°C to 125°C
SN7491A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN5491A			SN7491A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			16			16	mA
Width of clock input pulse, t_w	25			25			ns
Setup time, t_{setup} (see Figure 1)	25			25			ns
Hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5491A			SN7491A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$	2.4	3.5		2.4	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current‡	$V_{CC} = \text{MAX}$	-20	-57		-18	-57		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 3		35	50		35	58	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}$,	10	18		MHz
t_{PLH} Propagation delay time, low-to-high-level output	$R_L = 400 \Omega$,		24	40	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Figure 1		27	40	ns

TYPES SN54L91, SN74L91
8-BIT SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	8 V
Input voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54L91	-55°C to 125°C
SN74L91	0°C to 70°C
Storage temperature range	-65°C to 150°C

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

		SN54L91			SN74L91			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-100			-200			μA
Low-level output current, I_{OL}		2			3.6			mA
Width of clock input pulse, $t_w(\text{clock})$	High logic level	100			100			ns
	Low logic level	150			150			ns
Setup time, t_{setup} (see Figure 1)		120			120			ns
Hold time, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		-55			0			$^{\circ}\text{C}$
		125			70			

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54L91			SN74L91			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage			0.7			0.7			V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN},$ $V_{IL} = 0.7 \text{ V},$	$V_{IH} = 2 \text{ V},$ $I_{OH} = \text{MAX}$	2.4	3.3		2.4	3.2		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN},$ $V_{IL} = 0.7 \text{ V},$	$V_{IH} = 2 \text{ V},$ $I_{OL} = \text{MAX}$		0.15	0.3		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX},$	$V_I = 5.5 \text{ V}$	100			100			μA
I_{IH}	High-level input current	$V_{CC} = \text{MAX},$	$V_I = 2.4 \text{ V}$	10			10			μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX},$	$V_I = 0.3 \text{ V}$	-0.18			-0.18			mA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}$		-3	-15		-3	-15		mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$	See Note 3	3.5	6.6		3.5	6.6		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

NOTE 3: I_{CC} is measured after the eighth clock pulse with the outputs open and A and B inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f _{max}	Maximum clock frequency	C _L = 50 pF, R _L = 4 kΩ, See Figure 1		3	6.5		MHz
t _{PLH}	Propagation delay time, low-to-high-level output				55	100	ns
t _{PHL}	Propagation delay time, high-to-low-level output				100	150	ns

TYPES SN54LS91, SN74LS91
8-BIT SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS91	-55°C to 125°C
SN74LS91	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS91			SN74LS91			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Width of clock input pulse, t_w	25			25			ns
Setup time, t_{setup} (see Figure 1)	25			25			ns
Hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS91			SN74LS91			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25 0.4	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25 0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-6		-40	-5		-42	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 3	12		20	12		20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF},$	10	18		MHz
t_{PLH} Propagation delay time, low-to-high-level output	$R_L = 2 \text{ k}\Omega,$		24	40	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Figure 1		27	40	ns

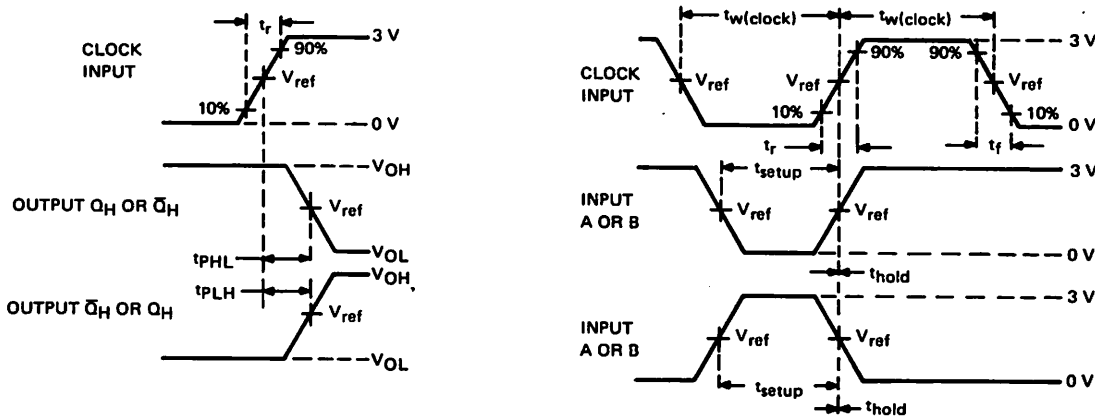
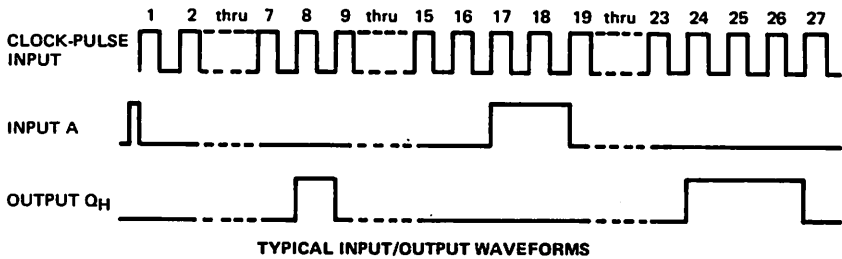
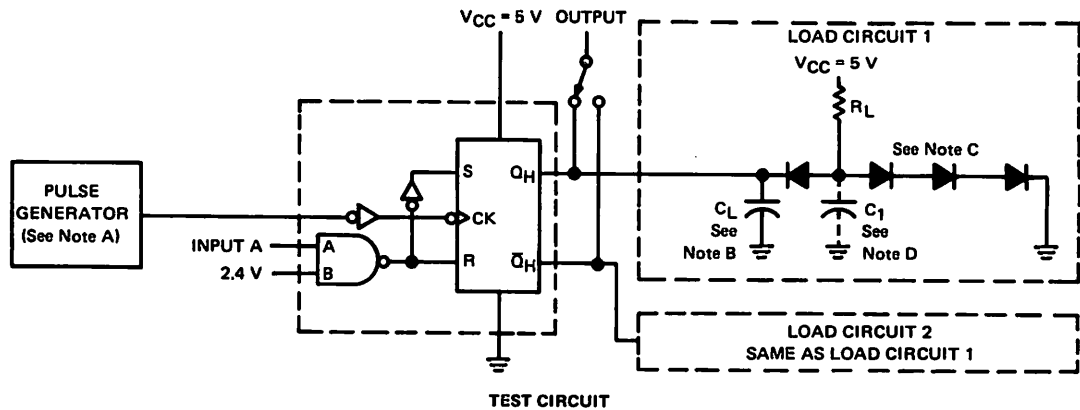
TENTATIVE DATA

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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TYPES SN5491A, SN54L91, SN54LS91, SN7491A, SN74L91, SN74LS91 8-BIT SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



PROPAGATION DELAY TIMES VOLTAGE WAVEFORMS

SWITCHING TIMES VOLTAGE WAVEFORMS

- NOTES: A. The generator has the following characteristics: $t_w(\text{clock}) = 500 \text{ ns}$, $\text{PRR} < 1 \text{ MHz}$, $Z_{\text{out}} \approx 50 \Omega$. For SN5491A/SN7491A, $t_r < 10 \text{ ns}$ and $t_f < 10 \text{ ns}$; for SN54L91/SN74L91, $t_r < 15 \text{ ns}$ and $t_f < 15 \text{ ns}$; and for SN54LS91/SN74LS91, $t_r = 15 \text{ ns}$, and $t_f = 6 \text{ ns}$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or 1N916.
- D. $C_1 = 30 \text{ pF}$ and is used for SN54L91/SN74L91 only.
- E. For SN5491A/SN7491A, $V_{\text{ref}} = 1.5 \text{ V}$; for SN54L91/SN74L91 and SN54LS91/SN74LS91, $V_{\text{ref}} = 1.3 \text{ V}$.

FIGURE 1—SWITCHING TIMES

TTL
MSI

TYPES SN5495A, SN54L95, SN54LS95B, SN7495A, SN74L95, SN74LS95B 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

BULLETIN NO: DL-S 7411872, MARCH 1974

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'95A	36 MHz	195 mW
'L95	5 MHz	19 mW
'LS95B	36 MHz	65 mW

description

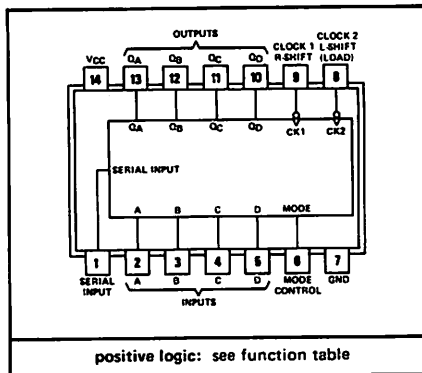
These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

- Parallel (broadside) load
- Shift right (the direction Q_A toward Q_D)
- Shift left (the direction Q_D toward Q_A)

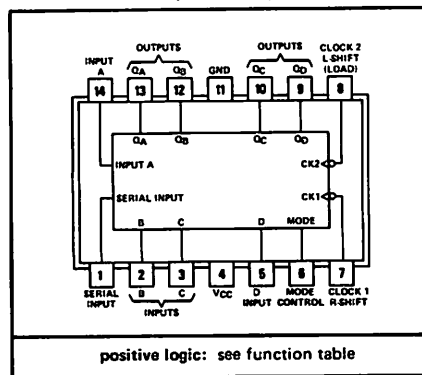
Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

SN5495A, SN54LS95B . . . J OR W PACKAGE
SN7495A, SN74LS95B . . . J OR N PACKAGE
(TOP VIEW)



SN54L95, SN74L95 . . . J, N, OR T PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS							OUTPUTS				
MODE CONTROL	CLOCKS		SERIAL	PARALLEL				Q _A	Q _B	Q _C	Q _D
	2 (L)	1 (R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q _B [†]	Q _C [†]	Q _D [†]	d	Q _{Bn}	Q _{Cn}	Q _{Dn}	d
L	L	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
L	X	↓	H	X	X	X	X	H	Q _A n	Q _B n	Q _C n
L	X	↓	L	X	X	X	X	L	Q _A n	Q _B n	Q _C n
↑	L	L	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
↓	L	L	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
↓	L	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
↑	H	L	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
↑	H	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

[†]Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level

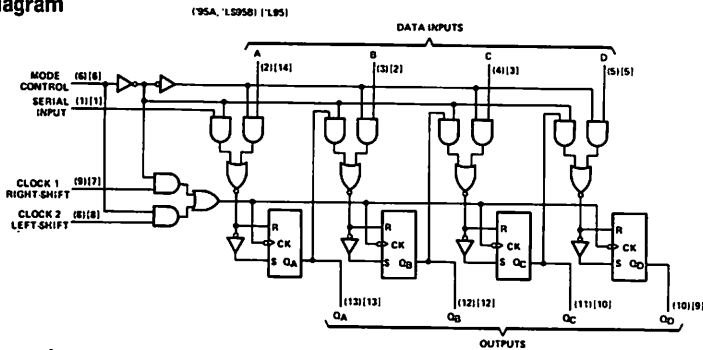
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the indicated steady-state input conditions were established.

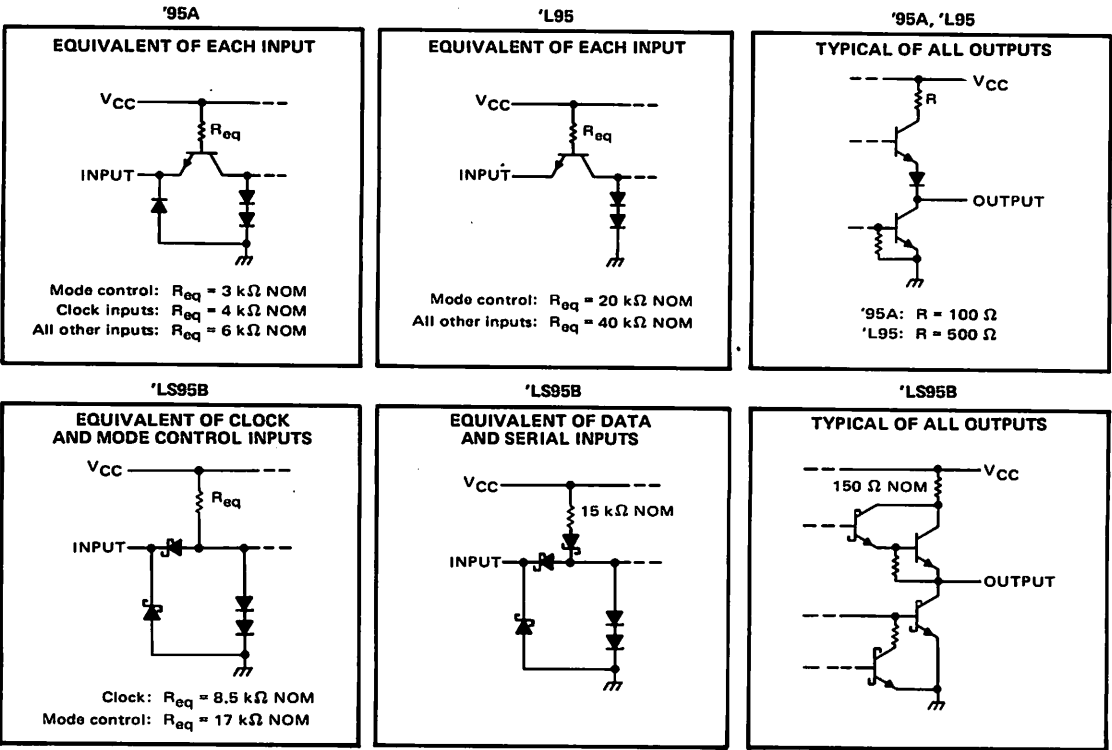
Q_{An} , Q_{Bn} , Q_{Cn} , Q_{Dn} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the most-recent ↓ transition of the clock.

TYPES SN5495A, SN54L95, SN54LS95B, SN7495A, SN74L95, SN74LS95B 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

functional block diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54'	SN54L'	SN54LS'	SN74'	SN74L'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	8	7	7	8	7	V
Input voltage (see Note 2)	5.5	5.5	7	5.5	5.5	7	V
Interemitter voltage (see Note 3)	5.5	5.5		5.5	5.5		V
Operating free-air temperature range	-55 to 125			0 to 70			°C
Storage temperature range	-65 to 150			-65 to 150			°C

- NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. For the 'L95, input voltages must be zero or positive with respect to network ground terminal.
3. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies between the clock-2 input and the mode control input.

TYPES SN5495A, SN7495A

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

REVISED MARCH 1974

recommended operating conditions

	SN5495A			SN7495A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 1)	20			20			ns
Setup time, high-level or low-level data, t_{setup} (see Figure 1)	15			15			ns
Hold time, high-level or low-level data, t_{hold} (see Figure 1)	0			0			ns
Time to enable clock 1, $t_{enable\ 1}$ (see Figure 2)	15			15			ns
Time to enable clock 2, $t_{enable\ 2}$ (see Figure 2)	15			15			ns
Time to inhibit clock 1, $t_{inhibit\ 1}$ (see Figure 2)	5			5			ns
Time to inhibit clock 2, $t_{inhibit\ 2}$ (see Figure 2)	5			5			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5495A			SN7495A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	High-level input current	Serial, A, B, C, D, Clock 1 or 2			40			40	μ A
		Mode control			80			80	
I_{IL}	Low-level input current	Serial, A, B, C, D, Clock 1 or 2			-1.6			-1.6	mA
		Mode control			-3.2			-3.2	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-18		-57	-18		-57	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 4}$		39	63		39	63	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 4: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	25	36		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock		18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		21	32	ns

$C_L = 15 \text{ pF}, R_L = 400 \Omega,$
See Figure 1

TYPES SN54L95, SN74L95
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

recommended operating conditions

	SN54L95			SN74L95			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	6.5	4.75	5	5.25	V
High-level output current, I_{OH}			-100			-200	μ A
Low-level output current, I_{OL}			2			3.6	mA
Clock frequency, f_{clock}	0		3	0		3	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 1)	200			200			ns
Setup time, high-level data, t_{setup} (see Figure 1)	100			100			ns
Setup time, low-level data, t_{setup} (see Figure 1)	120			120			ns
Hold time, high-level or low-level data, t_{hold} (see Figure 1)	0			0			ns
Time to enable clock 1, $t_{enable 1}$ (see Figure 2)	225			225			ns
Time to enable clock 2, $t_{enable 2}$ (see Figure 2)	200			200			ns
Time to inhibit clock 1, $t_{inhibit 1}$ (see Figure 2)	100			100			ns
Time to inhibit clock 2, $t_{inhibit 2}$ (see Figure 2)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54L95			SN74L95			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.7	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.7 \text{ V}, I_{OH} = \text{MAX}$	2.4	3.3		2.4	3.2		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.7 \text{ V}, I_{OL} = \text{MAX}$		0.15	0.3		0.2	0.4	V
I_I	Input current at maximum input voltage	Serial, A, B, C, D, Clock 1 or 2			100			100	μ A
		Mode control			200			200	
I_{IH}	High-level input current	Serial, A, B, C, D, Clock 1 or 2			10			10	μ A
		Mode control			20			20	
I_{IL}	Low-level input current	Serial, A, B, C, D, clock 1 or 2			-0.18			-0.18	mA
		Mode control			-0.36			-0.36	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-3		-15	-3		-15	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 4		3.8	9		3.8	9	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 4: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		3	5		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock	$C_L = 50 \text{ pF}, R_L = 4 \text{ k}\Omega$, See Figure 1		115	200	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			125	200	ns

TYPES SN54LS95B, SN74LS95B

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

recommended operating conditions

	SN54LS95B			SN74LS95B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 1)	25			25			ns
Setup time, high-level or low-level data, t_{setup} (see Figure 1)	20			20			ns
Hold time, high-level or low-level data, t_{hold} (see Figure 1)	10			10			ns
Time to enable clock 1, $t_{enable 1}$ (see Figure 2)	20			20			ns
Time to enable clock 2, $t_{enable 2}$ (see Figure 2)	20			20			ns
Time to inhibit clock 1, $t_{inhibit 1}$ (see Figure 2)	20			20			ns
Time to inhibit clock 2, $t_{inhibit 2}$ (see Figure 2)	20			20			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS95B			SN74LS95B			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I	Input current at maximum input voltage	Clock inputs			0.2			0.2	mA
		Other inputs			0.1			0.1	
I_{IH}	High-level input current	Clock inputs			40			40	μ A
		Other inputs			20			20	
I_{IL}	Low-level input current	Clock inputs			-0.8			-0.8	mA
		Other inputs			-0.4			-0.4	
I_{OS}	Short-circuit output current §	$V_{CC} = \text{MAX}$	-6		-40	-5		-42	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 4		13	21		13	21	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 4: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Figure 1	25	36		MHz
t_{PLH} Propagation delay time, low-to-high-level output from clock			18	27	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			21	32	ns

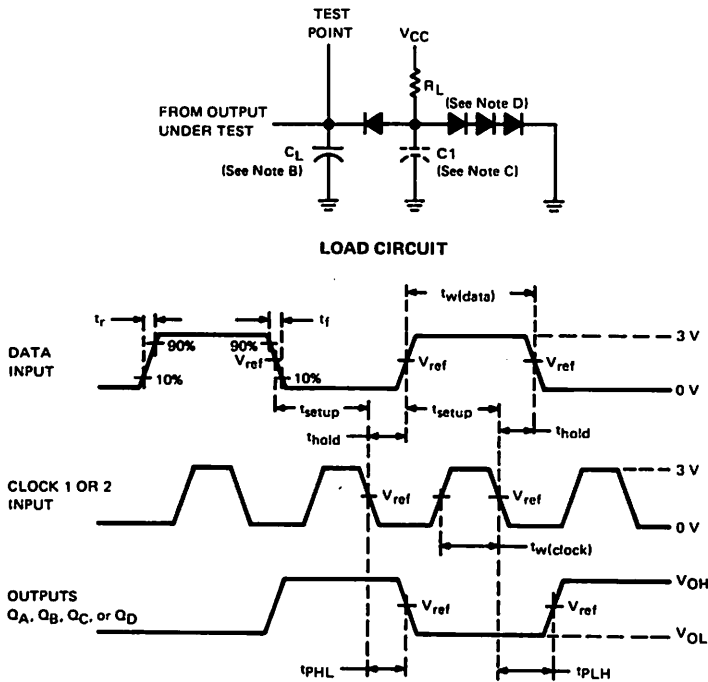
TENTATIVE DATA

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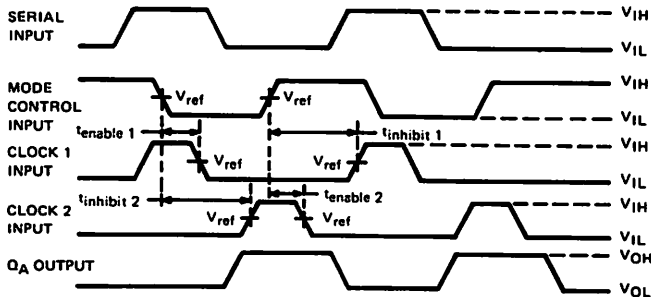
TYPES SN5495A, SN54L95, SN54LS95B, SN7495A, SN74L95, SN74LS95B
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, and $Z_{out} \approx 50 \Omega$. For the data pulse generator, PRR = 500 kHz; for the clock pulse generator, PRR = 1 MHz. When testing t_{max} , vary PRR. For '95A, $t_w(data) \geq 20$ ns; $t_w(clock) \geq 15$ ns. For 'L95, $t_w(data) \geq 150$ ns; $t_w(clock) \geq 200$ ns. For 'LS95B, $t_w(data) \geq 20$ ns, $t_w(clock) \geq 15$ ns.
- B. C_L includes probe and jig capacitance.
- C. C_1 (30 pF) is applicable for testing 'L95.
- D. All diodes are 1N916 or 1N3064.
- E. For '95A, $V_{ref} = 1.5$ V; for 'L95 and 'LS95B, $V_{ref} = 1.3$ V.

VOLTAGE WAVEFORMS
FIGURE 1—SWITCHING TIMES



- NOTES: A. Input A is at a low level.
- B. For '95A, $V_{ref} = 1.5$ V; for 'L95 and 'LS95B, $V_{ref} = 1.3$ V.

VOLTAGE WAVEFORMS
FIGURE 2—CLOCK ENABLE/INHIBIT TIMES

TYPES SN5496, SN54L96, SN54LS96, SN7496, SN74L96, SN74LS96 5-BIT SHIFT REGISTERS

BULLETIN NO. DL-S 7411821, MARCH 1974

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

TYPE	TYPICAL	
	PROPAGATION DELAY TIME	POWER DISSIPATION
'96	25 ns	240 mW
'L96	50 ns	120 mW
'LS96	25 ns	60 mW

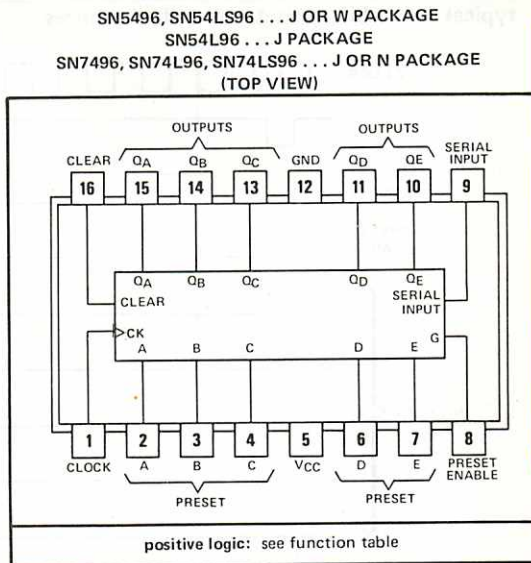
description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.



FUNCTION TABLE

CLEAR	PRESET ENABLE	INPUTS					CLOCK	SERIAL	OUTPUTS				
		A	B	C	D	E			QA	QB	QC	QD	QE
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	QA0	QB0	QC0	QD0	QE0
H	H	H	L	H	L	H	L	X	H	QB0	H	QD0	H
H	L	X	X	X	X	X	L	X	QA0	QB0	QC0	QD0	QE0
H	L	X	X	X	X	X	↑	H	H	QAn	QBn	QCn	QDn
H	L	X	X	X	X	X	↑	L	L	QAn	QBn	QCn	QDn

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

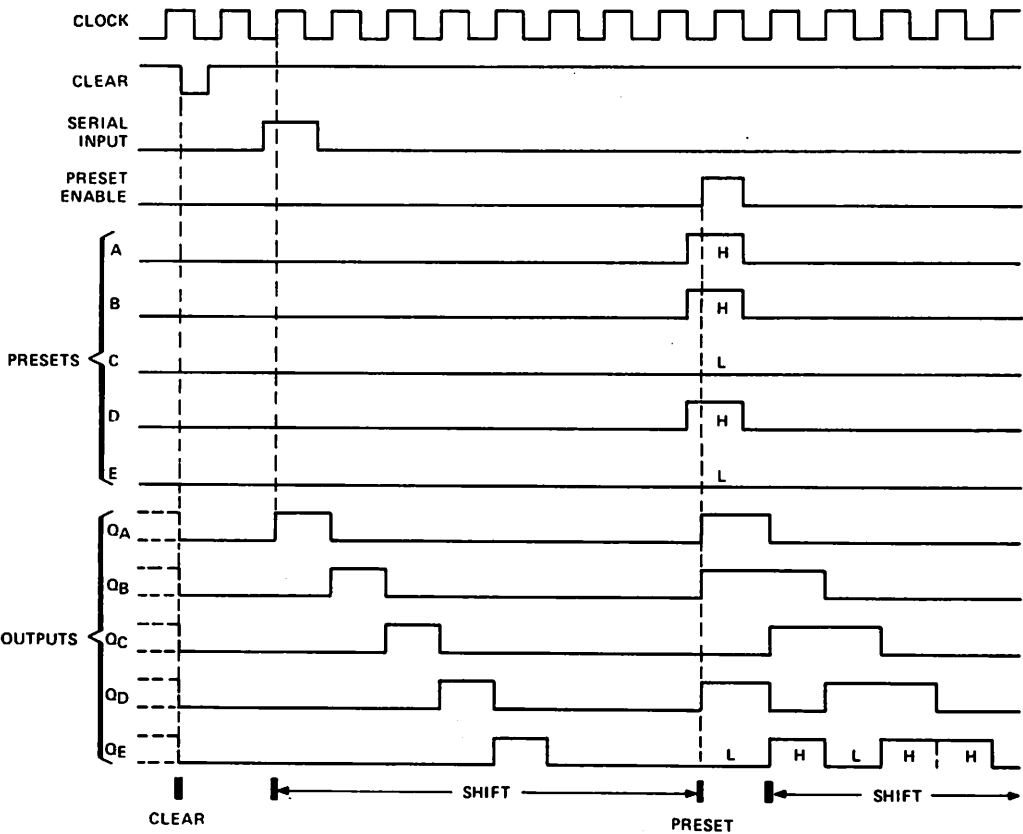
↑ = transition from low to high level

QA0, QB0, etc = the level of QA, QB, etc, respectively before the indicated steady-state input conditions were established.

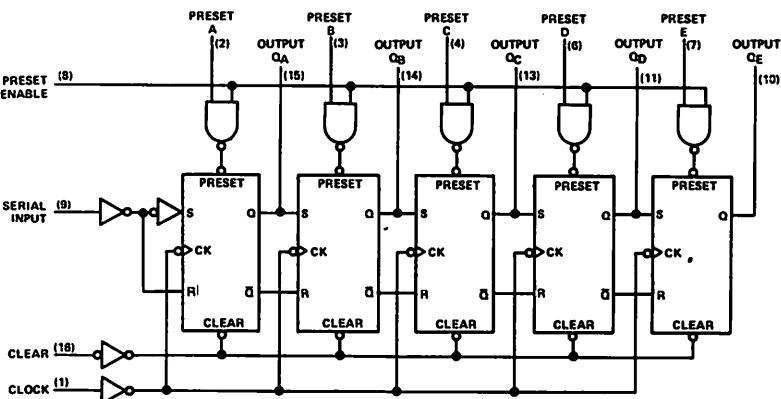
QAn, QBn, etc = the level of QA, QB, etc, respectively before the most-recent ↑ transition of the clock.

TYPES SN5496, SN54L96, SN54LS96, SN7496, SN74L96, SN74LS96 5-BIT SHIFT REGISTERS

typical clear, shift, preset, and shift sequences



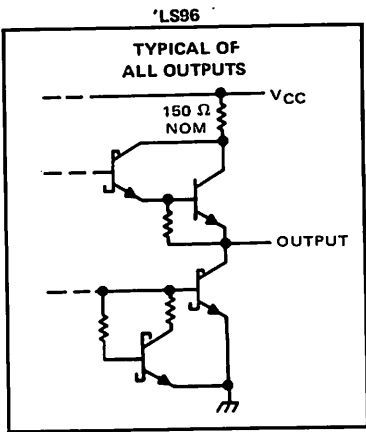
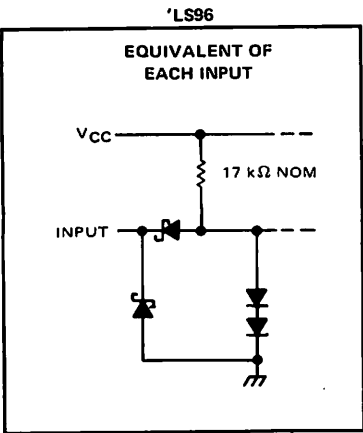
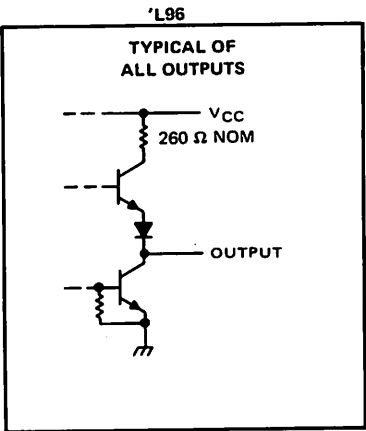
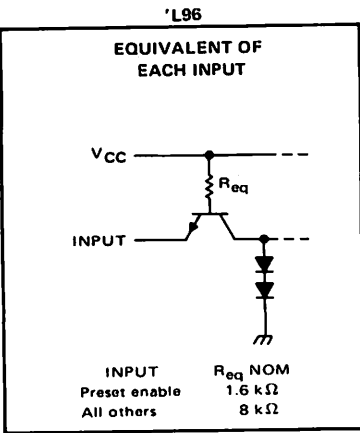
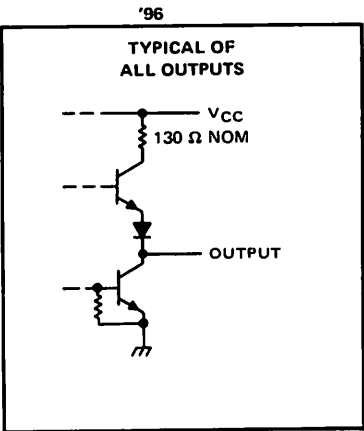
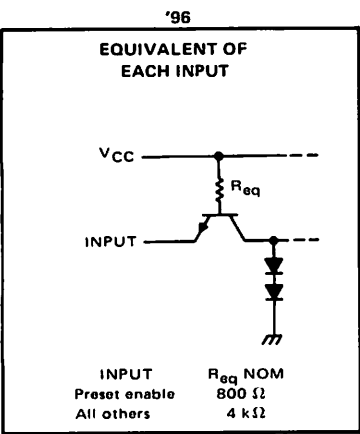
functional block diagram



... dynamic input activated by transition from a high level to a low level.

TYPES SN5496, SN54L96, SN54LS96, SN7496, SN74L96, SN74LS96 5-BIT SHIFT REGISTERS

schematics of inputs and outputs



TYPES SN5496, SN7496

5-BIT SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5496	-55°C to 125°C
SN7496	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN5496			SN7496			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		10	0		10	MHz
Width of clock input pulse, $t_w(\text{clock})$	35			35			ns
Width of preset and clear input pulse, t_w	30			30			ns
Serial input setup time, t_{setup} (see Figure 1)	30			30			ns
Serial input hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5496			SN7496			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	High-level input current	any input except preset enable			40			40	μ A
		preset enable			200			200	
I_{IL}	Low-level input current	any input except preset enable			-1.6			-1.6	mA
		preset enable			-8			-8	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-57	-18		-57	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 3		48	68		48	79	mA

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output from clock	$C_L = 15 \text{ pF}, R_L = 400 \Omega,$ See Figure 1		25	40	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			25	40	ns
t_{PLH} Propagation delay time, low-to-high-level output from preset or preset enable			28	35	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear				55	ns

TYPES SN54L96, SN74L96

5-BIT SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54L96	-55°C to 125°C
SN74L96	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN54L96			SN74L96			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-200			-200	μ A
Low-level output current, I_{OL}			8			8	mA
Clock frequency, f_{clock}	0		5	0		5	MHz
Width of clock, preset, or clear input pulse, t_W	100			100			ns
Serial input setup time, t_{setup} (see Figure 1)	100			100			ns
Serial input hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54L96			SN74L96			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -200 \mu\text{A}$	2.4	3.2		2.4	3.2		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 8 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	High-level input current	any input except preset enable			20			20	μ A
		preset enable			100			100	
		preset enable							
I_{IL}	Low-level input current	any input except preset enable			-0.8			-0.8	mA
		preset enable			-4			-4	
		preset enable							
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-10		-29	-9		-29	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 3}$	24		34	24		40	mA

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output from clock	$C_L = 15 \text{ pF}, R_L = 800 \Omega, \text{ See Figure 1}$		50	80	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			50	80	ns
t_{PLH} Propagation delay time, low-to-high-level output from preset or preset enable			56	70	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear				110	ns

TYPES SN54LS96, SN74LS96

5-BIT SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS96	-55°C to 125°C
SN74LS96	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS96			SN74LS96			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		10	0		10	MHz
Width of clock input pulse, $t_{w(\text{clock})}$	35			35			ns
Width of preset and clear input pulse, t_w	30			30			ns
Serial input setup time, t_{setup} (see Figure 1)	30			30			ns
Serial input hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS96		SN74LS96		UNIT
		MIN	TYP‡ MAX	MIN	TYP‡ MAX	
V_{IH} High-level input voltage		2		2		V
V_{IL} Low-level input voltage			0.7		0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5		-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}, I_{OH} = -400 \mu\text{A}$	2.5	3.5	2.7	3.5	V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}$	0.25	0.4	0.25	0.4	V
	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$			0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1		0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20		20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4		-0.4	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-6	-40	-5	-42	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 3}$	12	20	12	20	mA

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output from clock	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ See Figure 1}$		25	40	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			25	40	ns
t_{PLH} Propagation delay time, low-to-high-level output from preset or preset enable			28	35	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear				55	ns

TENTATIVE DATA

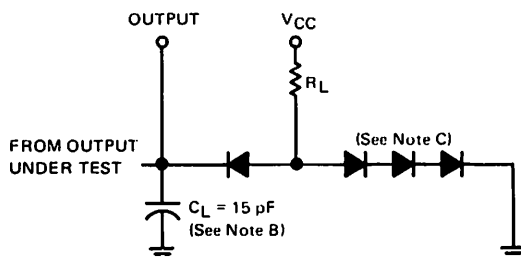
S-152

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

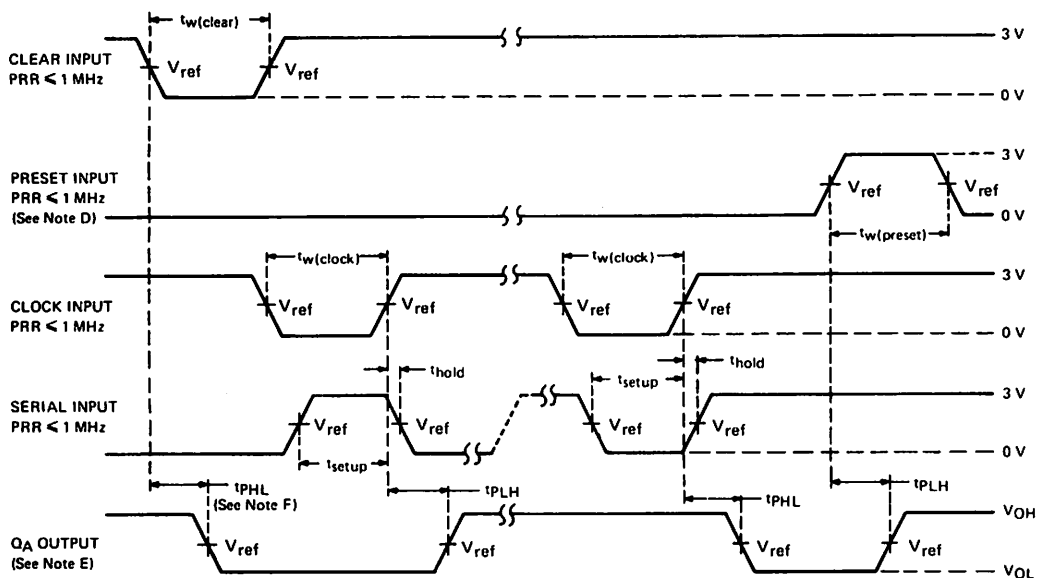
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TYPES SN5496, SN54L96, SN54LS96, SN7496, SN74L96, SN74LS96 5-BIT SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. Input pulses are supplied by pulse generators having the following characteristics: duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$; for '96 and 'L96, $t_r \leq 10$ ns, $t_f \leq 10$ ns, and for 'LS96 $t_r = 15$ ns, $t_f = 6$ ns.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or 1N916.
- D. Preset may be tested by applying a high-level voltage to the individual preset inputs and pulsing the preset enable or by applying a high-level voltage to the preset enable and pulsing the individual preset inputs.
- E. Q_A output is illustrated. Relationship of serial input to other Q outputs is illustrated in the typical shift sequence.
- F. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
- G. For '96 and 'L96, $V_{ref} = 1.5$ V; for 'LS96 $V_{ref} = 1.3$ V.

FIGURE 1—SWITCHING TIMES

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S-153

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

- Full Decoding of Input Logic
- SN54145, SN74145, and SN74LS145 Have 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions
- Low Power Dissipation of 'LS145 ... 35 mW Typical

logic

FUNCTION TABLE

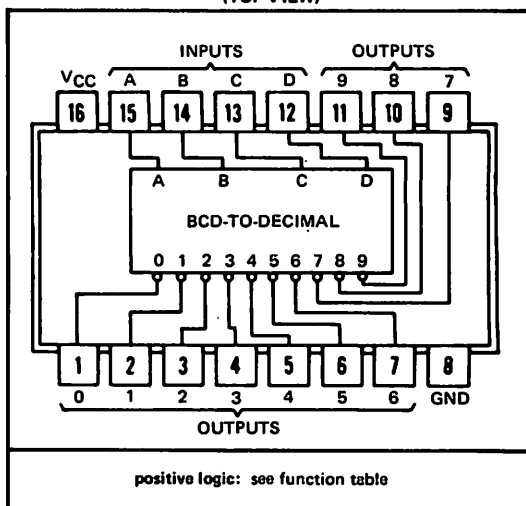
NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)

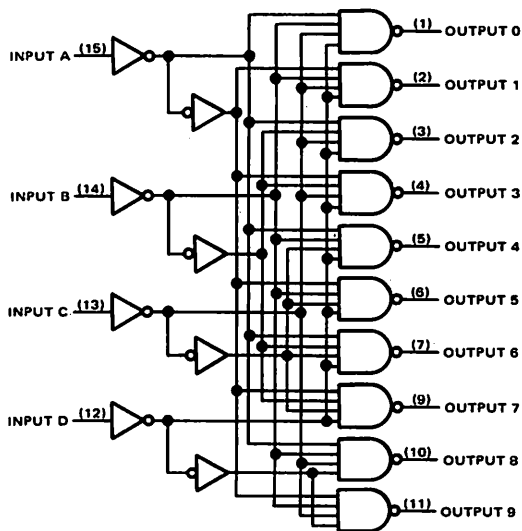
description

These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (15 volts) of the SN54145, SN74145, or SN74LS145 will sink up to 80 milliamperes of current. Each input is one Series 54/74 or Series 54LS/74LS standard load, respectively. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts for the '145 and 35 milliwatts for the 'LS145.

SN54145, SN54LS145 ... J OR W PACKAGE
SN74145, SN74LS145 ... J OR N PACKAGE
(TOP VIEW)



functional block diagram



TYPES SN54145, SN74145
BCD-TO-DECIMAL DECODERS/DRIVERS

REVISED MARCH 1974

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Maximum current into any output (off-state)	1 mA
Operating free-air temperature range: SN54145	-55°C to 125°C
SN74145	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54145			SN74145			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$			15			15	V
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
$I_{O(off)}$ Off-state output current	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $V_{O(off)} = 15 \text{ V}$			250	μA
$V_{O(on)}$ On-state output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$	$I_{O(on)} = 80 \text{ mA}$ $I_{O(on)} = 20 \text{ mA}$	0.5	0.9	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	SN54145 SN74145	43 43	62 70	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

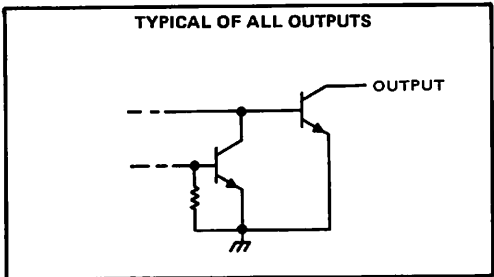
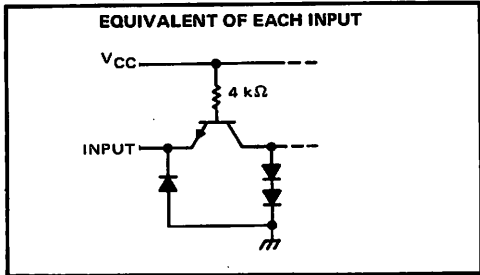
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$, $R_L = 100 \Omega$, See Note 3		50	ns
t_{PHL} Propagation delay time, high-to-low-level output			50	ns

NOTE 3: Load circuit and waveforms are shown on page S-87.

schematics of inputs and outputs



TYPES SN54LS145, SN74LS145
BCD-TO-DECIMAL DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS145	-55°C to 125°C
SN74LS145	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS145			SN74LS145			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$			15			15	V
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS145			SN74LS145			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
$I_{O(off)}$ Off-state output current	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $V_{OH} = 15 \text{ V}$			250			250	μA
$V_{O(on)}$ On-state output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4	$I_{OL} = 12 \text{ mA}$	0.25	0.4	V
		$I_{OL} = 24 \text{ mA}$			$I_{OL} = 24 \text{ mA}$	0.35	0.5	
		$I_{OL} = 80 \text{ mA}$			$I_{OL} = 80 \text{ mA}$	1.5	1.7	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	7		13	7		13	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

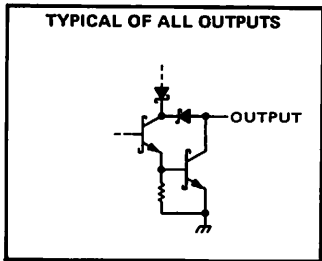
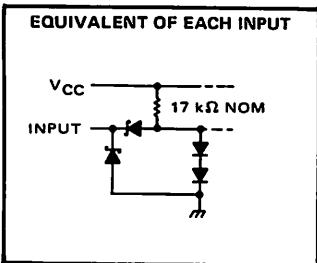
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 45 \text{ pF}$, $R_L = 665 \Omega$, See Note 4		50	ns
t_{PHL} Propagation delay time, high-to-low-level output			50	ns

NOTE 4: Load circuit and waveforms are shown on page S-88.

schematic of inputs and outputs



TENTATIVE DATA

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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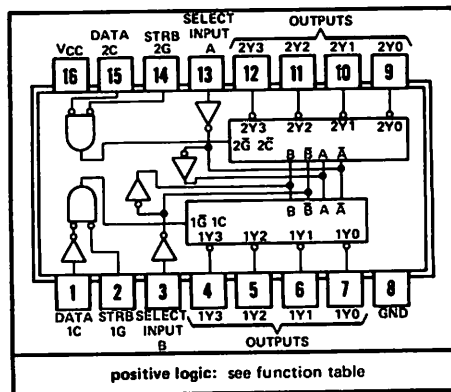
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TYPES SN54155, SN54156, SN54LS155, SN54LS156, SN74155, SN74156, SN74LS155, SN74LS156 DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

BULLETIN NO. DL-S 7411850, MARCH 1974

- Applications:
Dual 2-to-4-Line Decoder
Dual 1-to-4-Line Demultiplexer
3-to-8-Line Decoder
1-to-8-Line Demultiplexer
- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Input Clamping Diodes Simplify System Design
- Choice of Outputs:
Totem Pole ('155, 'LS155)
Open-Collector ('156, 'LS156)

SN54155, SN54156, SN54LS155, SN54LS156 ... J OR W PACKAGE
SN74155, SN74156, SN74LS155, SN74LS156 ... J OR N PACKAGE
(TOP VIEW)



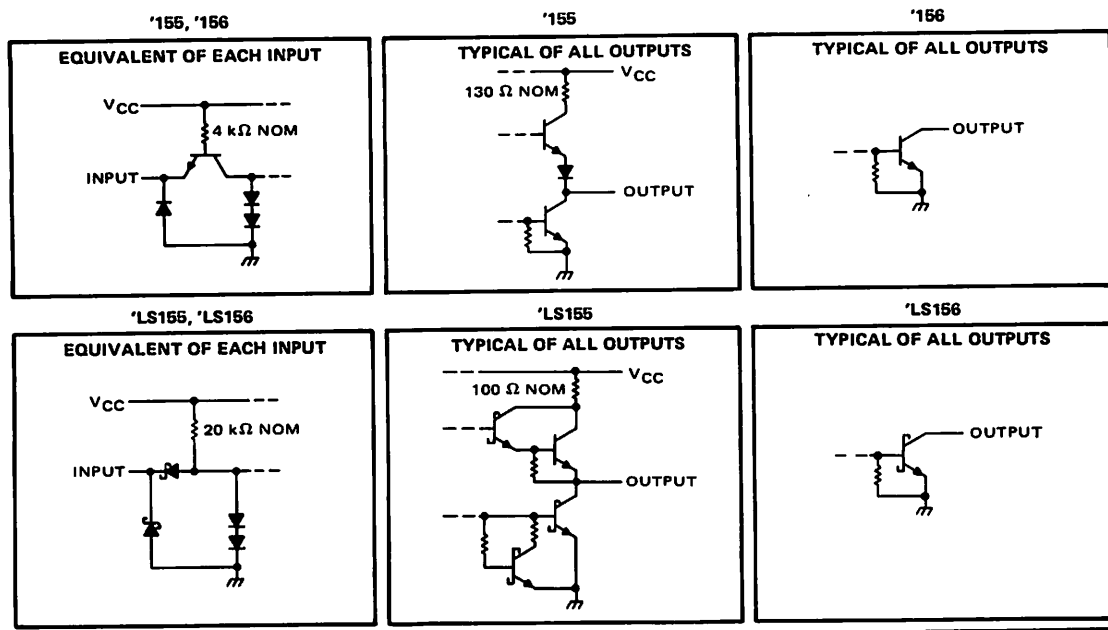
TYPES	TYPICAL AVERAGE PROPAGATION DELAY 3 GATE LEVELS	TYPICAL POWER DISSIPATION
'155, '156	21 ns	125 mW
'LS155	18 ns	31 mW
'LS156	32 ns	31 mW

description

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

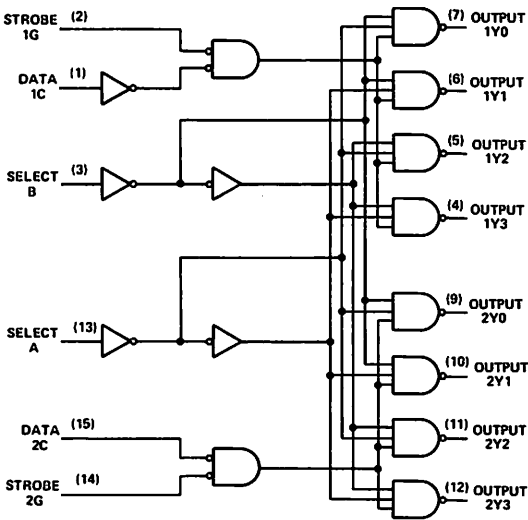
Series 54 and 54LS are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74 and 74LS are characterized for operation from 0°C to 70°C .

schematics of inputs and outputs



TYPES SN54155, SN54156, SN54LS155, SN54LS156,
SN74155, SN74156, SN74LS155, SN74LS156
DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

functional block diagram and logic



FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT		STROBE OR DATA		(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = Inputs 1C and 2C connected together

‡G = inputs 1G and 2G connected together

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '155, '156	5.5 V
'LS155, 'LS156	7 V
Off-state output voltage: '155	5.5 V
'LS155	7 V
Operating free-air temperature range: SN54', SN54LS' Circuits	-55°C to 125°C
SN74', SN74LS' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54155, SN74155

DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

recommended operating conditions

	SN54155			SN74155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}C$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER*	TEST CONDITIONS†	SN54155 SN74155			UNIT
		MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2		V
V_{IL} Low-level input voltage				0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu A$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	SN54155	-20	-55	mA
		SN74155	-18	-57	
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2	SN54155	25	35	mA
		SN74155	25	40	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	$C_L = 15 \text{ pF},$ $R_L = 400 \Omega,$ See Note 3		13	20	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2			18	27	ns
t_{PLH}	A or B	Y	3			21	32	ns
t_{PHL}	A or B	Y	3			21	32	ns
t_{PLH}	1C	Y	3			16	24	ns
t_{PHL}	1C	Y	3			20	30	ns

¶ t_{PLH} \equiv propagation delay time, low-to-high-level output

t_{PHL} \equiv propagation delay time, high-to-low-level output

NOTE 3: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54LS155, SN74LS155

DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

recommended operating conditions

	SN54LS155			SN74LS155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS155			SN74LS155			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$							V
	$I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		
	$I_{OL} = 8 \text{ mA}$				0.35	0.5		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.36			-0.36	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-6		-40	-5		-42	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	6.1	10		6.1	10		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54LS155 SN74LS155			UNIT
					MIN	TYP	MAX	
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ See Note 4}$	10	15		ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2		19	30		ns
t_{PLH}	A or B	Y	3		17	26		ns
t_{PHL}	A or B	Y	3		19	30		ns
t_{PLH}	1C	Y	3		18	27		ns
t_{PHL}	1C	Y	3		18	27		ns

¶ $t_{PLH} \equiv$ propagation delay time, low-to-high-level output

$t_{PHL} \equiv$ propagation delay time, high-to-low-level output

NOTE 4: Load circuit and voltage waveforms are shown on page S-88.

TYPES SN54156, SN74156
DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

recommended operating conditions

	SN54156			SN74156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54156 SN74156		UNIT	
			MIN	TYP‡ MAX		
V _{IH}	High-level input voltage		2		V	
V _{IL}	Low-level input voltage		0.8		V	
V _I	Input clamp voltage	V _{CC} = MIN, I _I = −12 mA	−1.5		V	
I _{OH}	High-level output current	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, V _{OH} = 5.5 V	250		µA	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA	0.2	0.4	V	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V	1		mA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.4 V	40		µA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V	−1.6		mA	
I _{CC}	Supply current	V _{CC} = MAX, See Note 2	SN54156	25	35	mA
		SN74156	25	40		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	$C_L = 15 \text{ pF},$ $R_L = 400 \Omega,$ See Note 3		15	23	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2			20	30	ns
t_{PLH}	A or B	Y	3			23	34	ns
t_{PHL}	A or B	Y	3			23	34	ns
t_{PLH}	1C	Y	3			18	27	ns
t_{PHL}	1C	Y	3			22	33	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54LS156, SN74LS156
DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

recommended operating conditions

	SN54LS156			SN74LS156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS156			SN74LS156			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$			100			100	µA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}$			$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$			$0.25, 0.4$ $0.25, 0.4$ $0.35, 0.5$	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.36			-0.36	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2			6.1 10			6.1 10	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54LS156 SN74LS156			UNIT
					MIN	TYP	MAX	
t_{PLH}	A, B, 2C 1G, or 2G	Y	2	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega,$ See Note 4	18	27		ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2		34	51		ns
t_{PLH}	A or B	Y	3		31	46		ns
t_{PHL}	A or B	Y	3		34	51		ns
t_{PLH}	1C	Y	3		32	48		ns
t_{PHL}	1C	Y	3		32	48		ns

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: Load circuit and voltage waveforms are shown on page S-88.

TENTATIVE DATA

PRINTED IN U.S.A.

TYPES SN54157, SN54L157, SN54LS157, SN54LS158, SN54S157, SN54S158, SN74157, SN74L157, SN74LS157, SN74LS158, SN74S157, SN74S158 QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7411847, MARCH 1974

features

- Buffered Inputs and Outputs
- Three Speed/Power Ranges Available

TYPES	TYPICAL AVERAGE PROPAGATION TIME	TYPICAL POWER DISSIPATION
'157	9 ns	150 mW
'L157	18 ns	75 mW
'LS157	9 ns	49 mW
'S157	5 ns	250 mW
'LS158	7 ns	24 mW
'S158	4 ns	195 mW

applications

- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variable Is Common)
- Source Programmable Counters

description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'L157, 'LS157, and 'S157 present true data whereas the 'LS158 and 'S158 present inverted data to minimize propagation delay time.

FUNCTION TABLE

INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	'157, 'L157, 'LS157, 'S157	'LS158, 'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

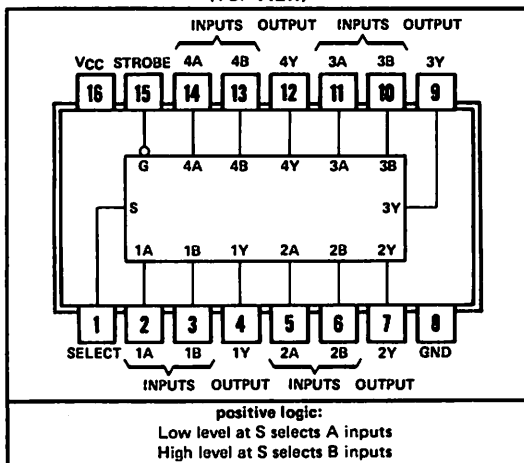
H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

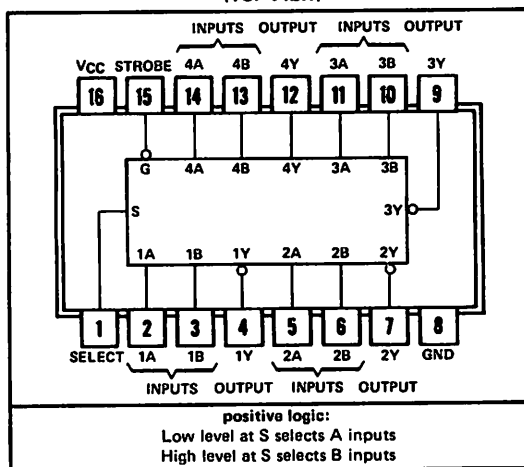
Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage: '157, 'L157, 'S158	5.5 V
'LS157, 'LS158	7 V
Operating free-air temperature range: SN54', SN54L', SN54LS', SN54S' Circuits	-55°C to 125°C
SN74', SN74L', SN74LS', SN74S' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN54157, SN54LS157, SN54S157 ... J OR W PACKAGE
SN54L157 ... J PACKAGE
SN74157, SN74L157, SN74LS157, SN74S157 ... J OR N PACKAGE
(TOP VIEW)



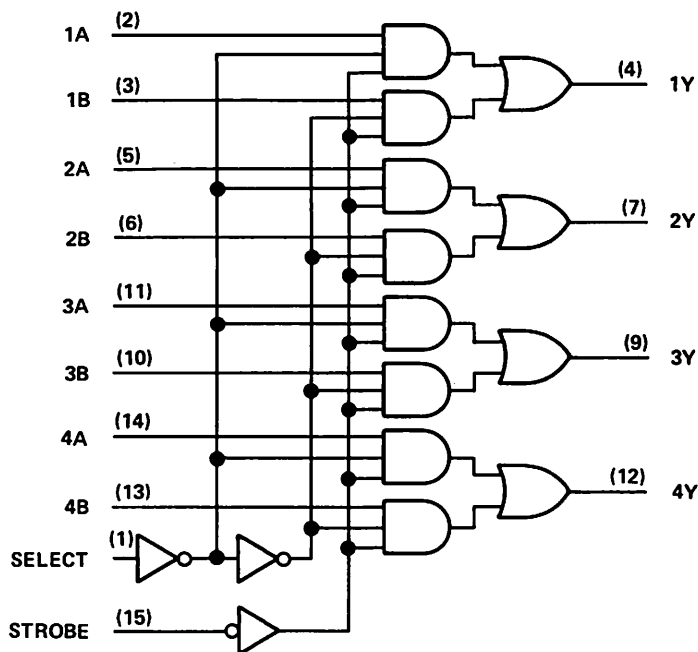
SN54LS158, SN54S158 ... J OR W PACKAGE
SN74LS158, SN74S158 ... J OR N PACKAGE
(TOP VIEW)



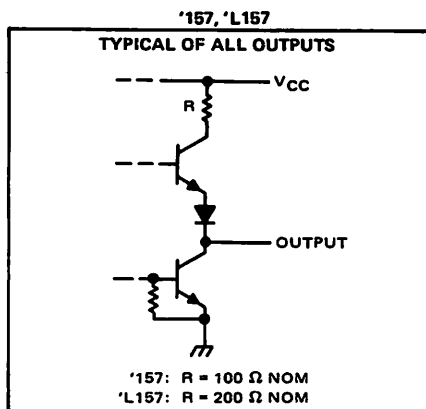
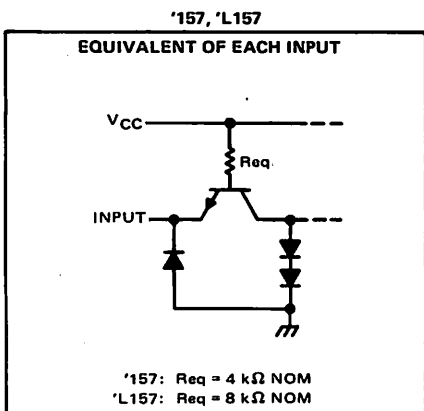
TYPES SN54157, SN54L157, SN74157, SN74L157, QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

functional block diagram

'157, 'L157

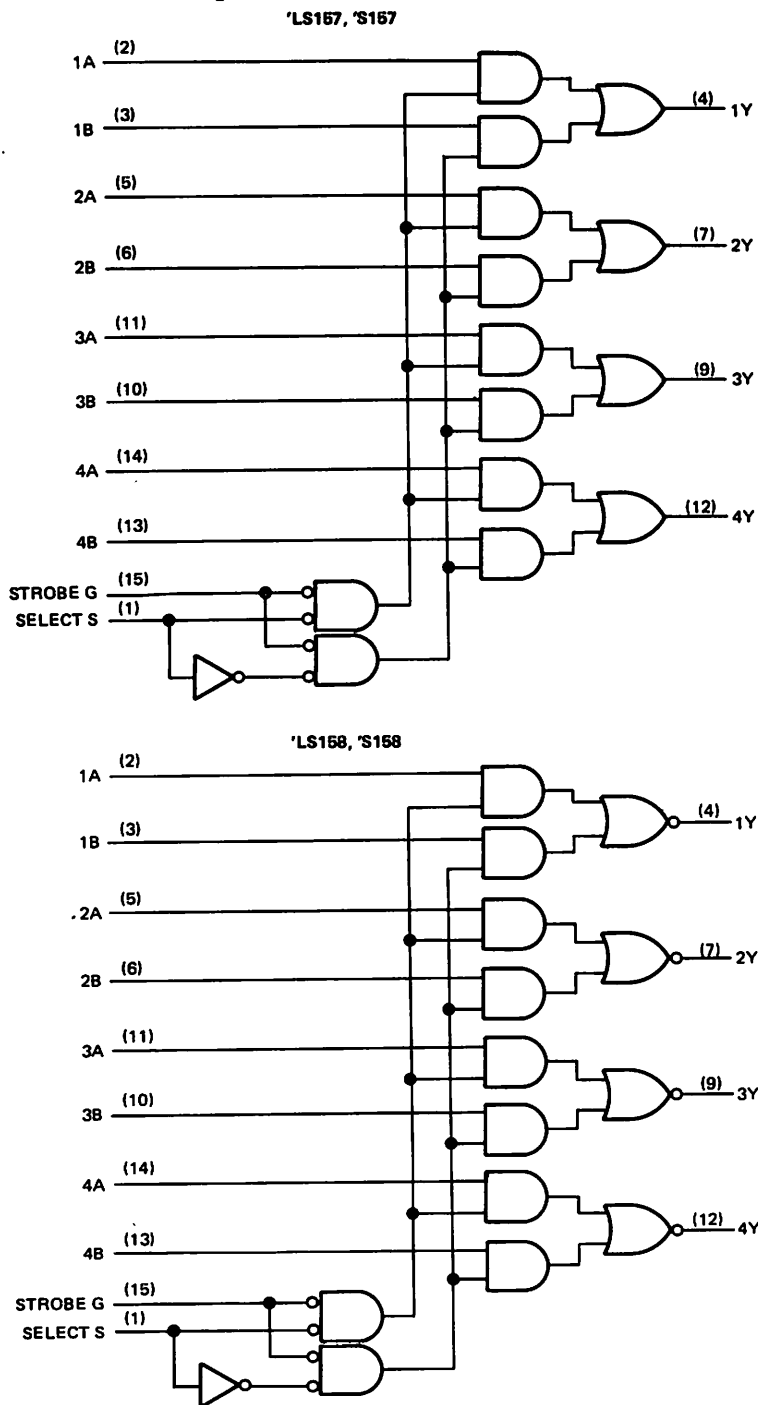


schematics of inputs and outputs

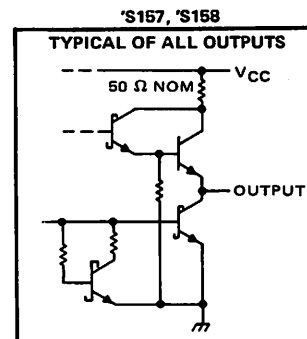
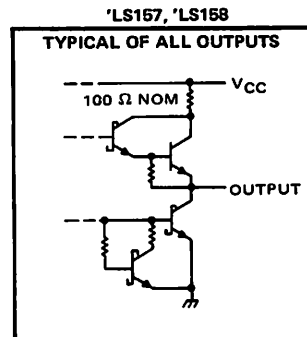
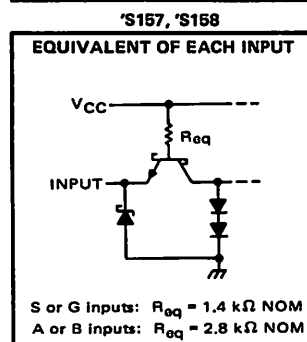
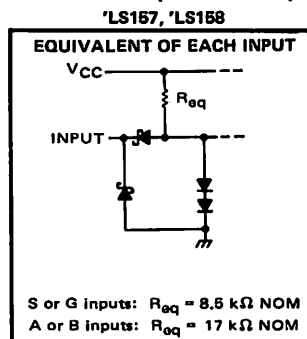


TYPES SN54LS157, SN54LS158, SN54S157, SN54S158, SN74LS157, SN74LS158, SN74S157, SN74S158 **QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS**

functional block diagrams



schematics of inputs and outputs



TYPES SN54157, SN74157

QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54157			SN74157			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54157			SN74157			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20	-55		-18	-55		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		30	48		30	48	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER [¶]	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Data	C _L = 15 pF, R _L = 400 Ω, See Note 3	9	14	ns	
t _{PHL}			9	14		
t _{PLH}	Strobe		13	20	ns	
t _{PHL}			14	21		
t _{PLH}	Select		15	23	ns	
t _{PHL}			18	27		

¶ $t_{PLH} \equiv$ propagation delay time, low-to-high-level output

$t_{PHL} \equiv$ propagation delay time, high-to-low-level output

NOTE 3: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54L157, SN74L157

QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54L157			SN74L157			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			8			8	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 8 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.8	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-9		-28	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		15	24	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER [¶]	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Data	C _L = 15 pF, R _L = 800 Ω, See Note 3	18	28		ns
t _{PHL}			18	28		
t _{PLH}	Strobe		26	40		ns
t _{PHL}			28	42		
t _{PLH}	Select		30	46		ns
t _{PHL}			36	54		

[¶] t_{PLH} \equiv propagation delay time, low-to-high-level output

t_{PHL} \equiv propagation delay time, high-to-low-level output

NOTE 3: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54LS157, SN54LS158, SN74LS157, SN74LS158

QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54LS ¹			SN74LS ¹			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN54LS ¹			SN74LS ¹			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
					$I_{OL} = 8 \text{ mA}$		0.35	0.5	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.2			0.2		mA
				0.1			0.1		
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		40			40		μ A
				20			20		
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.8			-0.8		mA
				-0.4			-0.4		
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-6	-40		-5	-42		mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		'LS157	9.7	16		'LS158	mA
					4.8	8			

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER [¶]	FROM (INPUT)	TEST CONDITIONS	'LS157			'LS158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	Data	C _L = 15 pF, R _L = 2 kΩ, See Note 4	9	14		7	12	ns	
t _{PHL}			9	14		7	12		
t _{PLH}	Strobe		13	20		11	17	ns	
t _{PHL}			14	21		12	18		
t _{PLH}	Select		15	23		13	20	ns	
t _{PHL}			18	27		16	24		

[¶] $t_{PLH} \equiv$ propagation delay time, low-to-high-level output

$t_{PHL} \equiv$ propagation delay time, high-to-low-level output

NOTE 4: Load circuit and voltage waveforms are shown on page S-88.

TENTATIVE DATA

S-168 This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TEXAS INSTRUMENTS
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TYPES SN54S157, SN54S158, SN74S157, SN74S158

QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54S157 SN54S158			SN74S157 SN74S158			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN54S157 SN74S157		SN54S158 SN74S158		UNIT
			MIN	TYP [‡] MAX	MIN	TYP [‡] MAX	
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.2		-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	Series 54S 2.5	3.4	Series 74S 2.5	3.4	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$		0.5		0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1		1	mA
I_{IH}	High-level input current	S or G input $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		100		100	μA
		A or B input		50		50	
I_{IL}	Low-level input current	S or G input $V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$		-4		-4	mA
		A or B input		-2		-2	
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-40	-100	-40	-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2	50	78	39	61	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

[§]Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER [†]	FROM (INPUT)	TEST CONDITIONS	SN54S157 SN74S157		SN54S158 SN74S158		UNIT
			MIN	TYP MAX	MIN	TYP MAX	
t _{PLH}	Data	C _L = 15 pF, R _L = 280 Ω, See Note 3	5	7.5	4	6	ns
t _{PHL}			4.5	6.5	4	6	
t _{PLH}	Strobe		8.5	12.5	6.5	11.5	ns
t _{PHL}			7.5	12	7	12	
t _{PLH}	Select		9.5	15	8	12	ns
t _{PHL}			9.5	15	8	12	

[¶] $t_{PLH} \equiv$ propagation delay time, low-to-high-level output

$t_{PHL} \equiv$ propagation delay time, high-to-low-level output

NOTE 3: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54160 THRU SN54163, SN54LS160 THRU SN54LS163, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160 THRU SN74LS163, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

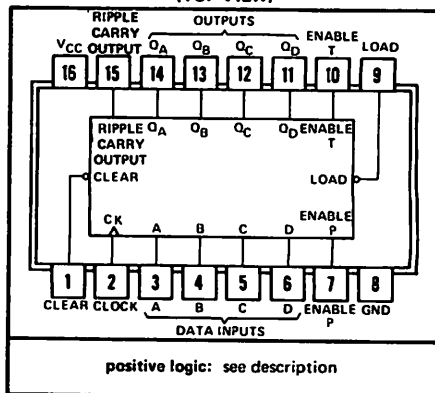
BULLETIN NO. DL-S 7411385, MARCH 1974

'160, '161, 'LS160, 'LS161 ... SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
'162, '163, 'LS162, 'LS163, 'S162, 'S163 ... FULLY SYNCHRONOUS COUNTERS

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

SERIES 54, 54LS, 54S ... J OR W PACKAGE
SERIES 74, 74LS, 74S ... J OR N PACKAGE

(TOP VIEW)



TYPE	TYPICAL PROPAGATION TIME, CLOCK TO Q OUTPUT	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'160 thru '163	14 ns	32 MHz	305 mW
'LS160 thru 'LS163	14 ns	32 MHz	93 mW
'S162 and 'S163	9 ns	70 MHz	475 mW

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160, '162, 'LS160, 'LS162, and 'S162 are decade counters and the '161, '163, 'LS161, 'LS163, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160 thru 'LS163, or 'S162 and 'S163. The clear function for the '160, '161, 'LS160, and 'LS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162, '163, 'LS162, 'LS163, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the QA output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160 thru 'LS163 or 'S162 and 'S163 are allowed regardless of the level of the clock input.

'LS160 thru 'LS163, 'S162 and 'S163 feature a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

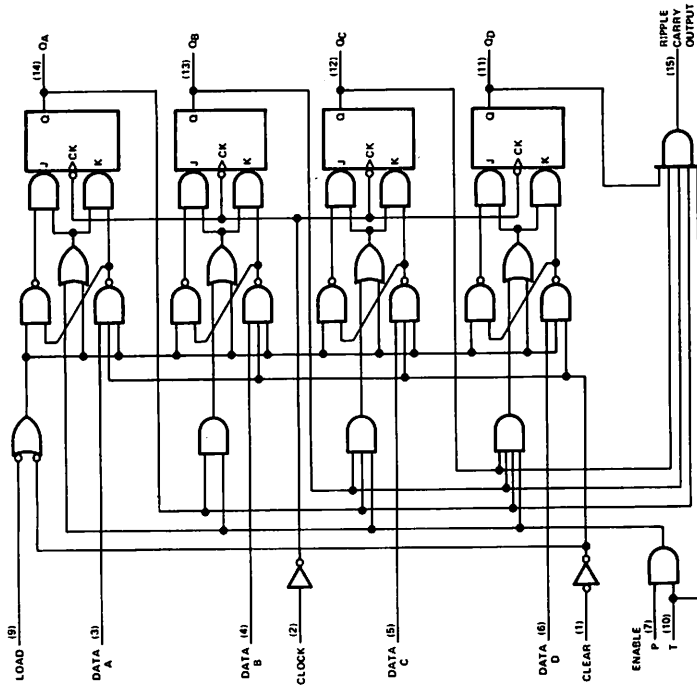
Series 54, Series 54LS, and Series 54S circuits are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74, Series 74LS, and Series 74S circuits are characterized for operation from 0°C to 70°C.

TYPES SN54160 THRU SN54163, SN74160 THRU SN74163 SYNCHRONOUS 4-BIT COUNTERS

functional block diagrams

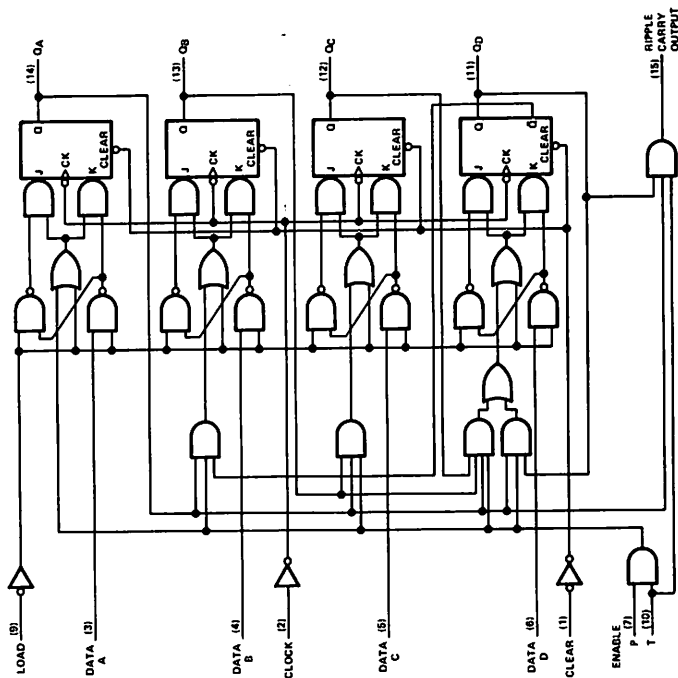
SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.



SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

SN54162, SN74162 synchronous decade counters are similar; however the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.

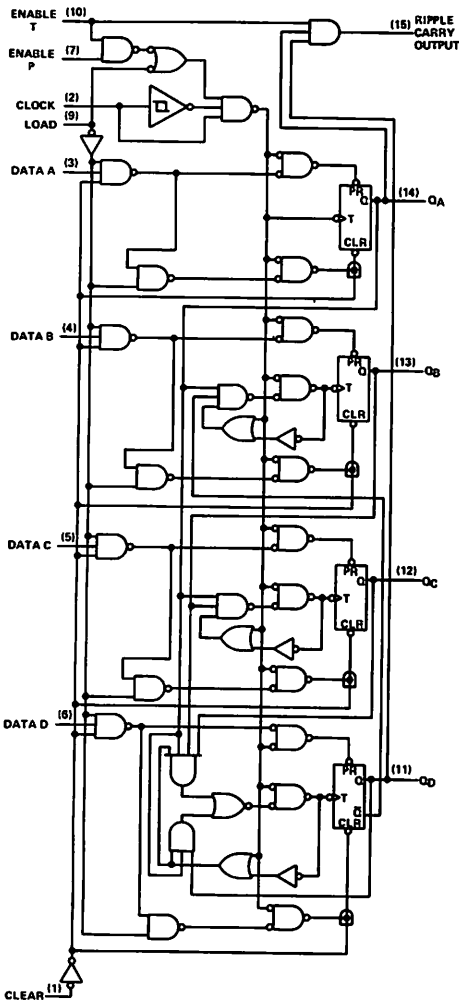


TYPES SN54LS160 THRU SN54LS163, SN74LS160 THRU SN74LS163 SYNCHRONOUS 4-BIT COUNTERS

functional block diagram

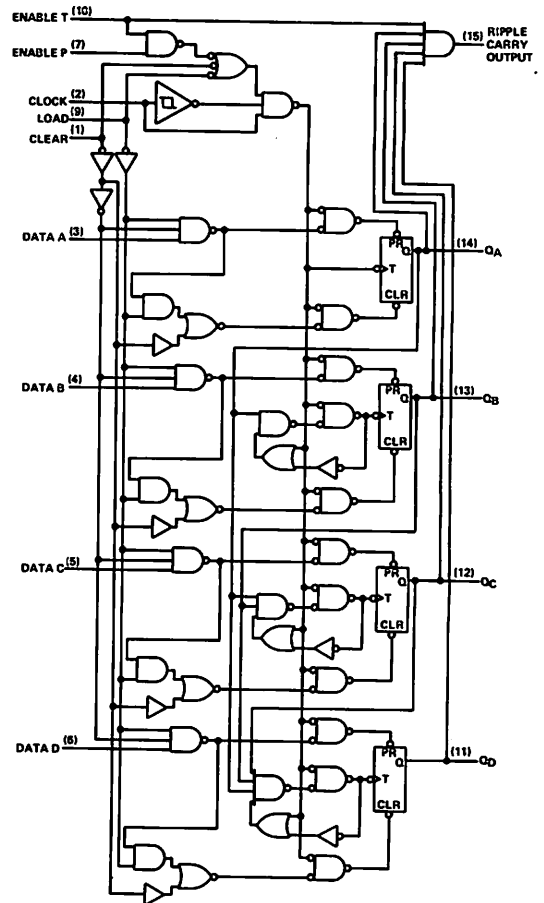
SN54LS160, SN74LS160 SYNCHRONOUS DECADE COUNTERS

SN54LS162, SN74LS162 synchronous decade counters are similar; however the clear is synchronous as shown for the SN54LS163, SN74LS163 binary counters at right.



SN54LS163, SN74LS163 SYNCHRONOUS BINARY COUNTERS

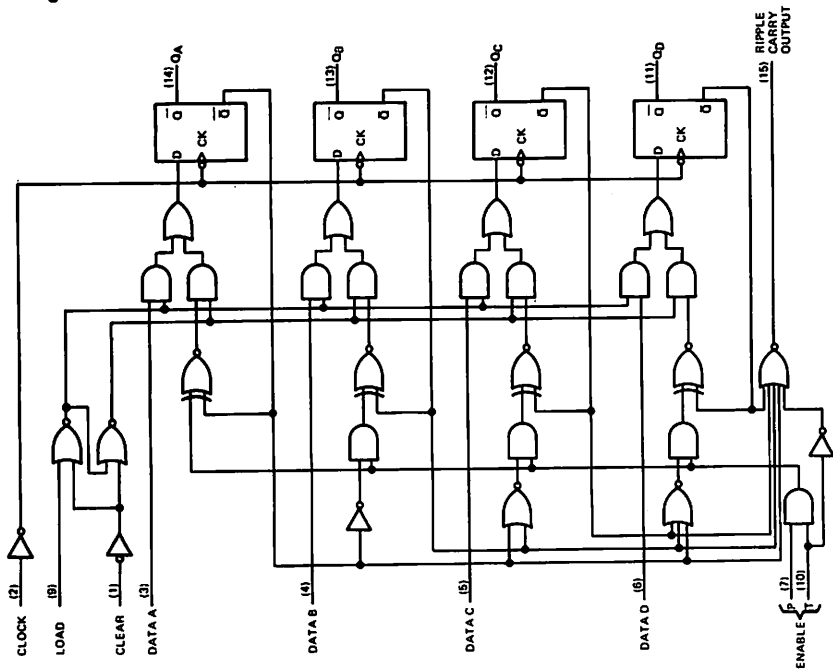
SN54LS161, SN74LS161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54LS160, SN74LS160 decade counters at left.



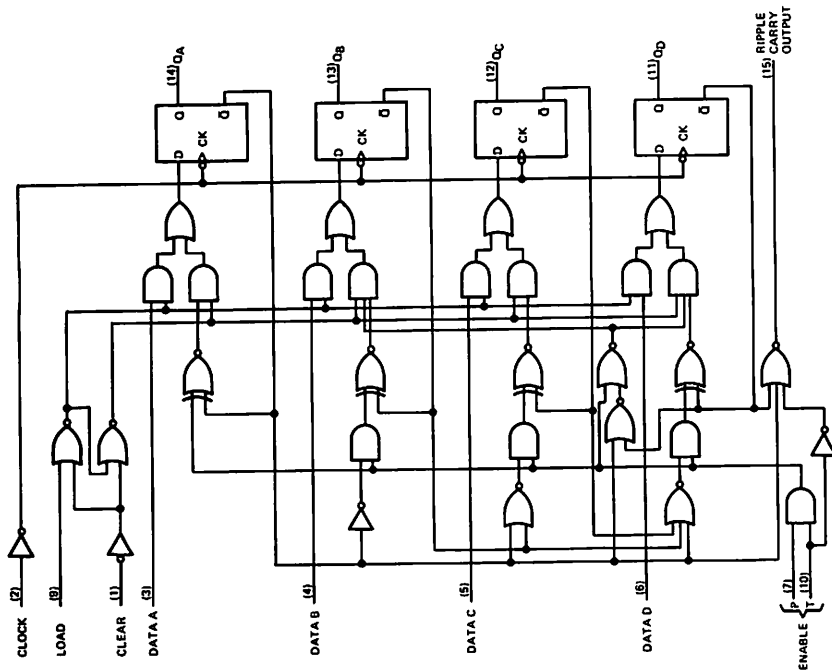
TYPES SN54S162, SN54S163, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

functional block diagrams

SN54S163, SN74S163 SYNCHRONOUS BINARY COUNTERS



SN54S162, SN74S162 SYNCHRONOUS DECADE COUNTERS



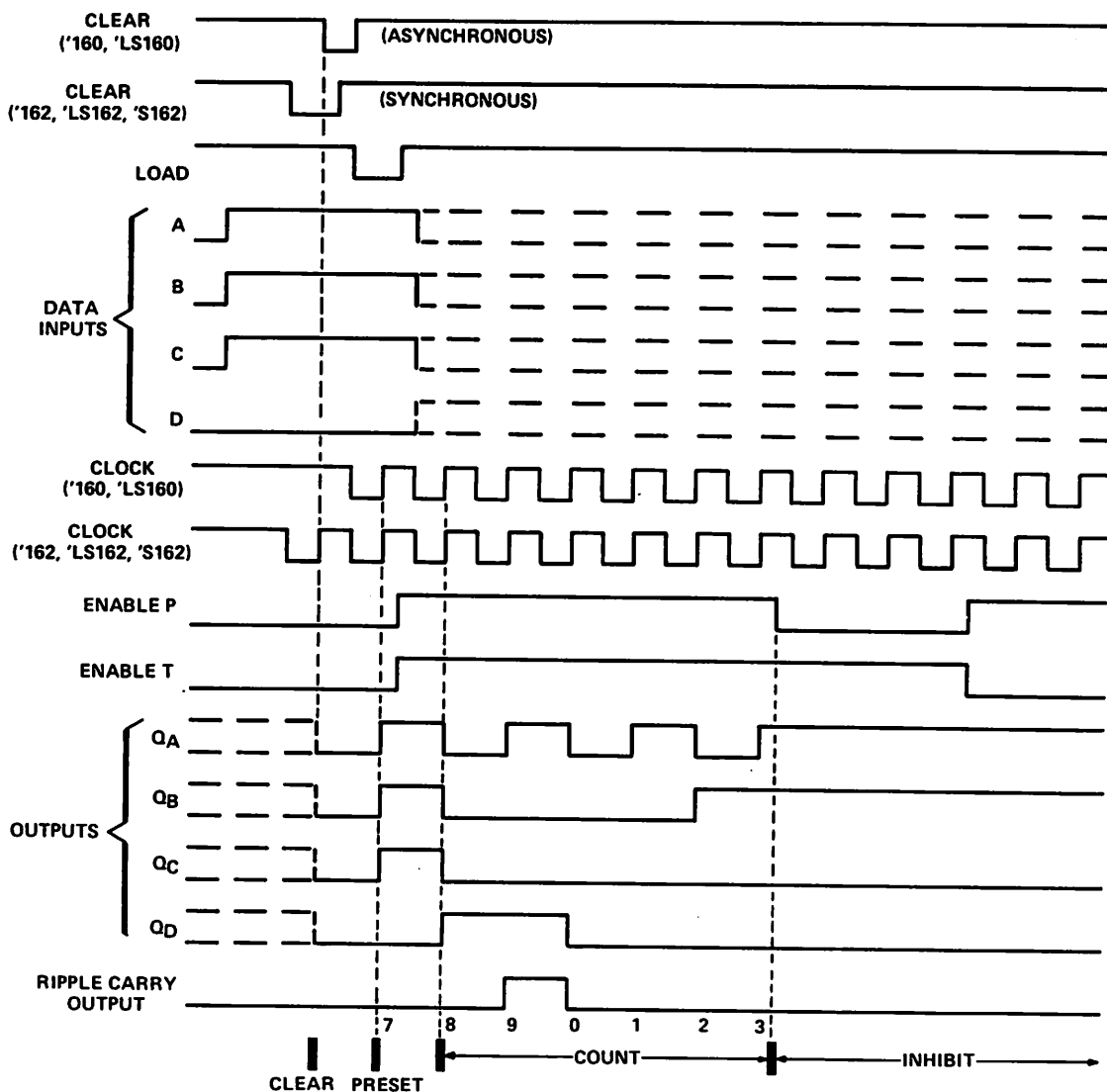
TYPES SN54160, SN54162, SN54LS160, SN54LS162, SN54S162, SN74160, SN74162, SN74LS160, SN74LS162, SN74S162 SYNCHRONOUS 4-BIT COUNTERS

'160, '162, 'LS160, 'LS162, 'S162 SYNCHRONOUS DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



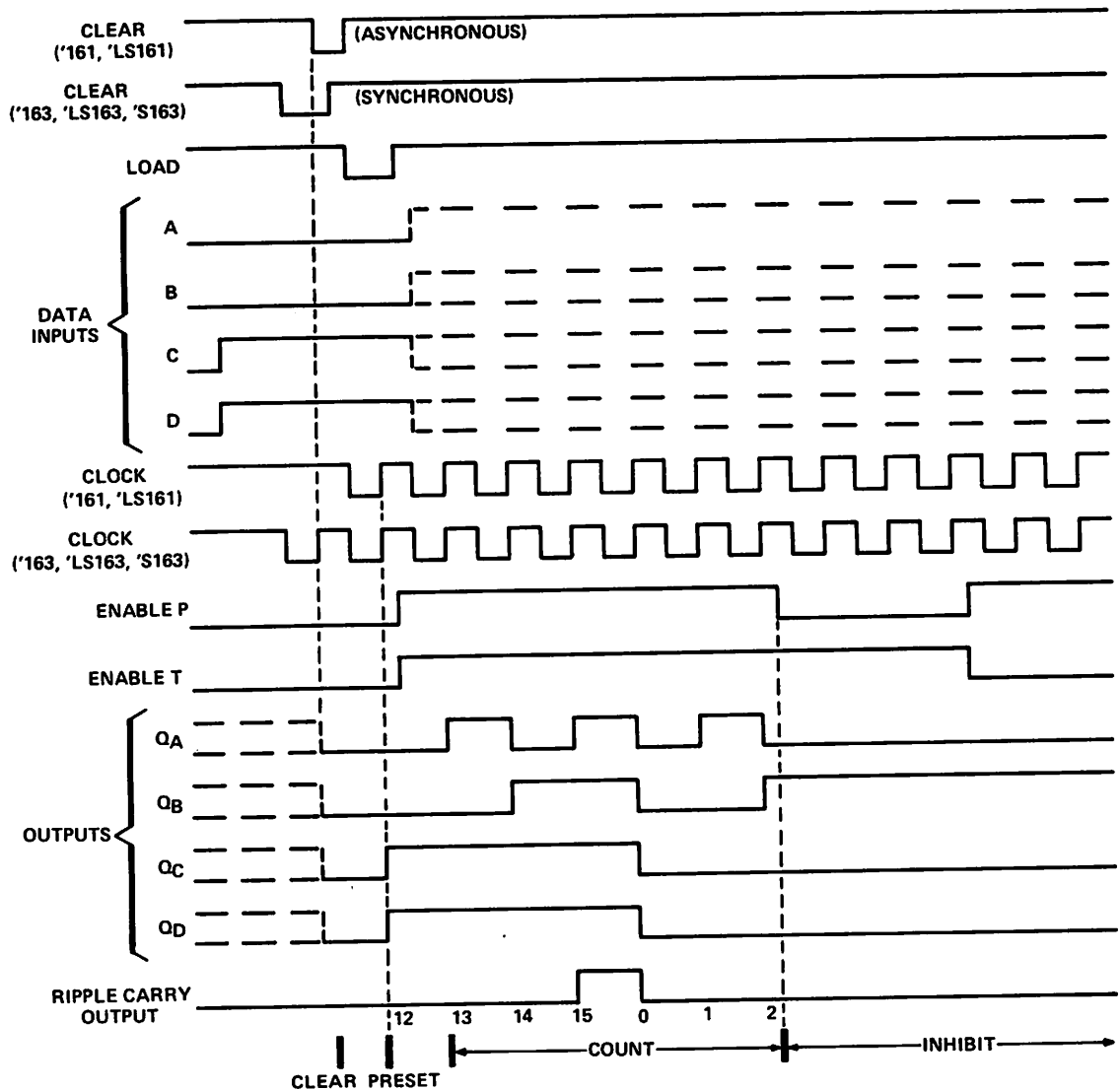
TYPES SN54161, SN54163, SN54LS161, SN54LS163, SN54S163, SN74161, SN74163, SN74LS161, SN74LS163, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

'161, 'LS161, '163, 'LS163, 'S163 SYNCHRONOUS BINARY COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit

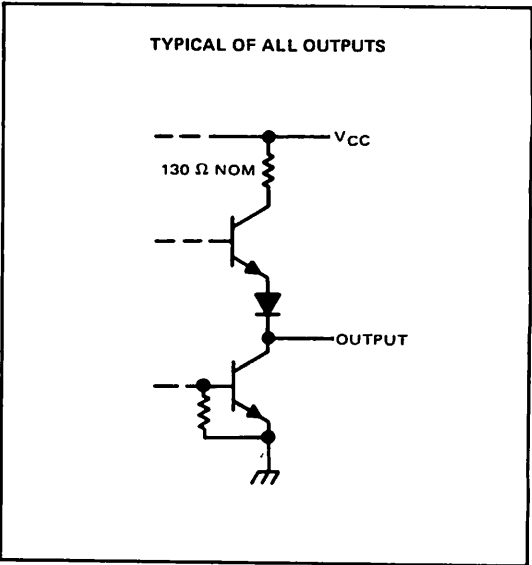
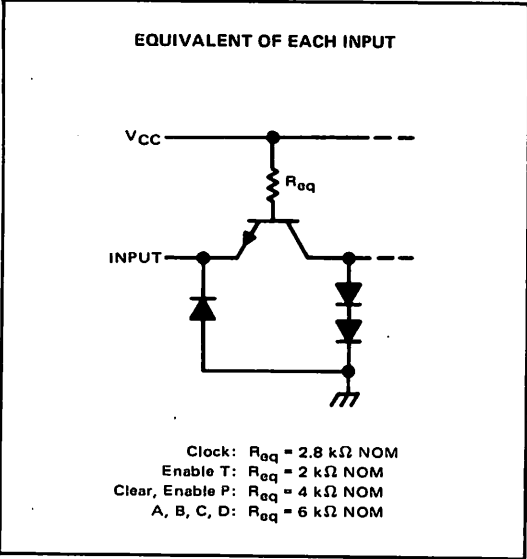


3

TYPES SN54160 THRU SN54163, SN74160 THRU SN74163
SYNCHRONOUS 4-BIT COUNTERS

REVISED MARCH 1974

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54' Circuits	-55°C to 125°C
SN74' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

		SN54160, SN54161 SN54162, SN54163			SN74160, SN74161 SN74162, SN74163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-800			-800	μ A
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_w(clock)$		25			25			ns
Width of clear pulse, $t_w(clear)$		20			20			ns
Setup time, t_{setup} (see Figures 1 and 2)	Data inputs A, B, C, D	20			20			ns
	Enable P	20			20			
	Load	25			25			
	Clear [○]	20			20			
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

[○]This applies only for '162 and '163, which have synchronous clear inputs.

TYPES SN54160 THRU SN54163, SN74160 THRU SN74163 SYNCHRONOUS 4-BIT COUNTERS

REVISED MARCH 1974

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54160, SN54161		SN74160, SN74161		UNIT		
			SN54162, SN54163	SN74162, SN74163	MIN	TYP‡		MAX	MIN
V _{IH}	High-level input voltage				2		2		V
V _{IL}	Low-level input voltage				0.8		0.8		V
V _I	Input clamp voltage		V _{CC} = MIN, I _I = -12 mA		-1.5		-1.5		V
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 µA		2.4	3.4	2.4	3.4	V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4	0.2	0.4	V
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 5.5 V		1		1		mA
I _{IH}	High-level input current	Clock or enable T	V _{CC} = MAX, V _I = 2.4 V		80		80		µA
		Other inputs			40		40		
I _{IL}	Low-level input current	Clock or enable T	V _{CC} = MAX, V _I = 0.4 V		-3.2		-3.2		mA
		Other inputs			-1.6		-1.6		
I _{OS}	Short-circuit output current §		V _{CC} = MAX		-20	-57	-18	-57	mA
I _{CCH}	Supply current, all outputs high		V _{CC} = MAX, See Note 3		59	85	59	94	mA
I _{CCL}	Supply current, all outputs low		V _{CC} = MAX, See Note 4		63	91	63	101	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			C _L = 15 pF, R _L = 400 Ω, See Figures 1 and 2 and Notes 5 and 6	25	32		ns
t _{PLH}	Clock	Ripple carry			23	35	ns
t _{PHL}					23	35	
t _{PLH}	Clock (load input high)	Any Q			13	20	ns
t _{PHL}					15	23	
t _{PLH}	Clock (load input low)	Any Q			17	25	ns
t _{PHL}					19	29	
t _{PLH}	Enable T	Ripple carry			11	16	ns
t _{PHL}					11	16	
t _{PHL}	Clear	Any Q			26	38	ns

¶ f_{max} ≡ Maximum clock frequency

t_{PLH} ≡ propagation delay time, low-to-high-level output

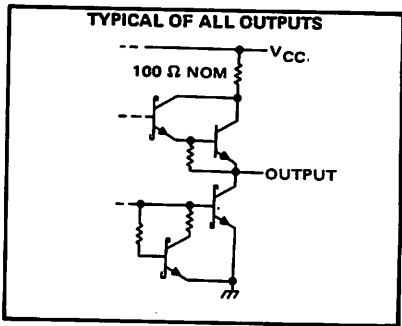
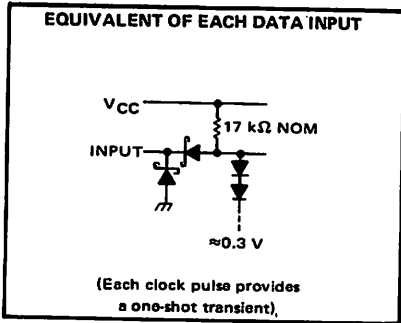
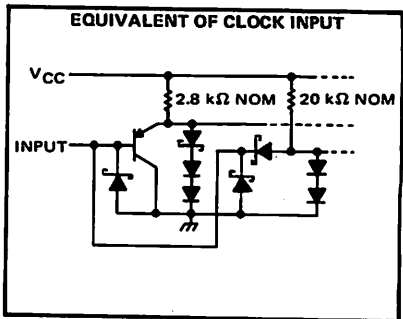
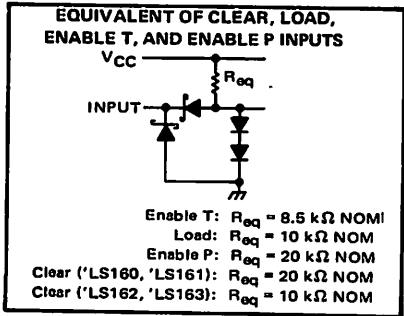
t_{PHL} ≡ propagation delay time, high-to-low-level output

NOTES: 5. Load circuit is shown on page S-87.

6. Propagation delay for clearing is measured from the clear input for the '160 and '161 or from the clock input transition for the '162 and '163.

TYPES SN54LS160 THRU SN54LS163, SN74LS160 THRU SN74LS163 SYNCHRONOUS 4-BIT COUNTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 7)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS' Circuits	-55°C to 125°C
SN74LS' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 7: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-400			-400			μA
Low-level output current, I_{OL}		4			8			mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_w(\text{clock})$		25			25			ns
Width of clear pulse, $t_w(\text{clear})$		20			20			ns
Setup time, t_{setup} (see Figures 1 and 2)	Data inputs A, B, C, D	0			0			ns
	Enable P or T	20			20			
	Load	20			20			
	Clear ^o	20			20			
Hold time at any input, t_{hold}		25 [†]			25 [†]			ns
Operating free-air temperature, T_A		-55		125	0		70	$^{\circ}\text{C}$

^o This applies only for 'LS162 and 'LS163, which have synchronous clear inputs.

[†] The minimum hold time is 25 ns or as long as the clock input takes to rise from 0.8 V to 2 V, whichever is longer.

TENTATIVE DATA

S-178

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TYPES SN54LS160 THRU SN54LS163, SN74LS160 THRU SN74LS163 SYNCHRONOUS 4-BIT COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _I	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 8 mA					0.35	0.5	
I _I	Input current at maximum input voltage	Data or enable P			0.1			0.1	mA
		Load, clock, or enable T			0.2			0.2	
		Clear ('LS160, 'LS161)			0.1			0.1	
		Clear ('LS162, 'LS163)			0.2			0.2	
I _{IH}	High-level input current	Data or enable P			20			20	µA
		Load, clock, or enable T			40			40	
		Clear ('LS160, 'LS161)			20			20	
		Clear ('LS162, 'LS163)			40			40	
I _{IL}	Low-level input current	Data or enable P			-0.4			-0.4	mA
		Load, clock, or enable T			-0.8			-0.8	
		Clear ('LS160, 'LS161)			-0.4			-0.4	
		Clear ('LS162, 'LS163)			-0.8			-0.8	
I _{OS}	Short-circuit output current §	V _{CC} = MAX	-6	-40		-5	-42		mA
I _{CC}	Supply current, all outputs high	V _{CC} = MAX, See Note 3		18	31		18	31	mA
I _{CCL}	Supply current, all outputs low	V _{CC} = MAX, See Note 4		19	32		19	32	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTES: 3. I_{CC} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				25	32		MHz
t _{PLH}	Clock	Ripple	C _L = 15 pF, R _L = 2 kΩ, See Figures 1 and 2 and Notes 8 and 9		23	35	ns
t _{PHL}		carry			23	35	
t _{PLH}	Clock (load input high)	Any			16	24	ns
t _{PHL}		Q			18	27	
t _{PLH}	Clock (load input low)	Any			17	25	ns
t _{PHL}		Q			19	29	
t _{PLH}	Enable T	Ripple			15	23	ns
t _{PHL}		carry			15	23	
t _{PHL}	Clear	Any Q			26	38	ns

¶ f_{max} = Maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output.

NOTES: 8. Load circuit is shown on page S-88.

9. Propagation delay for clearing is measured from the clear input for the 'LS160 and 'LS161 or from the clock input transition for the 'LS162 and 'LS163.

TENTATIVE DATA

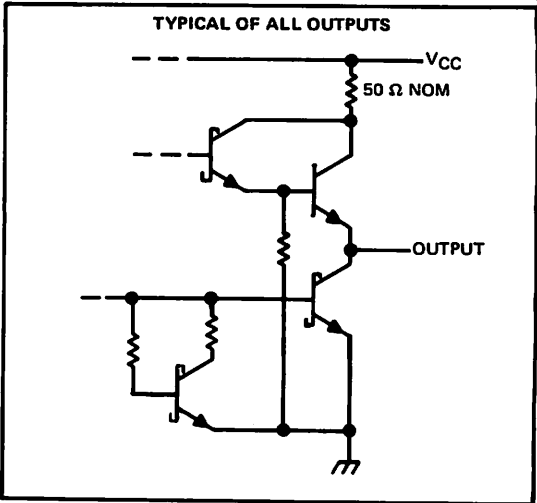
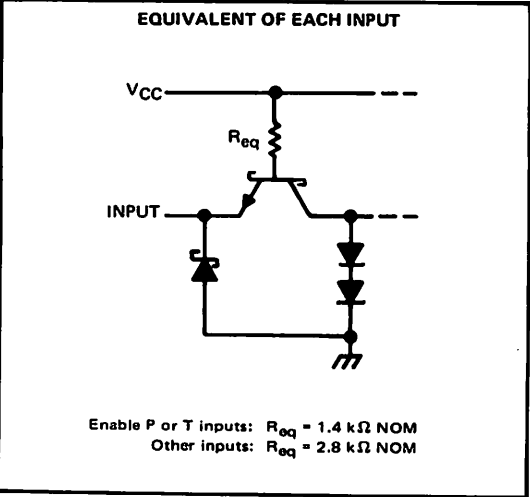
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S-179

TYPES SN54S162, SN54S163, SN74S162, SN74S163
SYNCHRONOUS 4-BIT COUNTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54S162, SN54S163 (see Note 10)	-55°C to 125°C
SN74S162, SN74S163	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54S162, SN54S163			SN74S162, SN74S163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-1			-1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		40	0		40	MHz
Width of clock pulse, $t_w(\text{clock})$ (high or low)		10			10			ns
Width of clear pulse, $t_w(\text{clear})$		10			10			ns
Setup time, t_{setup} (see Figure 4)	Data inputs, A, B, C, D	4			4			ns
	Enable P or T	12			12			
	Load	14			14			
	Clear	14			14			
	Load inactive-state	12			12			
	Clear inactive-state	12			12			
Release time, t_{release} (see Figure 4)				4			4	ns
Hold time, t_{hold} (see Figure 4)	Data inputs A, B, C, D	3			3			ns
	Load	0			0			
	Clear	0			0			
Operating free-air temperature, T_A (see Note 10)		-55		125	0		70	$^{\circ}\text{C}$

- NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.
10. An SN54S162 or SN54S163 in the W package operating at free-air temperatures above 91°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 26°C/W .

TYPES SN54S162, SN54S163, SN74S162, SN74S163

SYNCHRONOUS 4-BIT COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S162 SN54S163			SN74S162 SN74S163			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage			0.8			0.8		V
V _I Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA		0.5			0.5		V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		1			1		mA
I _{IH} High-level input current	Enable T		100			100		µA
	Other inputs		50			50		
I _{IL} Low-level input current	Enable T		-4			-4		mA
	Other inputs		-2			-2		
I _{OS} Short-circuit output current§	V _{CC} = MAX	-40	-100		-40	-100		mA
I _{CC} Supply current	V _{CC} = MAX		95	160		95	160	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			C _L = 15 pF, R _L = 280 Ω, See Figures 1, 3, and 4 and Note 5	40	70		MHz
t _{PLH}	Clock	Ripple carry			14	25	ns
t _{PHL}					17	25	
t _{PLH}	Clock	Any Q			8	15	ns
t _{PHL}					10	15	
t _{PLH}	Enable T	Ripple carry			10	15	ns
t _{PHL}					10	15	

¶f_{max} ≡ maximum clock frequency

t_{PLH} ≡ propagation delay time, low-to-high-level output

t_{PHL} ≡ propagation delay time, high-to-low-level output

NOTE 5: Load circuit is shown on page S-87.

TENTATIVE DATA

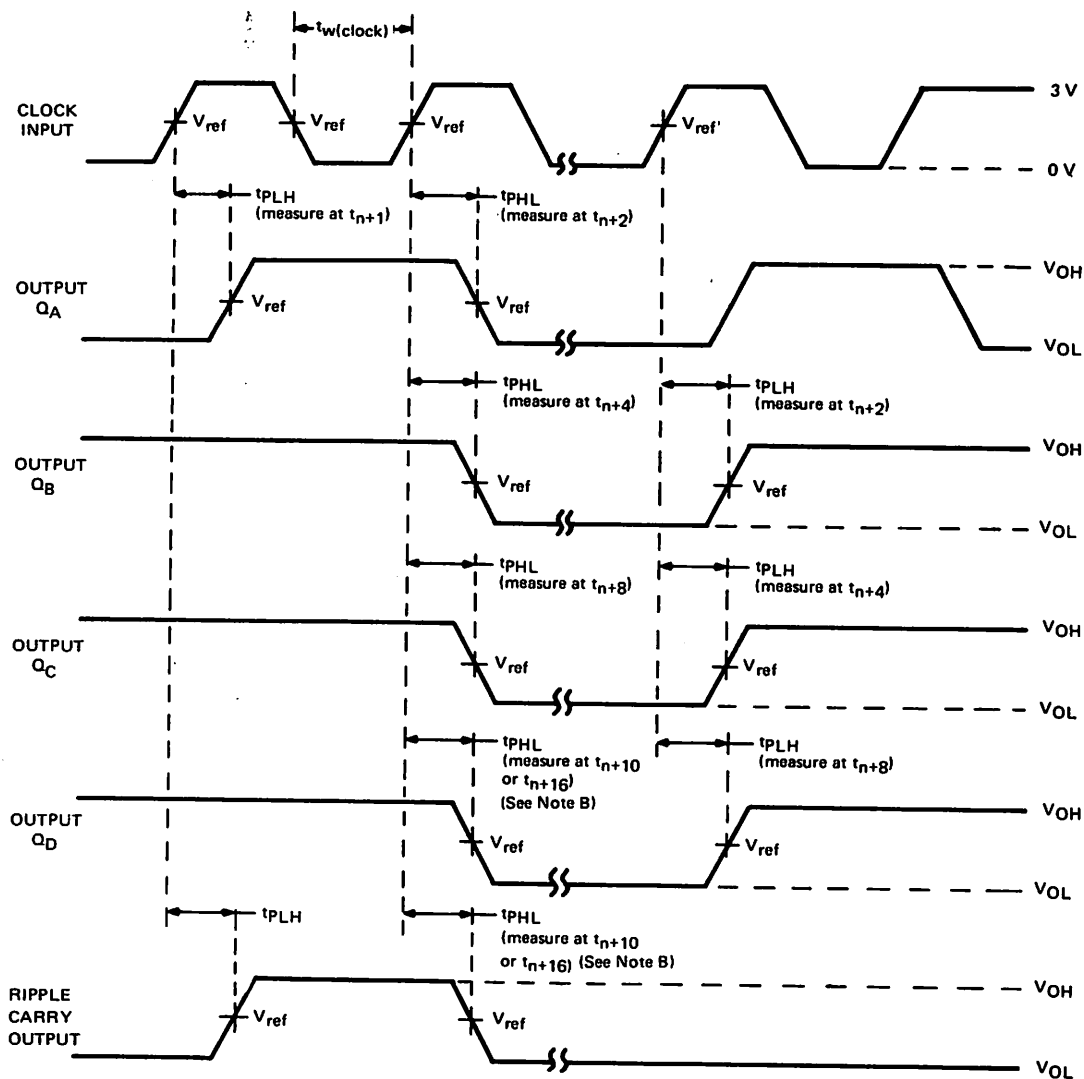
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S-181

**TYPES SN54160 THRU SN54163, SN54LS160 THRU SN54LS163,
SN54S162, SN54S163, SN74160 THRU SN74163,
SN74LS160 THRU SN74LS163, SN74S162, SN74S163
SYNCHRONOUS 4-BIT COUNTERS**

PARAMETER MEASUREMENT INFORMATION

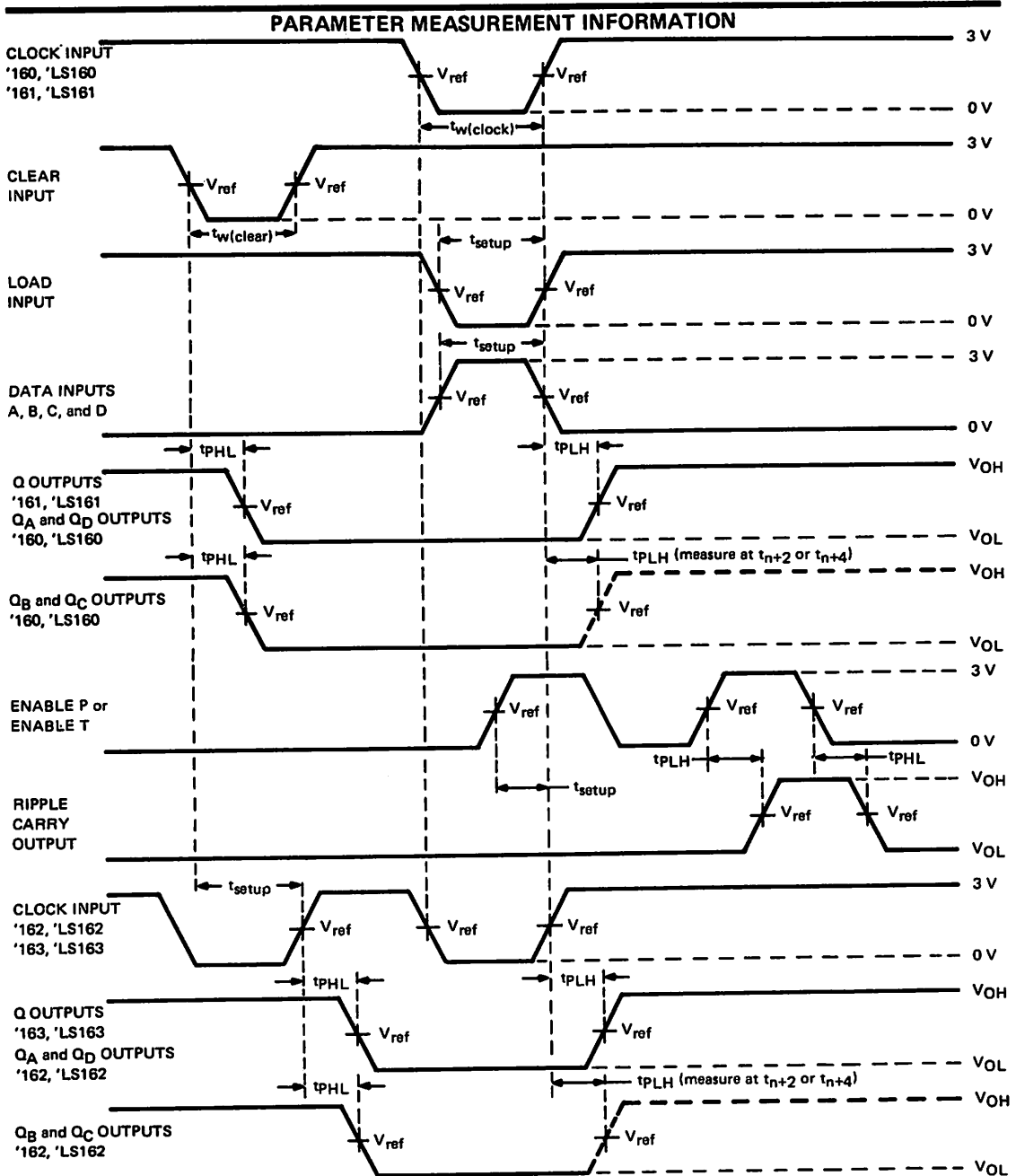


VOLTAGE WAVEFORMS

- NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{out} \approx 50 \Omega$; for '160 thru '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; for 'LS160 thru 'LS163, $t_r \leq 15$ ns, $t_f \leq 6$ ns; and for 'S162, 'S163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{max} .
- B. Outputs Q_D and carry are tested at t_{n+10} for '160, '162, 'LS160, 'LS162 and 'S162, and at t_{n+16} for '161, '163, 'LS161, 'LS163, and 'S163, where t_n is the bit time when all outputs are low.
- C. For '160 thru '163, 'S162, and 'S163, $V_{ref} = 1.5$ V; for 'LS160 thru 'LS163, $V_{ref} = 1.3$ V.

FIGURE 1—SWITCHING TIMES

TYPES SN54160 THRU SN54163, SN54LS160 THRU SN54LS163, SN74160 THRU SN74163, SN74LS160 THRU SN74LS163 SYNCHRONOUS 4-BIT COUNTERS

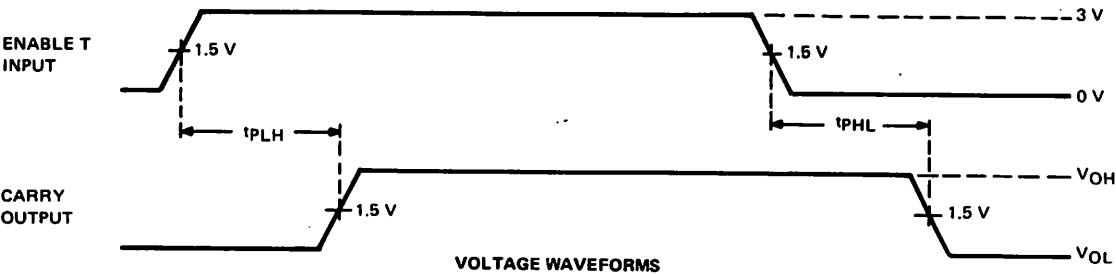


- NOTES:** A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$; for '160 thru '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; and for 'LS160 thru 'LS163, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
- B. Enable P and enable T setup times are measured at t_{n+0} .
- C. For '160 thru '163, $V_{ref} = 1.5$ V; for 'LS160 thru 'LS163, $V_{ref} = 1.3$ V.

FIGURE 2—SWITCHING TIMES

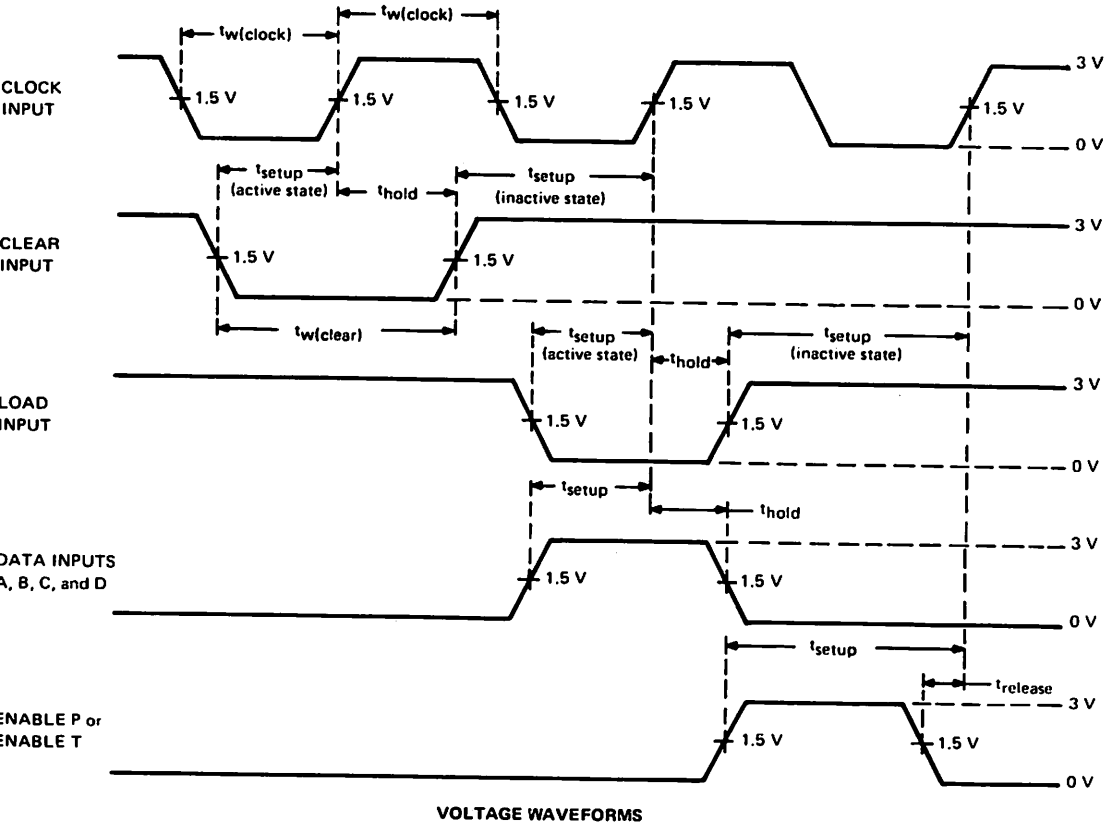
TYPES SN54S162, SN54S163, SN74S162, SN74S163 **SYNCHRONOUS 4-BIT COUNTERS**

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$.
 B. t_{PLH} and t_{PHL} from enable T input to carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'S162, all Q outputs high for 'S163).

FIGURE 3—PROPAGATION DELAY TIMES FROM ENABLE T INPUT TO CARRY OUTPUT



NOTE A: The input pulses are supplied by generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$.

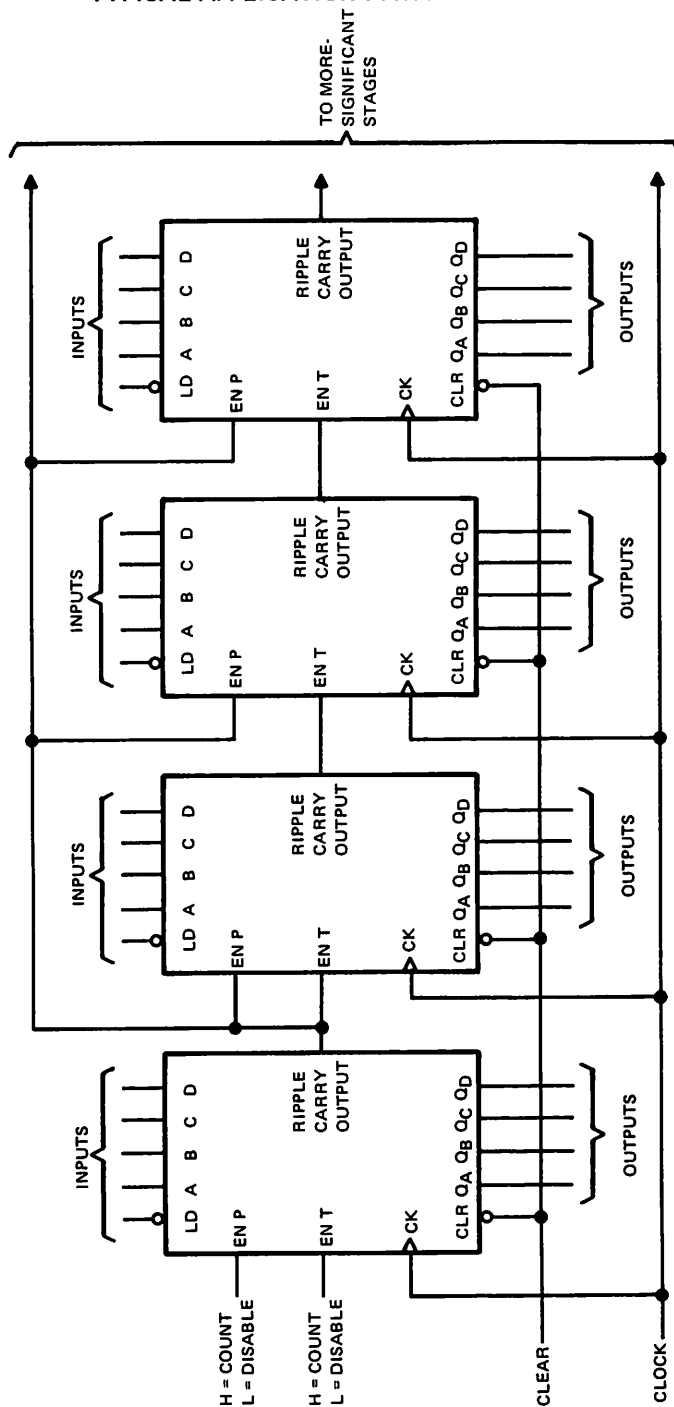
FIGURE 4—PULSE WIDTHS, SETUP TIMES, HOLD TIMES, AND RELEASE TIME

TYPES SN54160 THRU SN54163, SN54LS160 THRU SN54LS163, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160 THRU SN74LS163, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The '160, '162, 'LS160, 'LS162, or 'S162 will count in BCD and the '161, '163, 'LS161, 'LS163, or 'S163 will count in binary. Virtually any count mode (modulo-N, N₁-to-N₂, N₁-to-maximum) can be used with this fast look-ahead circuit.



H = COUNT
L = DISABLE

H = COUNT
L = DISABLE

CLEAR

CLOCK

TTL TYPES SN54164, SN54L164, SN54LS164, SN74164, SN74L164, SN74LS164 MSI

BULLETIN NO. DL-S 7411835, MARCH 1974

- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear

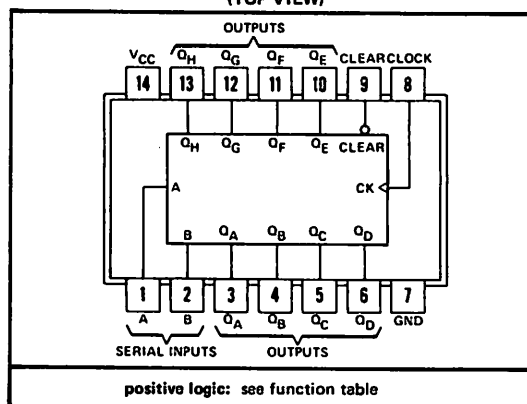
SN54164, SN54LS164 ... J OR W PACKAGE
SN54L164, SN74L164 ... J, N, OR T PACKAGE
SN74164, SN74LS164 ... J OR N PACKAGE
(TOP VIEW)

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'164	36 MHz	21 mW per bit
'L164	18 MHz	11 mW per bit
'LS164	36 MHz	10 mW per bit

description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Series 54, 54L, and 54LS devices are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74, 74L, and 74LS devices are characterized for operation from 0°C to 70°C .



positive logic: see function table

FUNCTION TABLE

INPUTS				OUTPUTS			
CLEAR	CLOCK	A	B	QA	QB	...	QH
L	X	X	X	L	L	...	L
H	L	X	X	QA0	QB0	...	QH0
H	↑	H	H	H	QA _n	...	QG _n
H	↑	L	X	L	QA _n	...	QG _n
H	↑	X	L	L	QA _n	...	QG _n

H = high level (steady state), L = low level (steady state)

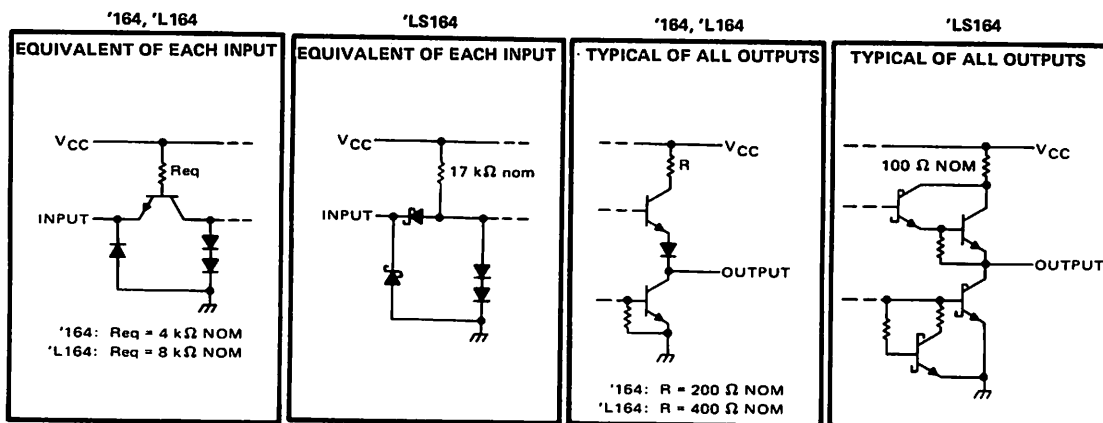
X = irrelevant (any input, including transitions)

↑ = transition from low to high level.

QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.

QA_n, QG_n = the level of QA or QG before the most-recent ↑ transition of the clock; indicates a one-bit shift.

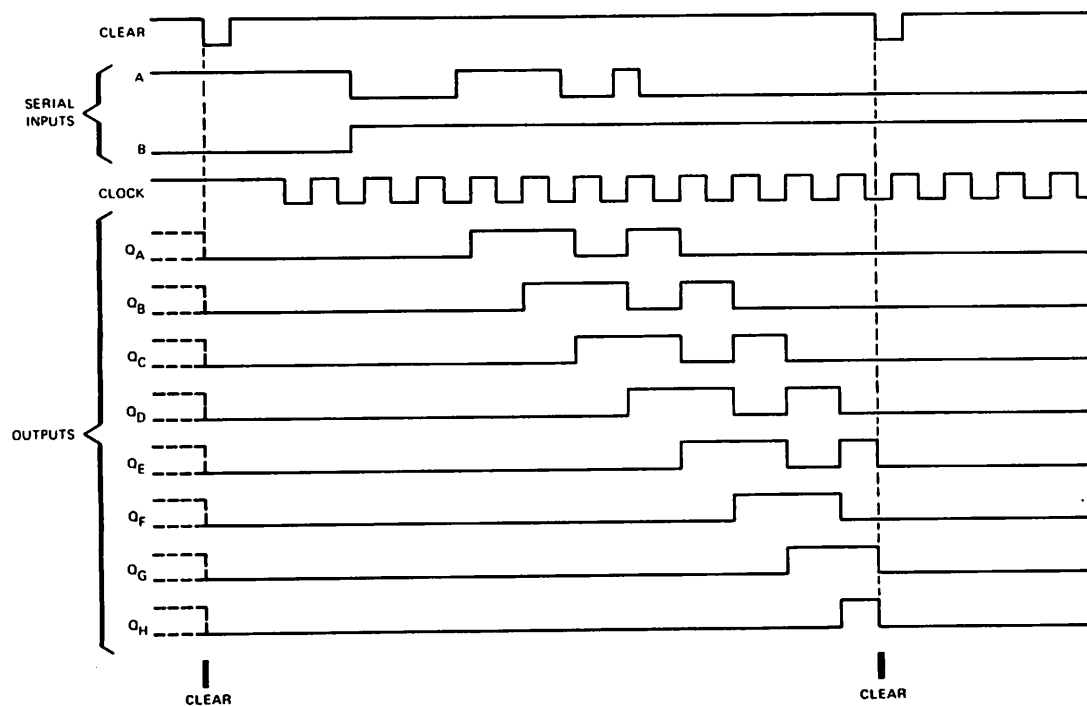
schematics of inputs and outputs



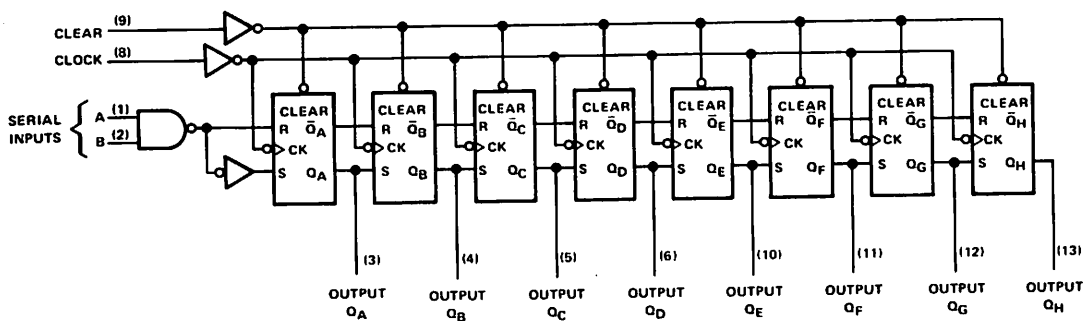
TYPES SN54164, SN54L164, SN54LS164, SN74164, SN74L164, SN74LS164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

typical clear, shift, and clear sequences



functional block diagram



TYPES SN54164, SN74164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

REVISED MARCH 1974

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54164	−55°C to 125°C
SN74164	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54164			SN74164			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			8			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear input pulse, t_W	20			20			ns
Data setup time, t_{setup} (see Figure 1)	15			15			ns
Data hold time, t_{hold} (see Figure 1)	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54164			SN74164			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			−1.5			−1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -400 \text{ μA}$	2.4	3.2		2.4	3.2		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 8 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			−1.6			−1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	−10	−27.5		−9	−27.5		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, $V_I(\text{clock}) = 0.4 \text{ V}$		30			30		mA
	See Note 2, $V_I(\text{clock}) = 2.4 \text{ V}$		37	54		37	54	

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than two outputs should be shorted at a time.

NOTE 2: I_{CC} is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V, applied to clear.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}$	25	36		MHz
t_{PHL} Propagation delay time, high-to-low-level Q outputs from clear input	$C_L = 15 \text{ pF}$		24	36	ns
	$C_L = 50 \text{ pF}$		28	42	
t_{PLH} Propagation delay time, low-to-high-level Q outputs from clock input	$C_L = 15 \text{ pF}$	8	17	27	ns
	$C_L = 50 \text{ pF}$	10	20	30	
t_{PHL} Propagation delay time, high-to-low-level Q outputs from the clock input	$C_L = 15 \text{ pF}$	10	21	32	ns
	$C_L = 50 \text{ pF}$	10	25	37	

TYPES SN54L164, SN74L164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

REVISED MARCH 1974

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	5.5 V
Input voltage	5.5 V
Operating free-air temperature range: SN54L164	−55°C to 125°C
SN74L164	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54L164			SN74L164			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−200			−200	μA
Low-level output current, I_{OL}			4			4	mA
Clock frequency, f_{clock}	0		12	0		12	MHz
Width of clock or clear input pulse, t_W	40			40			ns
Data setup time, t_{setup} (see Figure 1)	30			30			ns
Data hold time, t_{hold} (see Figure 1)	10			10			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54L164			SN74L164			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			−1.5			−1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -200 \mu\text{A}$	2.4	3.2		2.4	3.2		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 4 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			20			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			−0.8			−0.8	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	−5		−20	−4		−20	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 3}$		19	27		19	27	mA

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

§ Not more than two outputs should be shorted at a time.

NOTE 3: I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V, applied to clear.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}$	12	18		MHz
t_{PHL} Propagation delay time, high-to-low-level Q outputs from clear input	$C_L = 15 \text{ pF}$		48	72	ns
t_{PLH} Propagation delay time, low-to-high-level Q outputs from clock input	$C_L = 50 \text{ pF}$		56	84	ns
t_{PLH} Propagation delay time, low-to-high-level Q outputs from clock input	$C_L = 15 \text{ pF}$	8	34	54	ns
t_{PHL} Propagation delay time, high-to-low-level Q outputs from the clock input	$C_L = 50 \text{ pF}$	10	20	60	ns
t_{PHL} Propagation delay time, high-to-low-level Q outputs from the clock input	$C_L = 15 \text{ pF}$	10	42	64	ns
t_{PHL} Propagation delay time, high-to-low-level Q outputs from the clock input	$C_L = 50 \text{ pF}$	10	50	74	ns

TYPES SN54LS164, SN74LS164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS164	-55°C to 125°C
SN74LS164	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS164			SN74LS164			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear input pulse, t_W	20			20			ns
Data setup time, t_{setup} (see Figure 1)	15			15			ns
Data hold time, t_{hold} (see Figure 1)	5			5			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS164			SN74LS164			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage			0.7			0.8		V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5			-1.5		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	0.25	0.4		0.25	0.4	0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20		μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4			-0.4		mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-6	-40		-5	-42		mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 3		16	27		16	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V applied to clear.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Figure 1	25	36		MHz
t_{PHL} Propagation delay time, high-to-low-level Q outputs from clear input			24	36	ns
t_{PLH} Propagation delay time, low-to-high-level Q outputs from clock input			17	27	ns
t_{PHL} Propagation delay time, high-to-low-level Q outputs from clock input			21	32	ns

TENTATIVE DATA

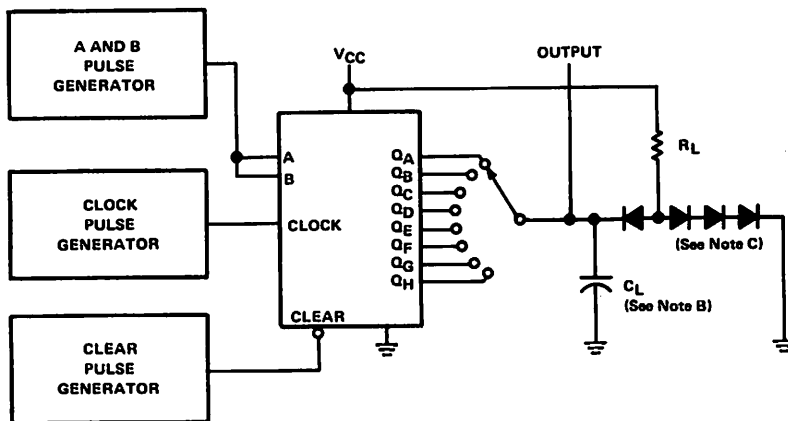
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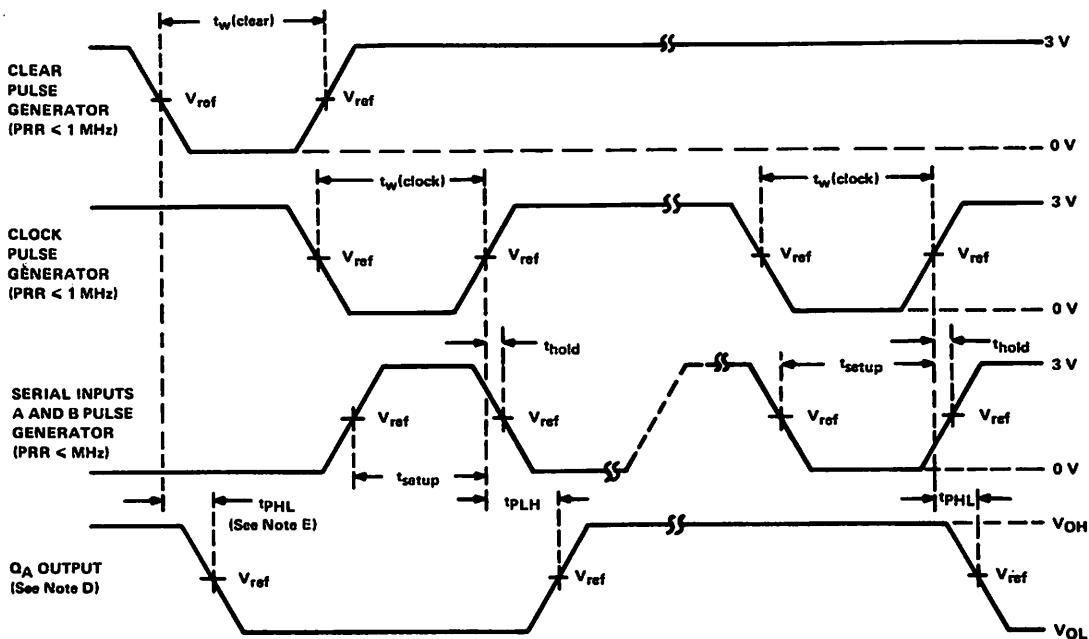
TYPES SN54164, SN54L164, SN54LS164, SN74164, SN74L164, SN74LS164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generators have the following characteristics: duty cycle $\leq 80\%$, $Z_{out} \approx 50 \Omega$; for '164 and 'L164, $t_r \leq 10$ ns, $t_f \leq 10$ ns, and for 'LS164, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or 1N916.
- D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
- E. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
- F. For '164 and 'L164, $V_{ref} = 1.5$ V; for 'LS164, $V_{ref} = 1.3$ V.

FIGURE 1—SWITCHING TIMES

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S-191

TYPES SN54LS168, SN54LS169, SN54S168, SN54S169, SN74LS168, SN74LS169, SN74S168, SN74S169 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

BULLETIN NO. DL-S 7412068, MARCH 1974

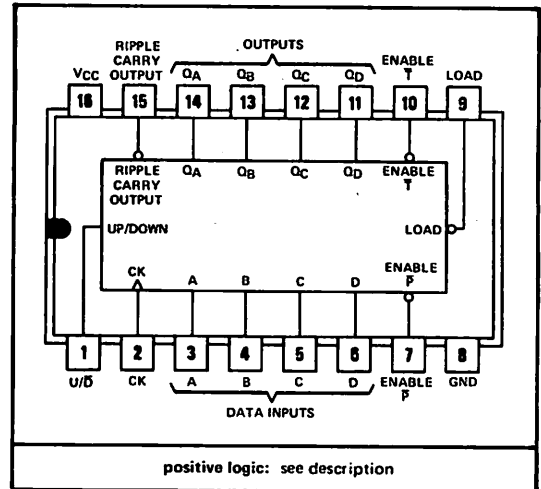
'LS168, 'S168 ... SYNCHRONOUS UP/DOWN DECADE COUNTERS
'LS169, 'S169 ... SYNCHRONOUS UP/DOWN BINARY COUNTERS

Programmable Look-Ahead Up/Down Binary/Decade Counters

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS168, 'LS169	35 MHz	35 MHz	100 mW
'S168, 'S169	70 MHz	55 MHz	500 mW

SERIES SN54LS', SN54S' ... J OR W PACKAGE
SERIES SN74LS', SN74S' ... J OR N PACKAGE
(TOP VIEW)



description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS168 and 'S168 are decade counters and the 'LS169 and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs (\bar{P} and \bar{T}) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input \bar{T} is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable \bar{P} or \bar{T} inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable \bar{P} , enable \bar{T} , load, up/down), which modify the operating mode, have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Series 54LS and Series 54S circuits are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74LS and Series 74S circuits are characterized for operation from 0°C to 70°C .

TENTATIVE DATA SHEET

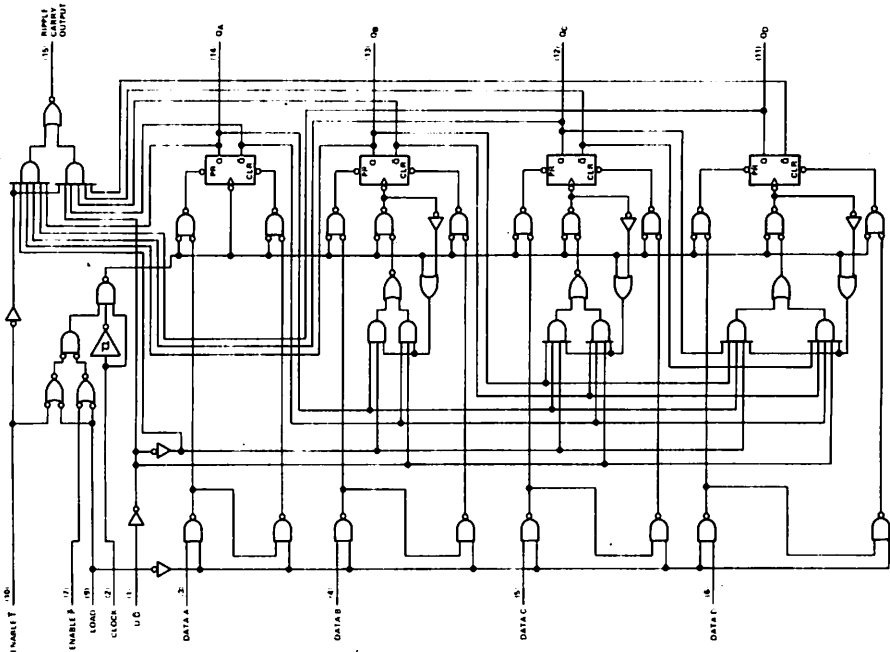
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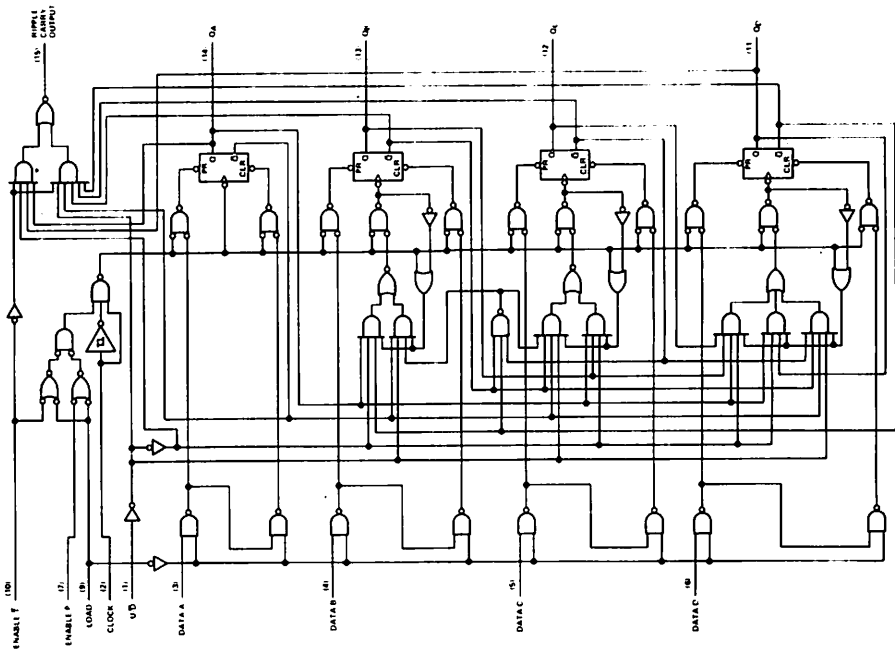
TYPES SN54LS168, SN54LS169, SN74LS168, SN74LS169, SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

functional block diagrams

SN54LS169, SN74LS169 BINARY COUNTERS



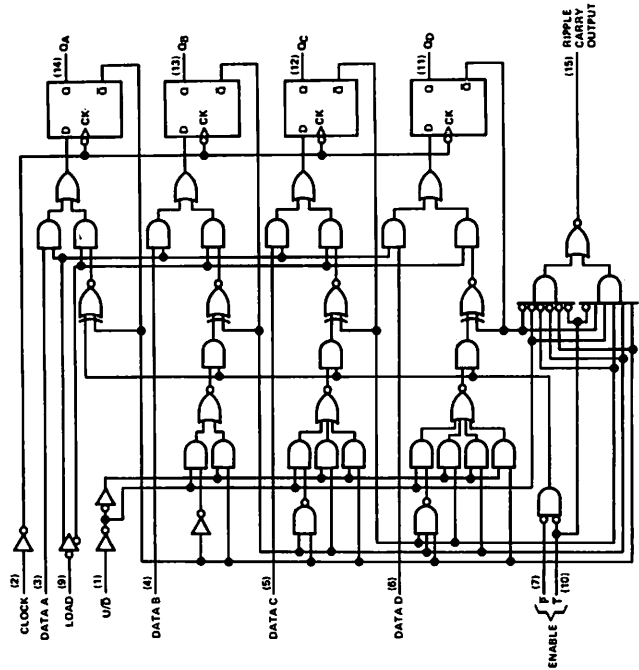
SN54LS168, SN74LS168 DECADE COUNTERS



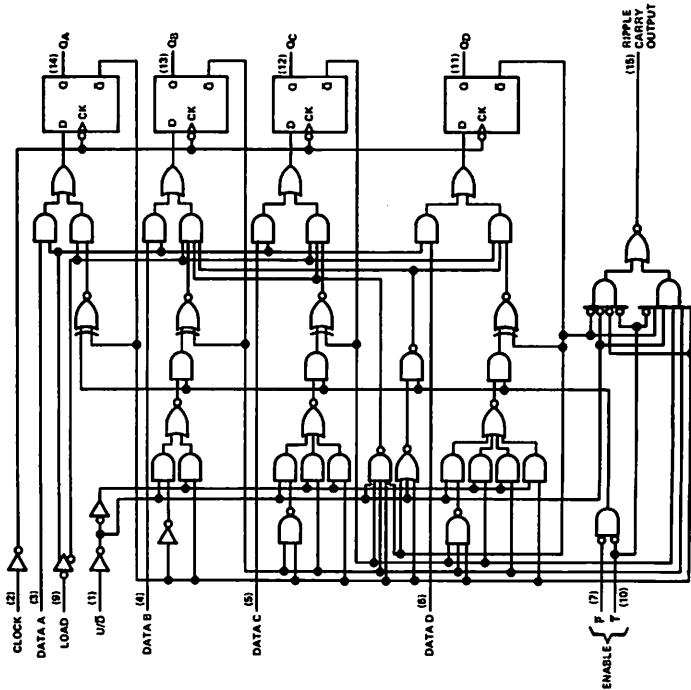
TYPES SN54S168, SN54S169, SN74S168, SN74S169
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

functional block diagrams

SN54S169, SN74S169 BINARY COUNTERS



SN54S168, SN74S168 DECADE COUNTERS



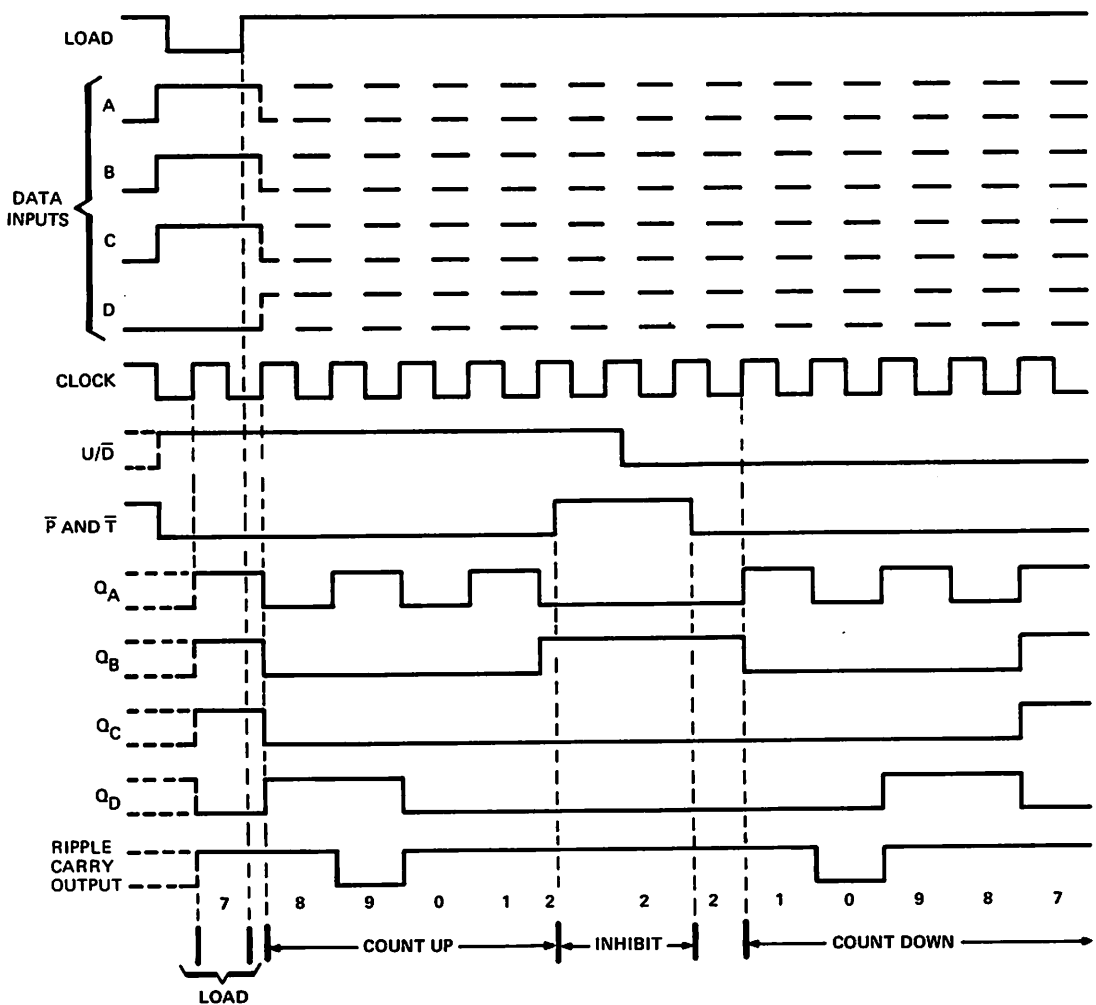
TYPES SN54LS168, SN54S168, SN74LS168, SN74S168 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

'LS168, 'S168 DECADE COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



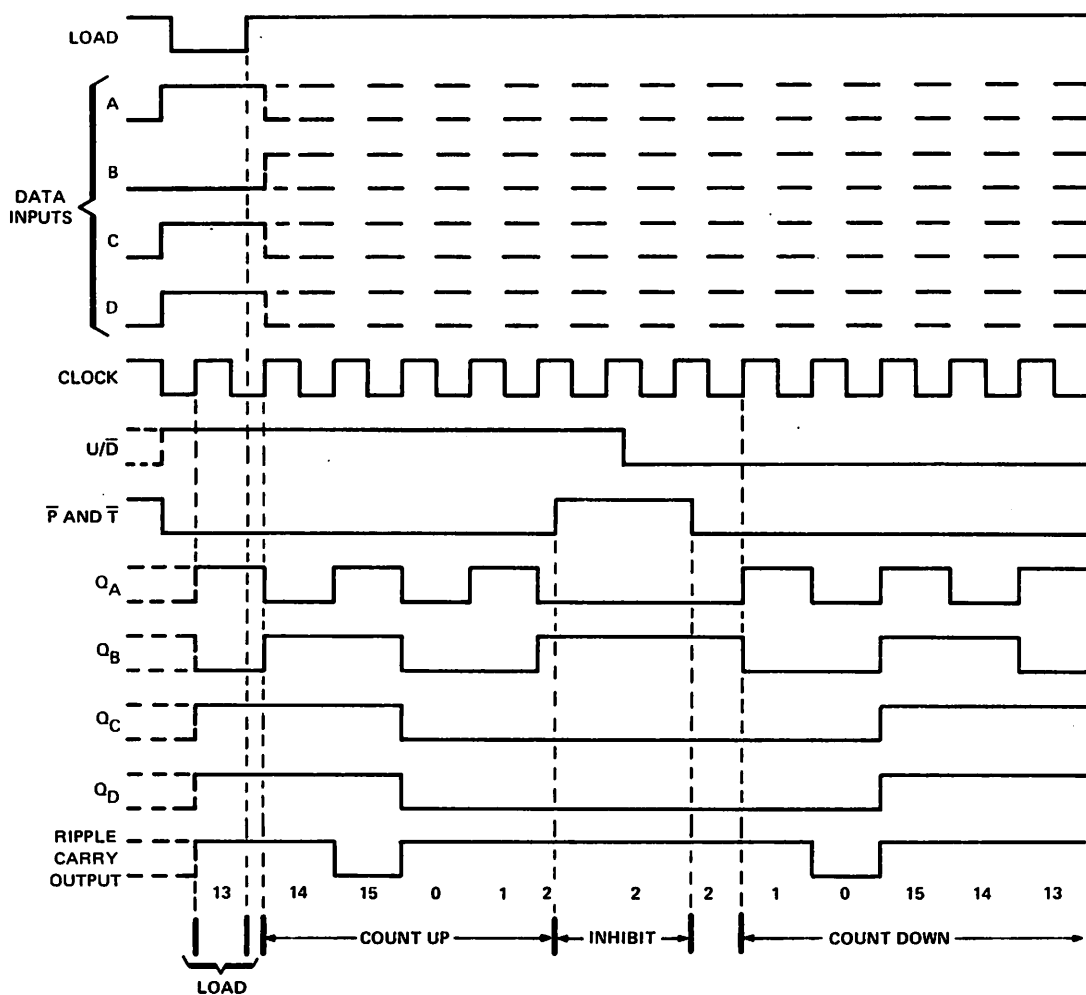
TYPES SN54LS169, SN54S169, SN74LS169, SN74S169 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

'LS169, 'S169 BINARY COUNTERS

typical load, count, and inhibit sequences

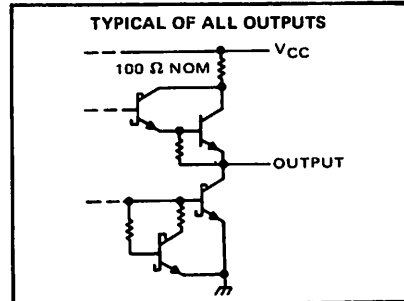
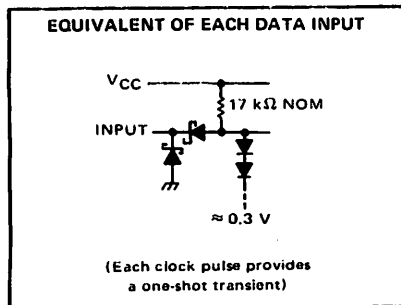
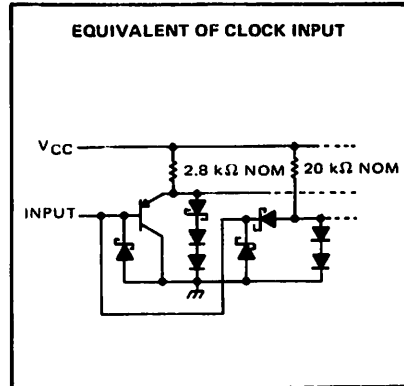
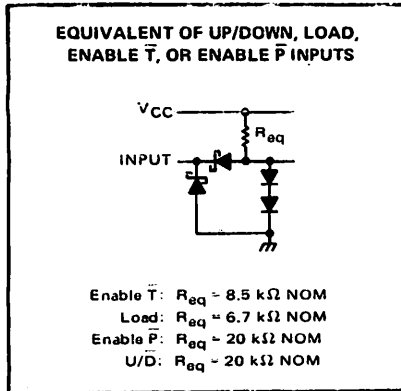
Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



TYPES SN54LS168, SN54LS169, SN74LS168, SN74LS169 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS168, SN54LS169	-55°C to 125°C
SN74LS168, SN74LS169	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS168 SN54LS169			SN74LS168 SN74LS169			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_w(\text{clock})$ (high or low) (see Figure 1)	25			25			ns
Setup time, t_{setup} (see Figure 1)	Data inputs A, B, C, D	15		15			ns
	Enable \bar{P} or \bar{T}	20		20			
	Load	25		25			
	Up/Down	30		30			
Hold time at any input with respect to clock, t_{hold} (see Figure 1)	25 [◊]			25 [◊]			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}\text{C}$

[◊]The minimum hold time is 25 ns or as long as the clock input takes to rise from 0.8 V to 2 V, whichever is longer.

TENTATIVE DATA SHEET

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TYPES SN54LS168, SN54LS169, SN74LS168, SN74LS169
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS168 SN54LS169			SN74LS168 SN74LS169			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _I	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, I _{OL} = 4 mA	0.25	0.4		0.25	0.4		V
		V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 8 mA				0.35	0.5		
I _I	Input current at maximum input voltage	A, B, C, D, \bar{P} , U/ \bar{D}			0.1			0.1	mA
		Clock, \bar{T}			0.2			0.2	
		Load			0.3			0.3	
I _{IH}	High-level input current	A, B, C, D, \bar{P} , U/ \bar{D}			20			20	µA
		Clock, \bar{T}			40			40	
		Load			60			60	
I _{IL}	Low-level input current	A, B, C, D, \bar{P} , U/ \bar{D}			-0.4			-0.4	mA
		Clock, \bar{T}			-0.8			-0.8	
		Load			-1.2			-1.2	
I _{OS}	Short-circuit output current§	V _{CC} = MAX	-6		-40	-5		-42	mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 2		20	34		20	34	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			C _L = 15 pF, R _L = 2 kΩ, See Figures 2 and 3 and Note 3	25	32		MHz
t _{PLH}	Clock	Ripple carry			23	35	ns
t _{PHL}		carry			23	35	
t _{PLH}	Clock	Any Q			13	20	ns
t _{PHL}		Q			15	23	
t _{PLH}	Enable \bar{T}	Ripple carry			10	14	ns
t _{PHL}		carry			10	14	
t _{PLH} °	Up/Down	Ripple			17	25	ns
t _{PHL} °		carry			19	29	

¶ f_{max} ≡ Maximum clock frequency

t_{PLH} ≡ propagation delay time, low-to-high-level output.

t_{PHL} ≡ propagation delay time, high-to-low-level output.

° Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS168 or 15 for 'LS169), the ripple carry output will be out of phase.

NOTE 3: Load circuit is shown on page S-88.

TENTATIVE DATA SHEET

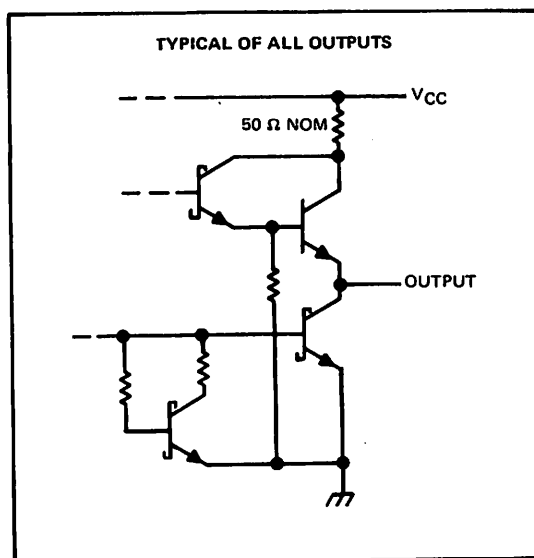
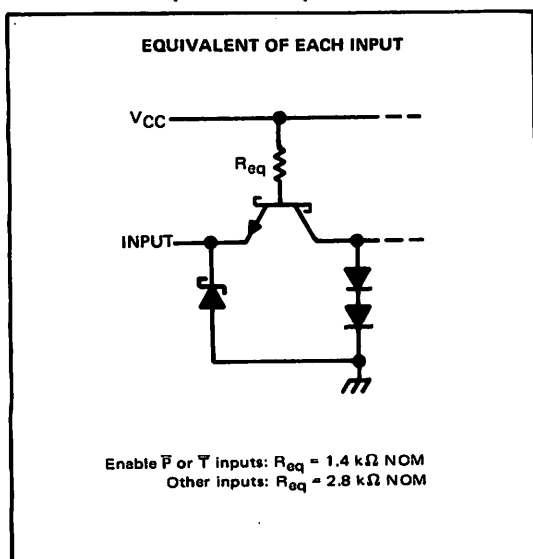
S-198

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TEXAS INSTRUMENTS
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TYPES SN54S168, SN54S169, SN74S168, SN74S169 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4)	7 V
Input voltage	5.5 V
Intermitter voltage (see Note 5)	5.5 V
Operating free-air temperature range: SN54S168, SN54S169 (see Note 6)	-55°C to 125°C
SN74S168, SN74S169	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	SN54S168 SN54S169			SN74S168 SN74S169			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Clock frequency, f_{clock}	0		40	0		40	MHz
Width of clock pulse, $t_w(\text{clock})$ (high or low) (see Figure 1)	10			10			ns
Setup time, t_{setup} (see Figure 1)	Data inputs A, B, C, D	4		4			ns
	Enable \bar{P} or \bar{T}	14		14			
	Load	6		6			
	Up/Down	20		20			
Hold time at any input with respect to clock, t_{hold} (see Figure 1)	1			1			ns
Operating free-air temperature, T_A (see Note 6)	-55		125	0		70	°C

- NOTES: 4. Voltage values, except intermitter voltage, are with respect to network ground terminal.
5. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs \bar{P} and \bar{T} .
6. An SN54S168 or SN54S169 in the W package operating at free-air temperatures above 91°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 26°C/W.

TYPES SN54S168, SN54S169, SN74S168, SN74S169

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S168 SN54S169			SN74S168 SN74S169			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
V _I	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA			0.5			0.5	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	High-level input current	Enable \bar{T}			100			100	μ A
		Other inputs			50			50	
I _{IL}	Low-level input current	Enable \bar{T}			-4			-4	mA
		Other inputs			-2			-2	
I _{OS}	Short-circuit output current§	V _{CC} = MAX	-40		-100	-40		-100	mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 2	100	160		100	160		mA
		V _{CC} = MAX, W package		160					
		T _A = 125°C only							

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	UP/DOWN = HIGH			UP/DOWN = LOW			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}			C _L = 15 pF, R _L = 280 Ω, See Figures 2 and 3 and Note 7	40	70		40	55		MHz
t _{PLH}	Clock	Ripple carry			14	21		14	21	ns
t _{PHL}					20	28		20	28	
t _{PLH}	Clock	Any Q			8	15		8	15	ns
t _{PHL}					11	15		11	15	
t _{PLH}	Enable \bar{T}	Ripple carry			7.5	11		6	12	ns
t _{PHL}					15	22		15	25	
t _{PLH} °	Up/Down	Ripple carry			9	15		8	15	ns
t _{PHL} °					10	15		16	22	

¶ f_{max} ≡ maximum clock frequency

t_{PLH} ≡ propagation delay time, low-to-high-level output

t_{PHL} ≡ propagation delay time, high-to-low-level output

° Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'S168 or 15 for 'S169), the ripple carry output will be out of phase.

NOTE 7: Load circuit is shown on page S-87.

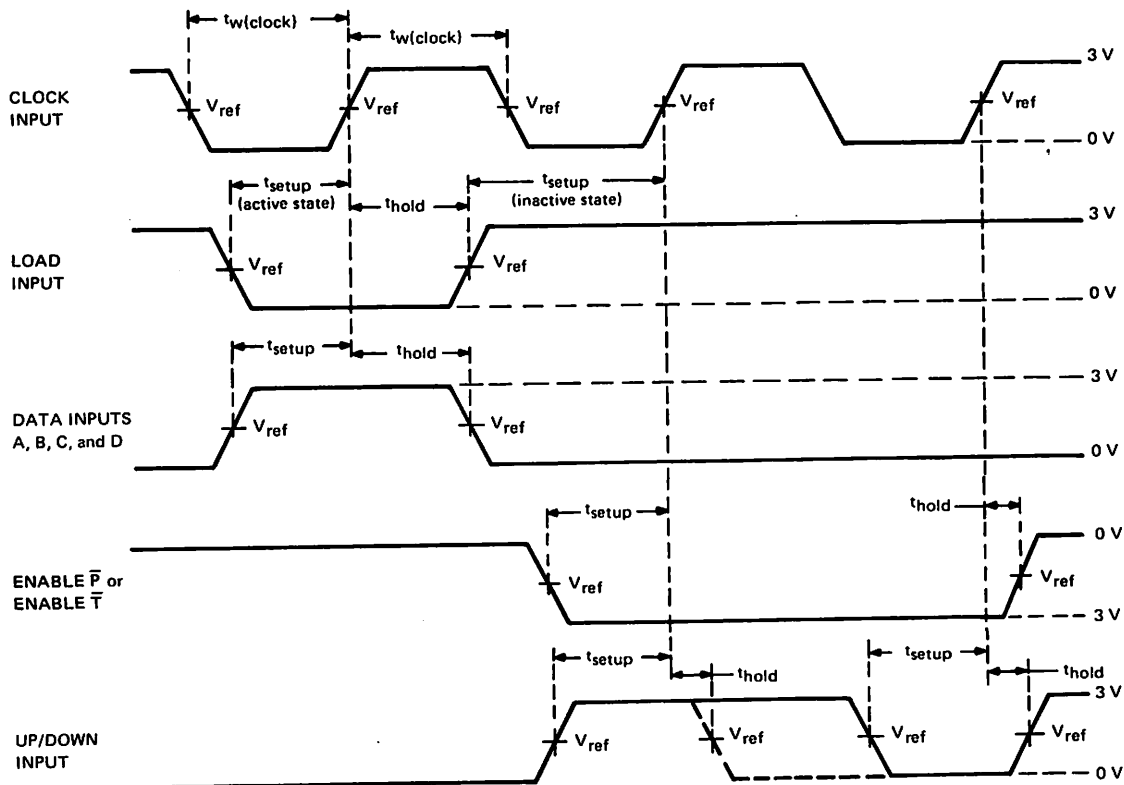
TENTATIVE DATA SHEET

S-200 This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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TYPES SN54LS168, SN54LS169, SN54S168, SN54S169, SN74LS168, SN74LS169, SN74S168, SN74S169 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

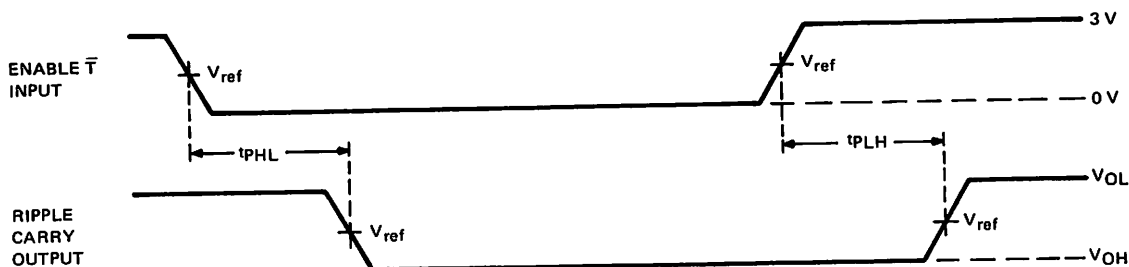
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

- NOTES: A. The input pulses are supplied by a generator having the following characteristics: $\text{PRR} \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_{\text{out}} \approx 50 \Omega$; for 'LS168 and 'LS169, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$; and for 'S168 and 'S169, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
B. For 'LS168 and 'LS169, $V_{\text{ref}} = 1.3 \text{ V}$; for 'S168 and 'S169, $V_{\text{ref}} = 1.5 \text{ V}$.

FIGURE 1—PULSE WIDTHS, SETUP TIMES, HOLD TIMES



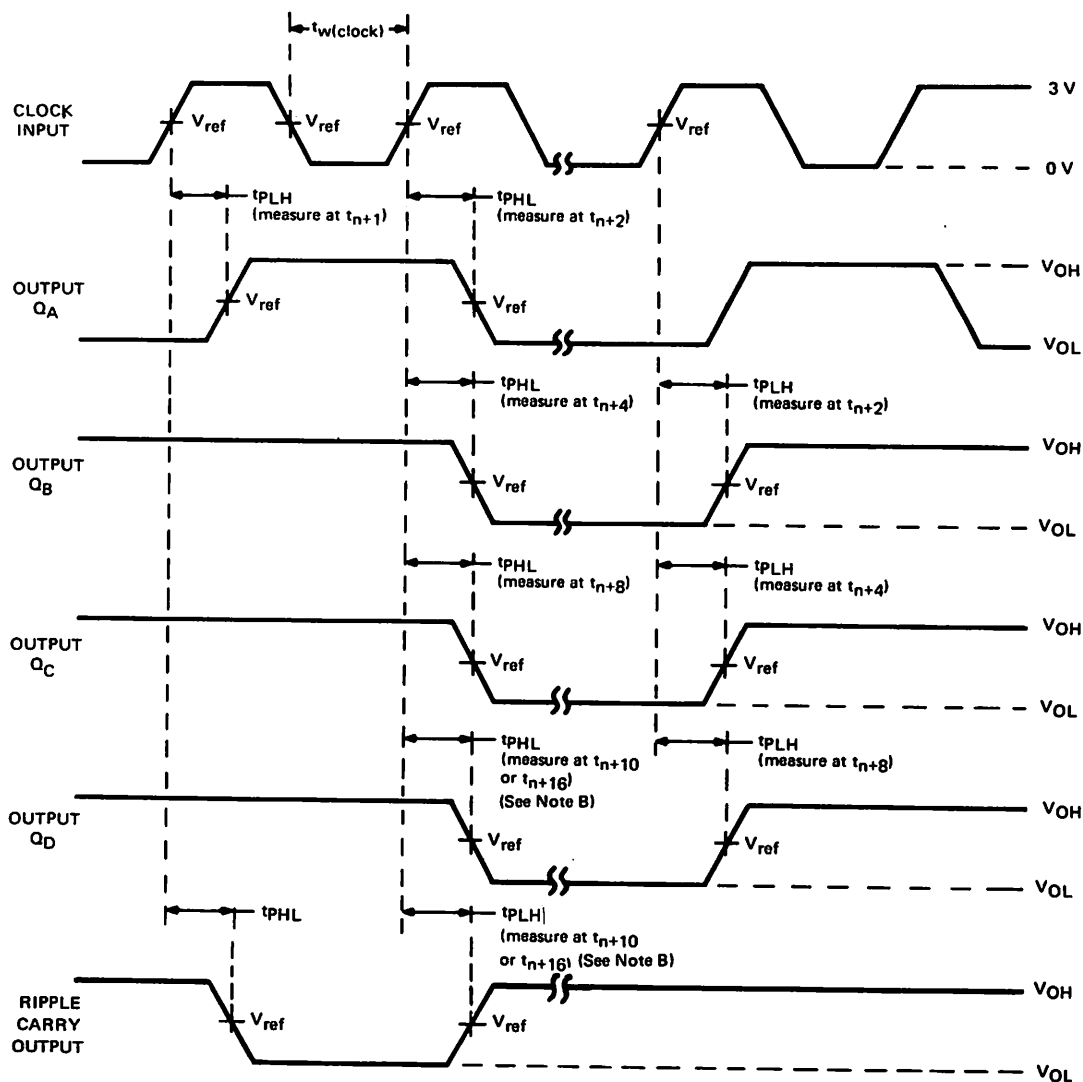
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_{\text{out}} \approx 50 \Omega$; for 'LS168 and 'LS169, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$; and for 'S168 and 'S169, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
B. t_{PLH} and t_{PHL} from enable \bar{T} input to ripple carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'LS168 and 'S168, all Q outputs high for 'LS169 and 'S169).
C. For 'LS168 and 'LS169, $V_{\text{ref}} = 1.3 \text{ V}$; for 'S168 and 'S169, $V_{\text{ref}} = 1.5 \text{ V}$.
D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS168 or 15 for 'LS169 and 'S169) the ripple carry output will be out of phase.

FIGURE 2—PROPAGATION DELAY TIMES TO CARRY OUTPUT

**TYPES SN54LS168, SN54LS169, SN54S168, SN54S169,
SN74LS168, SN74LS169, SN74S168, SN74S169
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS**

PARAMETER MEASUREMENT INFORMATION



UP-COUNT VOLTAGE WAVEFORMS

- NOTES: A. The input pulses are supplied by a generator having the following characteristics: $\text{PRR} \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_{\text{out}} \approx 50 \Omega$; for 'LS168 and 'LS169, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$; and for 'S168 and 'S169, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$. Vary PRR to measure f_{max} .
- B. Outputs Q_D and carry are tested at t_{n+10} for the 'LS168 and 'S168, and at t_{n+16} for the 'LS169 and 'S169, where t_n is the bit-time when all outputs are low.
- C. For 'LS168 and 'LS169, $V_{\text{ref}} = 1.3 \text{ V}$; for 'S168 and 'S169, $V_{\text{ref}} = 1.5 \text{ V}$.

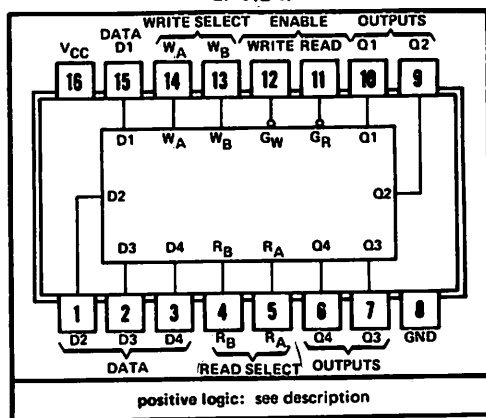
FIGURE 3—PROPAGATION DELAY TIMES FROM CLOCK

TYPES SN54170, SN54LS170, SN74170, SN74LS170 **4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS**

BULLETIN NO. DL-S 7411349, MARCH 1974

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Organized as 4 Words of 4 Bits
- Expandable to 1024 Words of n-Bits
- For Use as:
Scratch-Pad Memory
Buffer Storage between Processors
Bit Storage in Fast Multiplication Designs
- Open-Collector Outputs with Low Maximum Off-State Current:
'170 . . . 30 μ A
'LS170 . . . 100 μ A
- SN54LS670 and SN74LS670 Are Similar But Have 3-State Outputs

SN54170, SN54LS170 . . . J OR W PACKAGE
SN74170, SN74LS170 . . . J OR N PACKAGE
(TOP VIEW)



description

The '170 and 'LS170 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W , is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R , is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (30 nanoseconds typical) and the read time (25 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All '170 inputs and all inputs except the read enable and write enable of the 'LS170 are buffered to lower the drive requirements to one Series 54/74 or Series 54LS/74LS standard load, respectively. Input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

The SN54170 and SN54LS170 are characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74170 and SN74LS170 are characterized for operation from 0°C to 70°C .

TYPES SN54170, SN54LS170, SN74170, SN74LS170
4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

logic

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

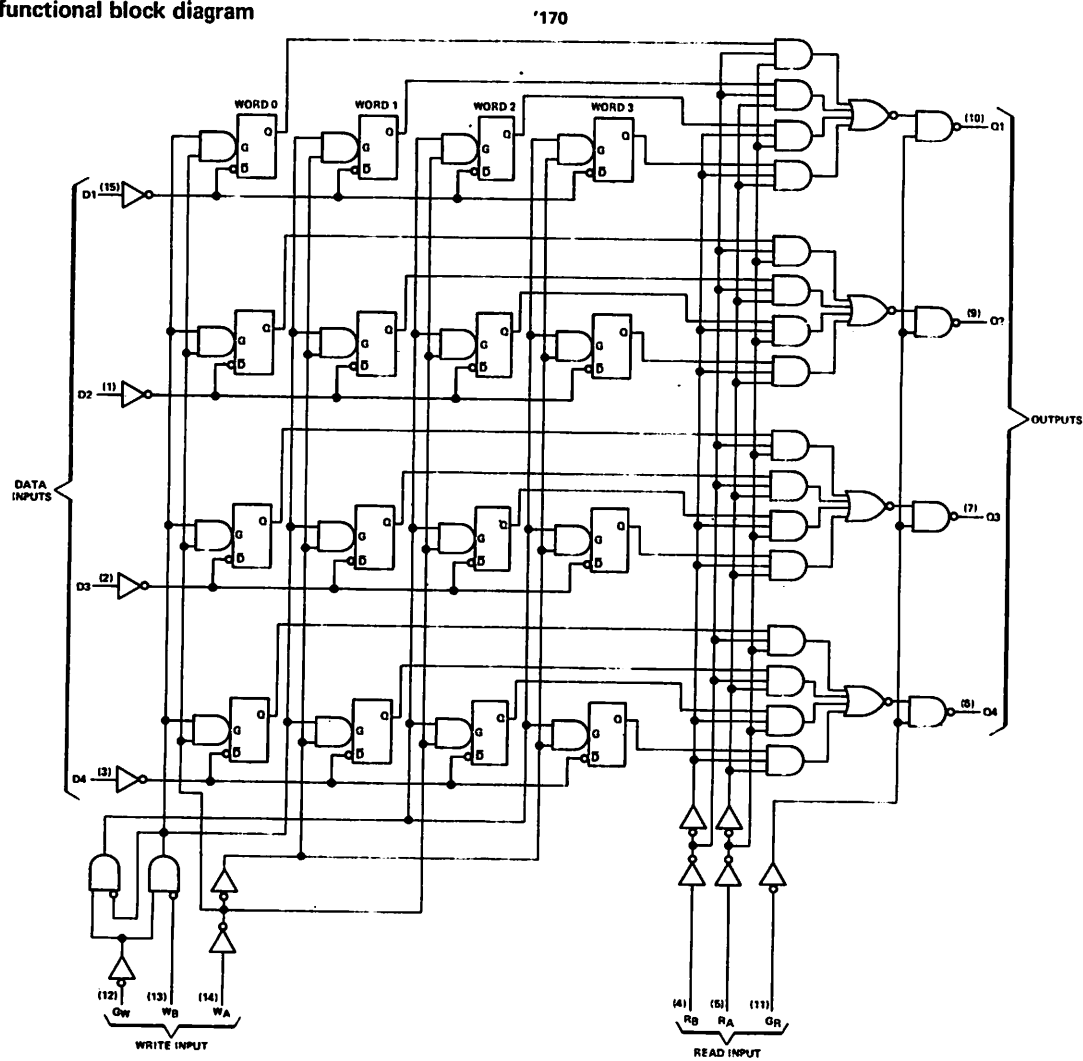
WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	$Q = D$	Q_0	Q_0	Q_0
L	H	L	Q_0	$Q = D$	Q_0	Q_0
H	L	L	Q_0	Q_0	$Q = D$	Q_0
H	H	L	Q_0	Q_0	Q_0	$Q = D$
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: A. H = high level, L = low level, X = irrelevant.
B. ($Q = D$) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_0 = the level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

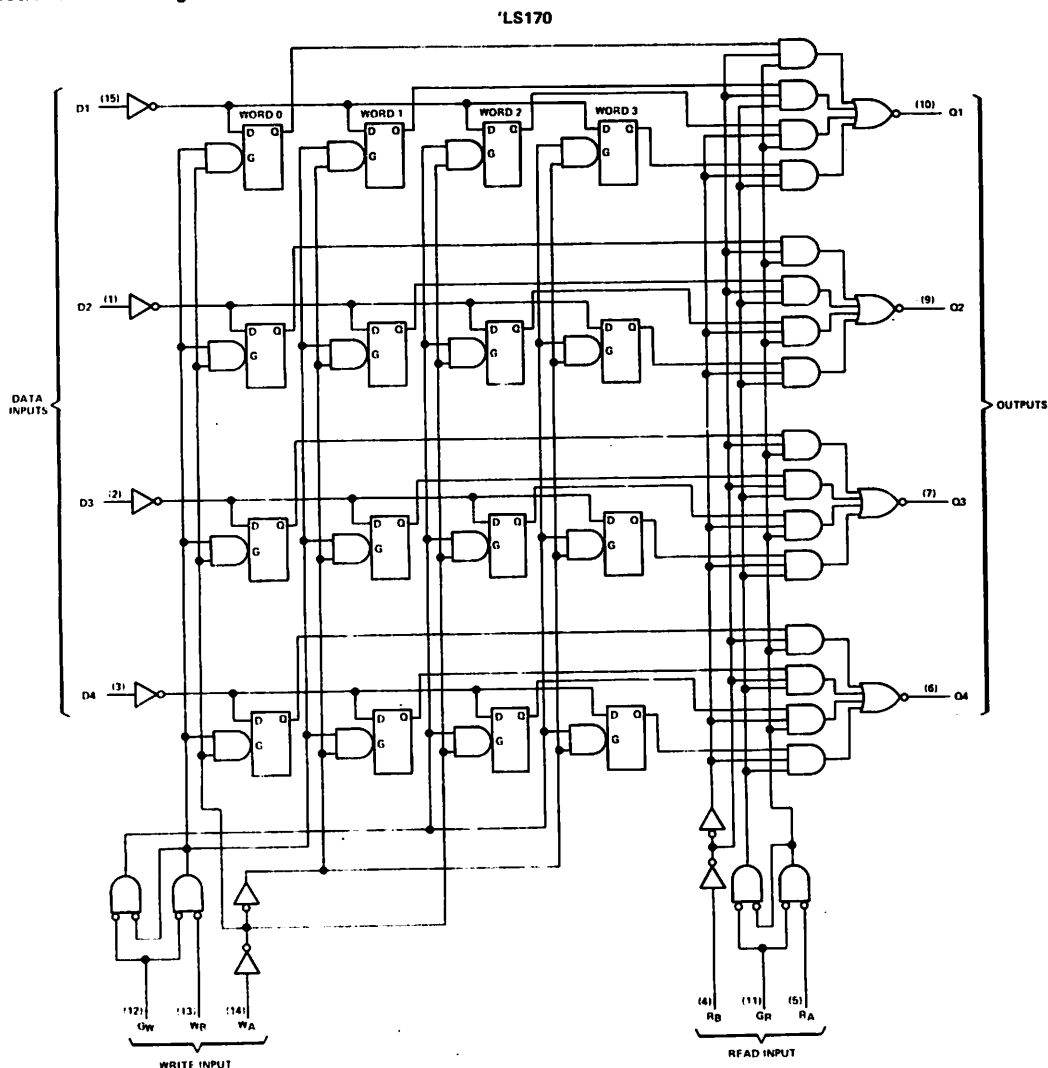
functional block diagram



TYPES SN54170, SN54LS170, SN74170, SN74LS170

4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '170	5.5 V
'LS170	7 V
Off-state output voltage: '170	5.5 V
'LS170	7 V
Operating free-air temperature range: SN54170, SN54LS170 (see Note 2)	-55°C to 125°C
SN74170, SN74LS170	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54170 in the W package operating at free-air temperatures above 105°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$ of not more than 38°C/W

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S-205

TYPES SN54170, SN74170

4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

		SN54170			SN74170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				16			16	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{setup}(D)$	10			10			ns
	Write select with respect to write enable, $t_{setup}(W)$	15			15			ns
Hold times, high- or low-level data (see Note 3 and Figure 2)	Data input with respect to write enable, $t_{hold}(D)$	15			15			ns
	Write select with respect to write enable, $t_{hold}(W)$	5			5			ns
Latch time for new data, t_{latch} (see Note 4)		25			25			ns
Operating free-air temperature range, T_A (see Note 2)		-55			0			70 °C

- NOTES: 2. An SN54170 in the W package operating at free-air temperatures above 105°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 38°C/W.
3. Write select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{setup}(W)$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{hold}(W)$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
4. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{OH} = 5.5 \text{ V}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}$			30	µA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{SN54170}$		127§	140	mA
	See Note 5, SN74170		127§	150	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Typical supply current shown is an average for 50% duty cycle.

NOTE 5: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

TYPES SN54170, SN74170

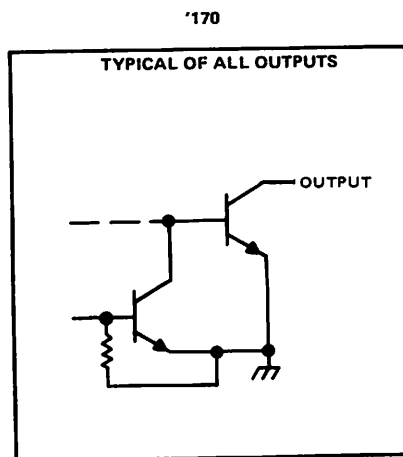
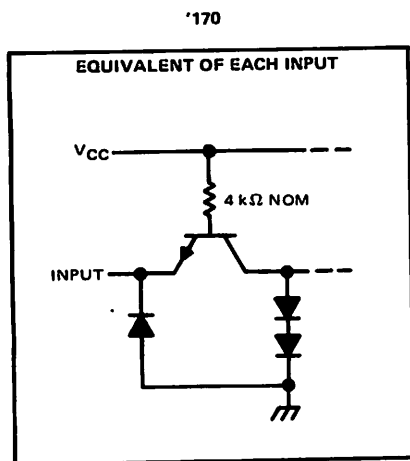
4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	Read enable	Any Q	CL = 15 pF, RL = 400 Ω, See Figures 1 and 2	10	15	ns	
tPHL				20	30		
tPLH	Read Select	Any Q		23	35	ns	
tPHL				30	40		
tPLH	Write enable	Any Q	CL = 15 pF, RL = 400 Ω, See Figures 1 and 3	25	40	ns	
tPHL				34	45		
tPLH	Data	Any Q		20	30	ns	
tPHL				30	45		

[†] t_{PLH} \equiv propagation delay time, low-to-high-level output
 t_{PHL} \equiv propagation delay time, high-to-low-level output

schematics of inputs and outputs



TYPES SN54LS170, SN74LS170

4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

		SN54LS170			SN74LS170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				4			8	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{setup}(D)$	10			10			ns
	Write select with respect to write enable, $t_{setup}(W)$	15			15			ns
Hold times, high- or low-level data (see Note 3 and Figure 2)	Data input with respect to write enable, $t_{hold}(D)$	15			15			ns
	Write select with respect to write enable, $t_{hold}(W)$	5			5			ns
Latch time for new data, t_{latch} (see Note 4)		25			25			ns
Operating free-air temperature range, T_A		-55		125	0		70	°C

- NOTES: 3. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{setup}(W)$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{hold}(W)$ will result in data being written into that location. Depending on the input conditions, one or a number of previous addresses may have been written into.
4. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS170			SN74LS170			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH}	High-level output current	$V_{CC} = \text{MIN}, V_{OH} = 5.5 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{IH} = 2 \text{ V}$			100			100	µA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I	Input current at maximum input voltage	Any D, R, or W GR or GW	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1	mA
					0.2			0.2	
I_{IH}	High-level input current	Any D, R, or W GR or GW	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20	µA
					40			40	
I_{IL}	Low-level input current	Any D, R, or W GR or GW	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4			-0.4	mA
					-0.8			-0.8	
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 6	25	40		25	40		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 6: I_{CC} is measured under the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

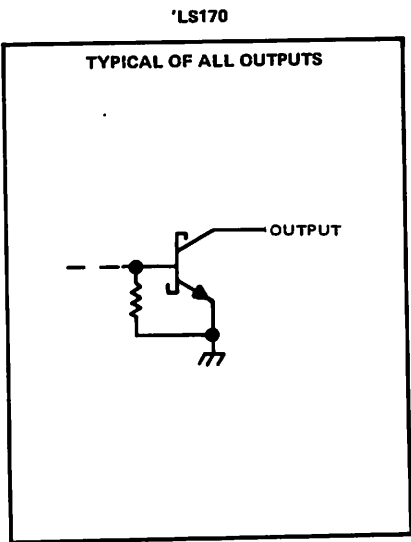
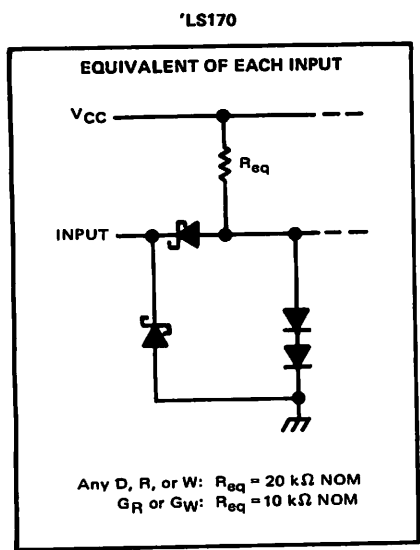
TYPES SN54LS170, SN74LS170
4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	Read enable	Any Q	CL = 15 pF, RL = 2 kΩ, See Figures 1 and 2	20	30	ns	
tPHL				20	30		
tPLH	Read select	Any Q		25	40	ns	
tPHL				24	40		
tPLH	Write enable	Any Q	CL = 15 pF, RL = 2 kΩ, See Figures 1 and 3	30	45	ns	
tPHL				26	40		
tPLH	Data	Any Q		30	45	ns	
tPHL				22	35		

† $t_{PLH} \equiv$ propagation delay time, low-to-high-level output
 $t_{PHL} \equiv$ propagation delay time, high-to-low-level output

schematics of inputs and outputs



TYPES SN54170, SN54LS170, SN74170, SN74LS170

4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

REVISED MARCH 1974

PARAMETER MEASUREMENT INFORMATION

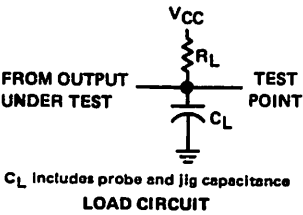


FIGURE 1

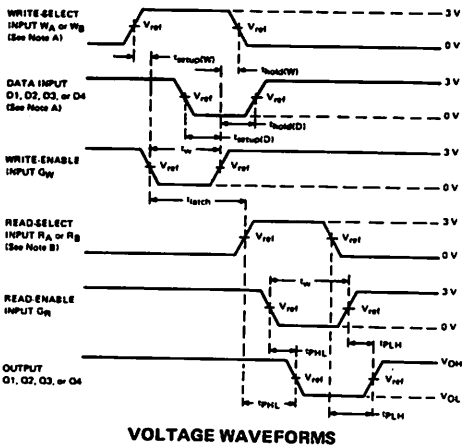


FIGURE 2

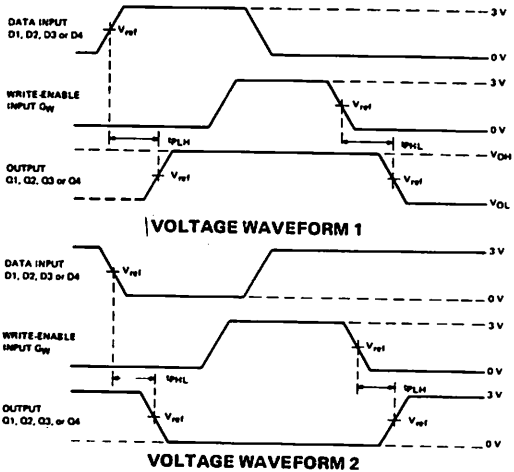
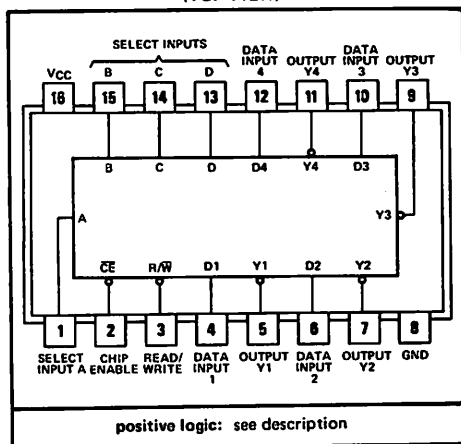


FIGURE 3

- NOTES:
- High-level input pulses at the select and data inputs are illustrated in Figure 2; however, times associated with low-level pulses are measured from the same reference points.
 - When measuring delay times from a read-select input, the read-enable input is low. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.
 - In Figure 3, each select address is tested. Prior to the start of each of the above tests, both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.
 - Input waveforms are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_{out} \approx 50 \Omega$, duty cycle $\leq 50\%$, $t_r \leq 10$ ns and $t_f \leq 10$ ns for '170, and $t_r \leq 15$ ns and $t_f \leq 6$ ns for 'LS170.
 - For '170, $V_{ref} = 1.5$ V; for 'LS170, $V_{ref} = 1.3$ V.

- Schottky-Clamped for High-Speed Buffer/Scratchpad Memory Systems:
Access from Chip-Enable Inputs . . . 12 ns Typ
Access from Address Inputs . . . 25 ns Typ
- Three-State Outputs Drive Bus-Organized Systems and/or Highly Capacitive Loads
- SN54S289, SN74S289 Are Functionally Equivalent, Have Open-Collector Outputs, and Replace Intel 3101A in Most Applications
- SN54S189 Is Guaranteed for Operation Over the Full Military Temperature Range of -55°C to 125°C
- Compatible with Most TTL and DTL Logic Circuits
- Chip-Enable Input Simplifies Word Expansion

SN54S189 . . . J OR W PACKAGE
SN74S189 . . . J OR N PACKAGE
(TOP VIEW)



description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four-bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature p-n-p input transistors that reduce the low-level input current requirement to a maximum of -0.25 milliamperes, only one-eighth that of a Series 54S/74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The three-state output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast-rise-time characteristic of the TTL totem-pole output. Systems utilizing data-bus lines with a defined pull-up impedance can employ the open-collector 'S289.

write cycle

The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the 'S189 outputs are bus-connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

read cycle

The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable input is low. When the chip-enable input is high, the outputs will be in the high-impedance state.

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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INCORPORATED
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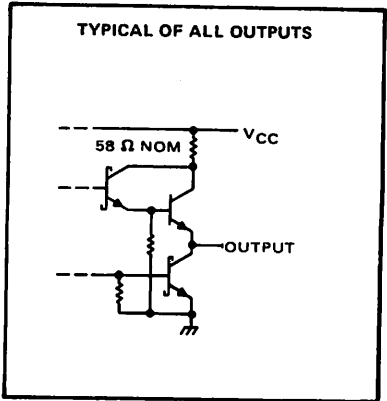
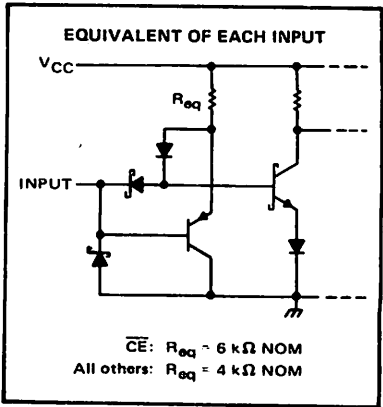
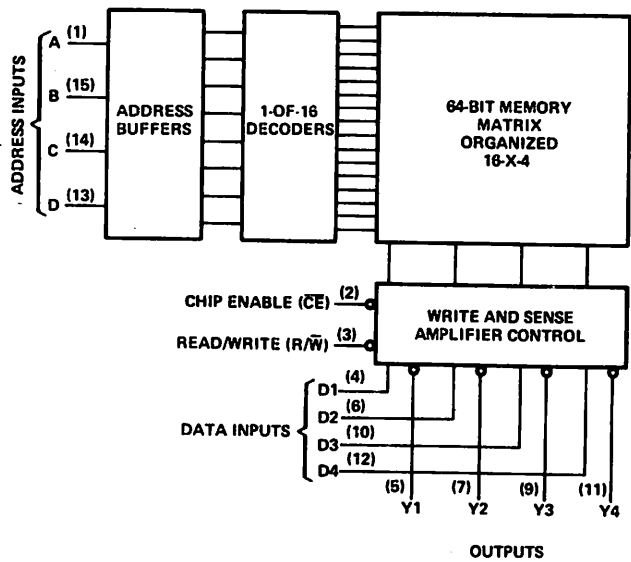
TYPES SN54S189, SN74S189
64-BIT RANDOM-ACCESS MEMORIES WITH 3-STATE OUTPUTS

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

H = high level, L = low level, X = irrelevant

The fast access time of the 'S189 makes it particularly attractive for implementing high-performance memory functions requiring access times on the order of 25 nanoseconds. The high capacitive-drive capability of the outputs permits expansion without additional output buffering. The unique functional capability of the 'S189 outputs being at a high impedance during writing combined with the data inputs being inhibited during reading means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

functional block diagram and schematics of inputs and outputs



TYPES SN54S189, SN74S189

64-BIT RANDOM-ACCESS MEMORIES WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54S189	-55°C to 125°C
SN74S189	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

			SN54S189			SN74S189			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V		
High-level output voltage, I_{OH}			-2			-6.5			V		
Low-level output current, I_{OL}			16			16			mA		
Width of write-enable pulse (read/write low), t_w			25			25			ns		
Setup time, t_{setup} (see Figure 1)	Address to read/write		0↓			0↓			ns		
	Data to read/write		25↑			25↑					
	Chip enable to read/write		0↓			0↓					
Hold time, t_{hold} (see Figure 1)	Address from read/write		0↑			0↑			ns		
	Data from read/write		0↑			0↑					
	Chip enable from read/write		0↑			0↑					
Operating free-air temperature, T_A			-55			125			0	70	°C

† The arrow indicates the transition of the read/write input used for reference: \uparrow for the low-to-high transition, \downarrow for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S189			SN74S189			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4	3.4		2.4	3.2		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$			0.5			0.45	V
I_{OZH} Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_O = 2.4 \text{ V}$			50			50	μA
I_{OZL} Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_O = 0.5 \text{ V}$			-50			-50	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			25			25	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-250			-250	μA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-30		-100	-30		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		75	110		75	110	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Duration of the short-circuit should not exceed one second.

NOTES: 1. All voltage values are with respect to network ground terminal.

2. I_{CC} is measured with the read/write and chip-enable inputs grounded, all other inputs at 4.5 V, and the outputs open.

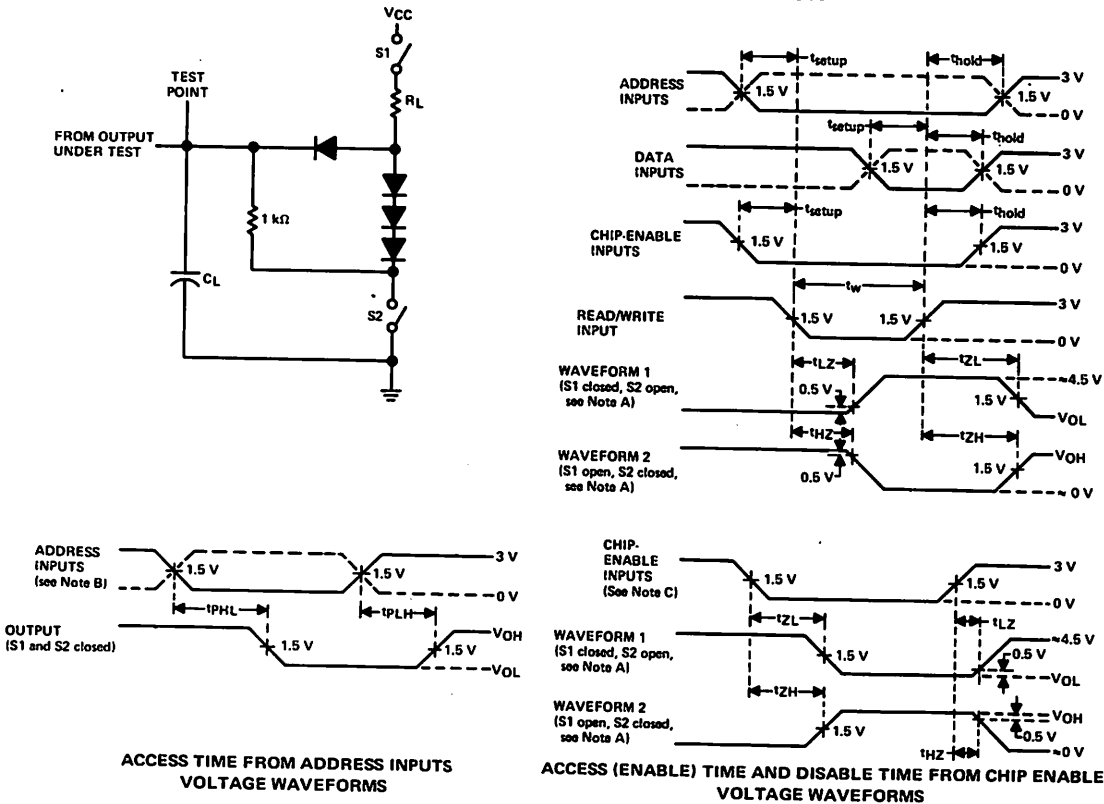
TYPES SN54S189, SN74S189
64-BIT RANDOM-ACCESS MEMORIES WITH 3-STATE OUTPUTS

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S189		SN74S189		UNIT
				TYP†	MAX	TYP†	MAX	
tPLH	Propagation delay time, low-to-high-level output	Access times	CL = 30 pF, RL = 280 Ω, See Figure 1	25	50	25	35	ns
tPHL	Propagation delay time, high-to-low-level output	from address		25	50	25	35	
tZH	Output enable time to high level	Access times from		12	25	12	17	ns
tZL	Output enable time to low level	chip enable		12	25	12	17	
tZH	Output enable time to high level	Sense recovery times		22	40	22	35	ns
tZL	Output enable time to low level	from read/write		22	40	22	35	
tHZ	Output disable time from high level	Disable times from	CL = 5 pF, RL = 280 Ω, See Figure 1	12	25	12	17	ns
tLZ	Output disable time from low level	chip enable		12	25	12	17	
tHZ	Output disable time from high level	Disable times		12		12		ns
tLZ	Output disable time from low level	from read/write		12		12		

†All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
B. When measuring delay times from address inputs, the chip-enable input is low and the read/write input is high.
C. When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r < 2.5\text{ ns}$, $t_f < 2.5\text{ ns}$, $\text{PRR} < 1\text{ MHz}$, and $Z_{out} \approx 50\ \Omega$.

FIGURE 1

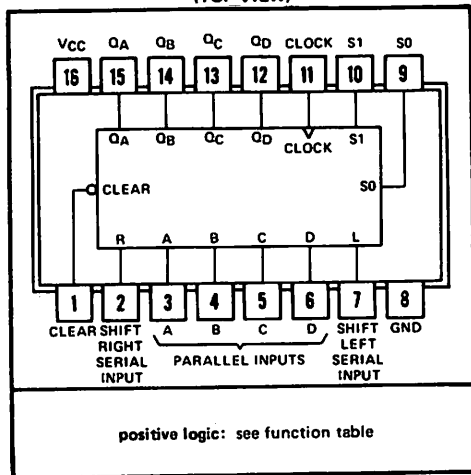
TYPES SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

BULLETIN NO. DL-S 7411866, MARCH 1974

- Parallel Inputs and Outputs
- Four Operating Modes:
 - Synchronous Parallel Load
 - Right Shift
 - Left Shift
 - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'194	36 MHz	195 mW
'LS194A	36 MHz	75 mW
'S194	105 MHz	425 mW

SN54194, SN54LS194A, SN54S194 ... J OR W PACKAGE
SN74194, SN74LS194A, SN74S194 ... J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

- Parallel (broadside) load
- Shift right (in the direction Q_A toward Q_D)
- Shift left (in the direction Q_D toward Q_A)
- Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1 , high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the SN54194/SN74194 should be changed only while the clock input is high.

FUNCTION TABLE

FUNCTION TABLE													
INPUTS							OUTPUTS						
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q _A	Q _B	Q _C	Q _D
	S ₁	S ₀		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}
H	H	L	↑	H	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

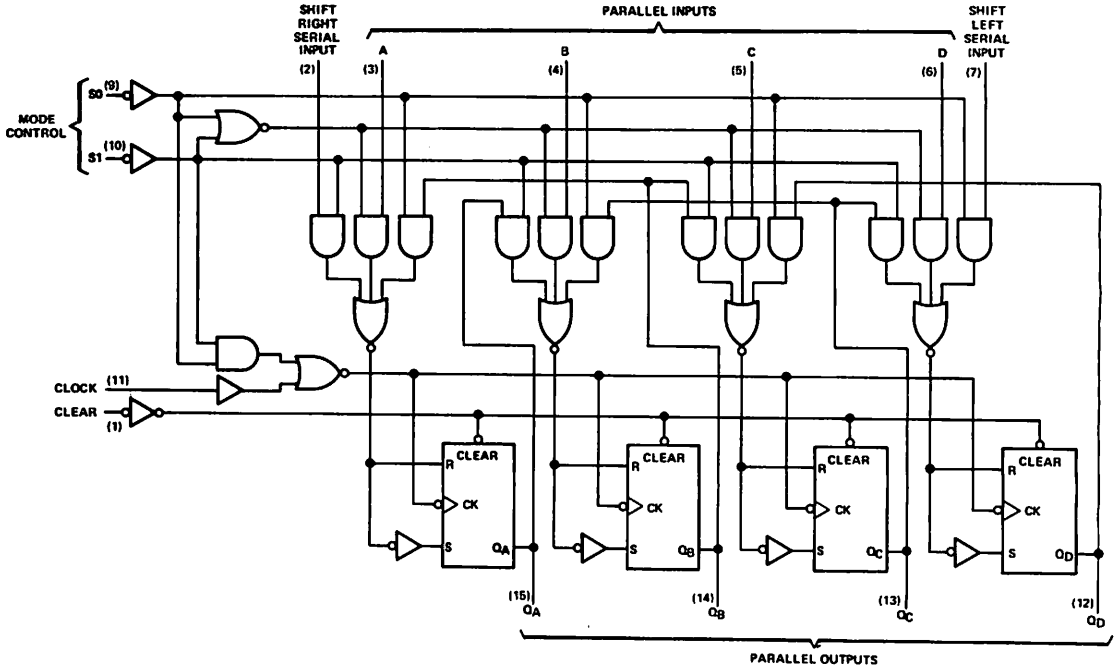
$Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$ = the level of $Q_A, Q_B, Q_C,$ or Q_D , respectively, before the indicated steady-state input conditions were established.

$Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}$ = the level of $Q_A, Q_B, Q_C,$ respectively, before the most-recent ↑ transition of the clock.

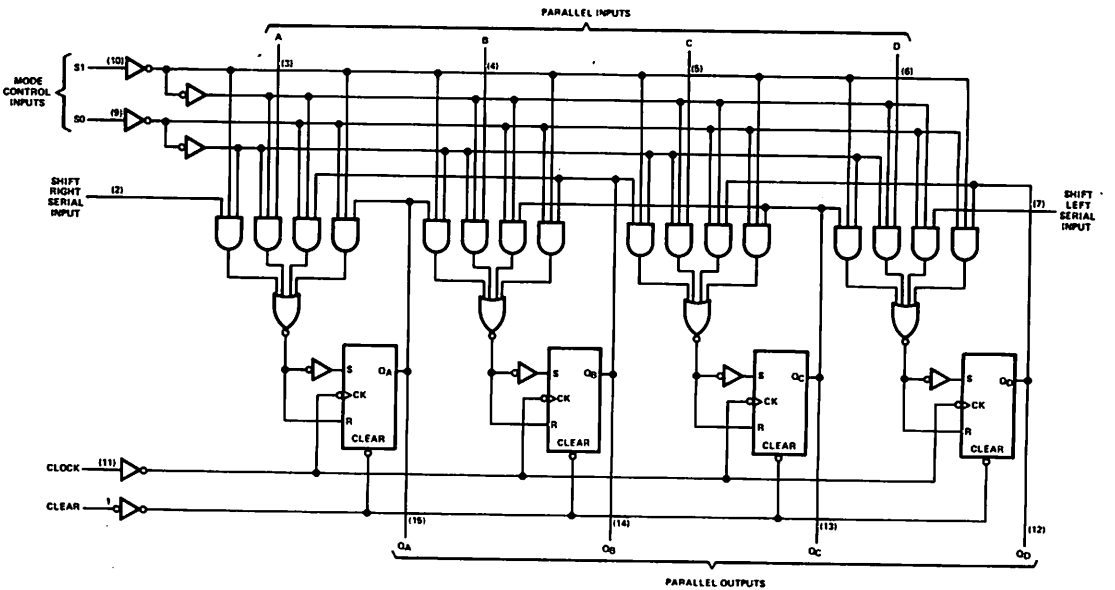
**TYPES SN54194, SN54LS194A, SN54S194,
SN74194, SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS**

functional block diagrams

'194

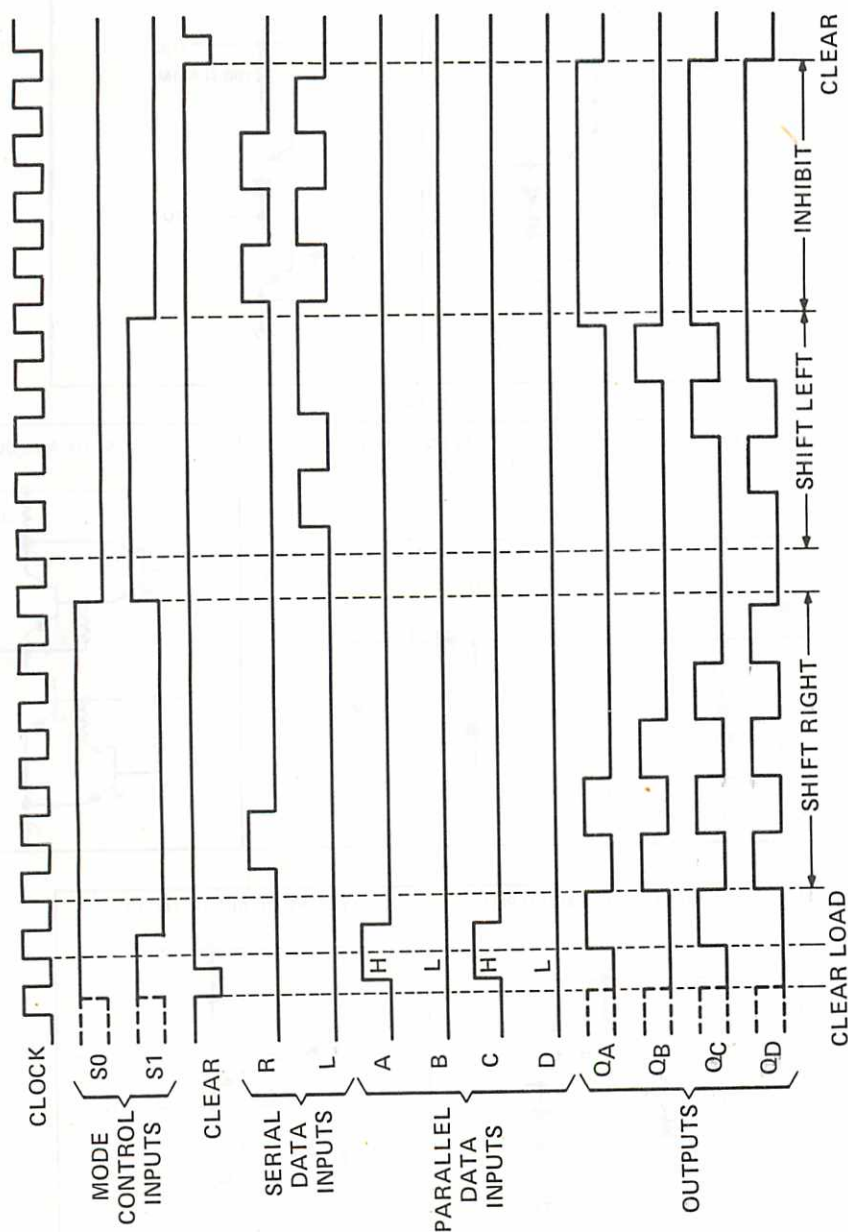


'LS194A, 'S194



**TYPES SN54194, SN54LS194A, SN54S194,
SN74194, SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS**

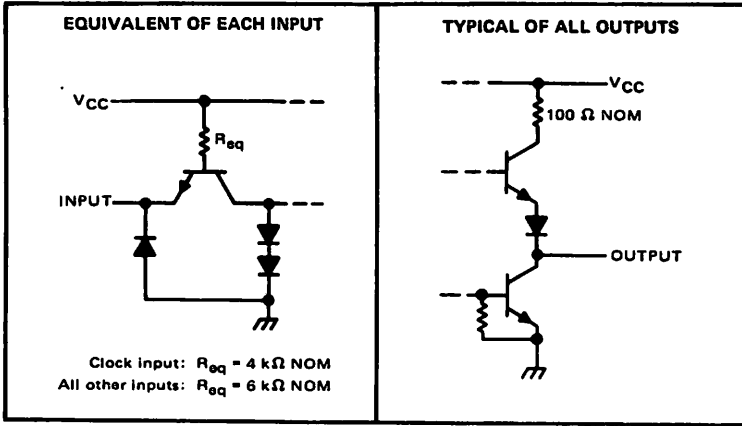
typical clear, load, right-shift, left-shift, inhibit, and clear sequences



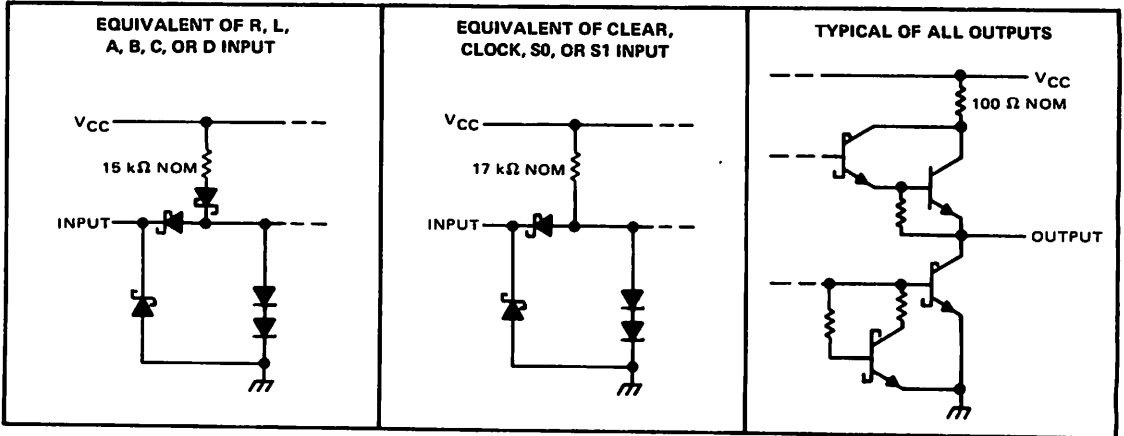
**TYPES SN54194, SN54LS194A, SN54S194,
SN74194, SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS**

schematics of inputs and outputs

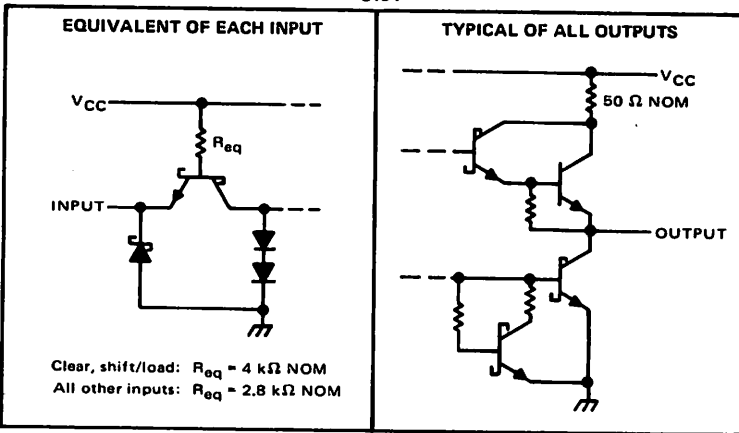
'194



'LS194A



'S194



TYPES SN54194, SN74194

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

REVISED MARCH 1974

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54194	-55°C to 125°C
SN74194	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54194			SN74194			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_W	20			20			ns
Setup time, t_{setup}	Mode control			30			ns
	Serial and parallel data			20			ns
	Clear inactive-state			25			ns
Hold time at any input, t_{hold}	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54194			SN74194			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-57	-18		-57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	39		63	39		63	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 400 \Omega$, See Figure 1	25	36		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			14	22	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			17	26	ns

TYPES SN54LS194A, SN74LS194A

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS194A	-55°C to 125°C
SN74LS194A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS194A			SN74LS194A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-400			-400			μ A
Low-level output current, I_{OL}		4			8			mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_W		20			20			ns
Setup time, t_{setup}	Mode control	30			30			ns
	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			ns
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		-55			0			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS194A			SN74LS194A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage		0.7			0.8			V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$	-1.5			-1.5			V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}$ 0.25		0.4	$I_{OL} = 4 \text{ mA}$ 0.25		0.4	V
		$I_{OL} = 8 \text{ mA}$			$I_{OL} = 8 \text{ mA}$		0.35	0.5
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$	0.1			0.1			mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$	20			20			μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	-0.4			-0.4			mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-6		-40	-5		-42	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	15		23	15		23	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Figure 1	25	36		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			14	22	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			17	22	ns

TENTATIVE DATA

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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TYPES SN54S194, SN74S194

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

REVISED MARCH 1974

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S194	-55°C to 125°C
SN74S194	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S194			SN74S194			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Clock frequency, f_{clock}	0		70	0		70	MHz
Width of clock pulse, $t_w(\text{clock})$	7			7			ns
Width of clear pulse, $t_w(\text{clear})$	12			12			ns
Setup time, t_{setup}	Mode control			11			ns
	Serial and parallel data			5			ns
	Clear inactive-state			9			ns
Hold time at any input, t_{hold}	3			3			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S194			SN74S194			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			50			50	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-2			-2	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		85	135		85	135	mA
	$V_{CC} = \text{MAX}, T_A = 125^\circ\text{C}, \text{ W package}$			110				
	See Note 2							

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

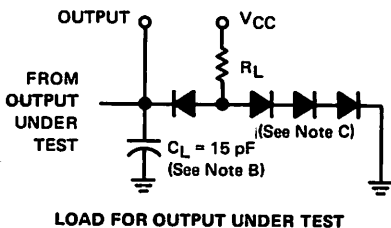
NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applies to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 280 \Omega, \text{ See Figure 1}$	70	105		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			12.5	18.5	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock		4	8	12	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock		4	11	16.5	ns

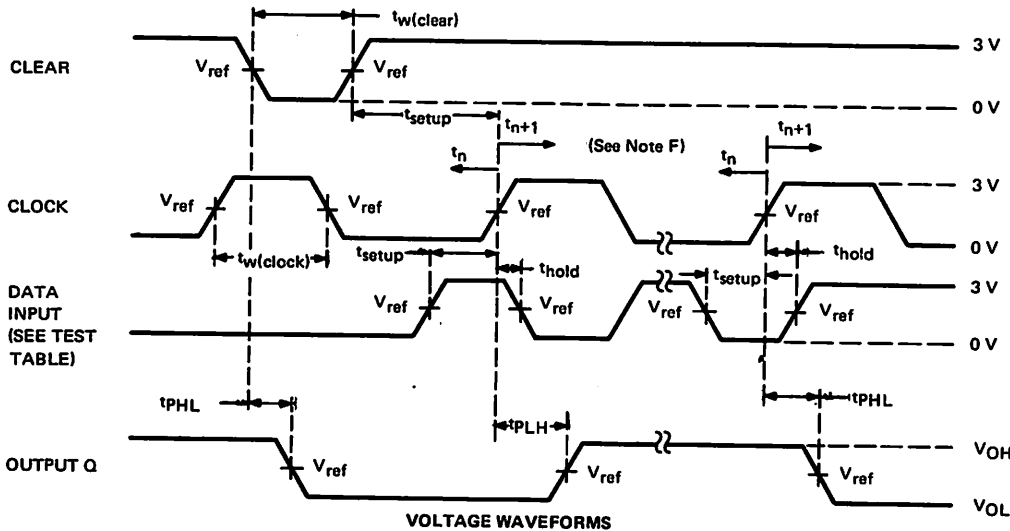
TYPES SN54194, SN54LS194A, SN54S194,
SN74194, SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	QA at tn+1
B	4.5 V	4.5 V	QB at tn+1
C	4.5 V	4.5 V	QC at tn+1
D	4.5 V	4.5 V	QD at tn+1
L Serial Input	4.5 V	0 V	QA at tn+4
R Serial Input	0 V	4.5 V	QD at tn+4



- NOTES: A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50 \Omega$ and $PRR \leq 1 \text{ MHz}$. For '194, $t_r \leq 7 \text{ ns}$ and $t_f \leq 7 \text{ ns}$. For 'LS194A, $t_r \leq 15 \text{ ns}$ and $t_f \leq 6 \text{ ns}$. For 'S194, $t_r \leq 2.5 \text{ ns}$ and $t_f \leq 2.5 \text{ ns}$. When testing f_{max} , vary PRR.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or 1N916.
- D. A clear pulse is applied prior to each test.
- E. For '194 and 'S194, $V_{ref} = 1.5 \text{ V}$; for 'LS194A, $V_{ref} = 1.3 \text{ V}$.
- F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+4} with a functional test.
- G. t_n = bit time before clocking transition.
 t_{n+1} = bit time after one clocking transition.
 t_{n+4} = bit time after four clocking transitions.

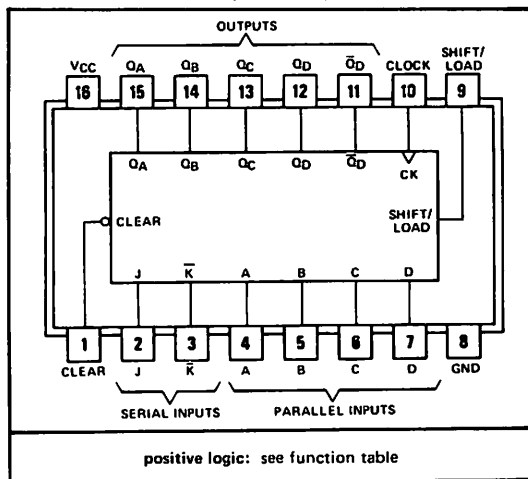
FIGURE 1—SWITCHING TIMES

TYPES SN54195, SN54LS195A, SN54S195, SN74195, SN74LS195A, SN74S195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

BULLETIN NO. DL-S 7411820, MARCH 1974

SN54195, SN54LS195A, SN54S195 ... J OR W PACKAGE
SN74195, SN74LS195A, SN74S195 ... J OR N PACKAGE
(TOP VIEW)

- Synchronous Parallel Load
- Positive-Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- J and \bar{K} Inputs to First Stage
- Complementary Outputs from Last Stage
- For Use in High-Performance:
Accumulators/Processors
Serial-to-Parallel, Parallel-to-Serial Converters



description

These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

- Parallel (broadside) load
- Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

The high-performance 'S195, with a 105-megahertz typical maximum shift-frequency, is particularly attractive for very-high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

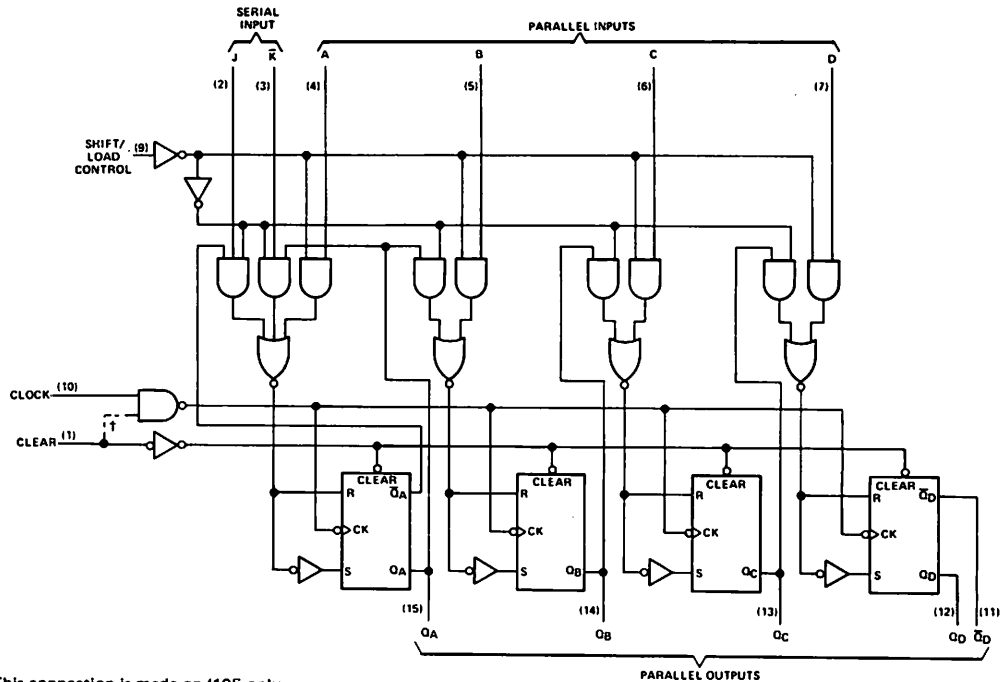
FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q _A	Q _B	Q _C	Q _D	\overline{Q}_D
			J	\overline{K}	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	\overline{d}
H	H	L	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	\overline{Q}_{D0}
H	H	↑	L	H	X	X	X	X	Q _{A0}	Q _{A0}	Q _{Bn}	Q _{Cn}	\overline{Q}_{Cn}
H	H	↑	L	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}	\overline{Q}_{Cn}
H	H	↑	H	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}	\overline{Q}_{Cn}
H	H	↑	H	L	X	X	X	X	\overline{Q}_{An}	Q _{An}	Q _{Bn}	Q _{Cn}	\overline{Q}_{Cn}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively
 $Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$ = the level of Q_A, Q_B, Q_C , or Q_D , respectively, before the indicated steady-state input conditions were established
 Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B , or Q_C , respectively, before the most-recent transition of the clock

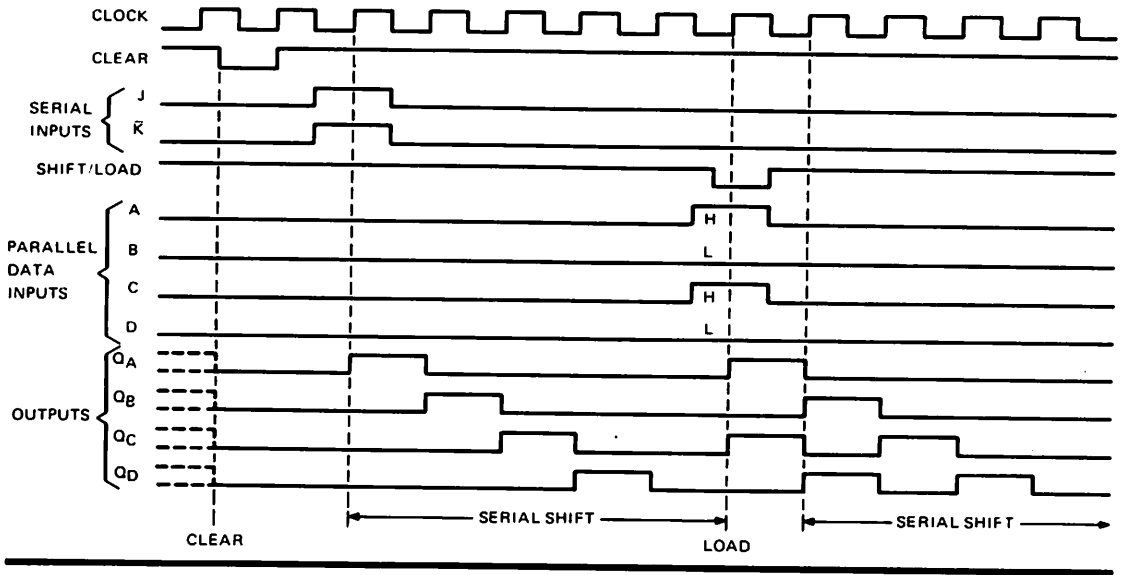
TYPES SN54195, SN54LS195A, SN54S195, SN74195, SN74LS195A, SN74S195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

functional block diagram



† This connection is made on '195 only.

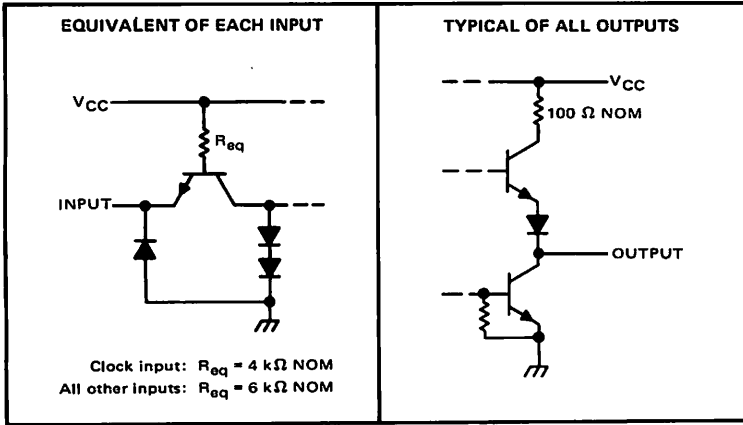
typical clear, shift, and load sequences



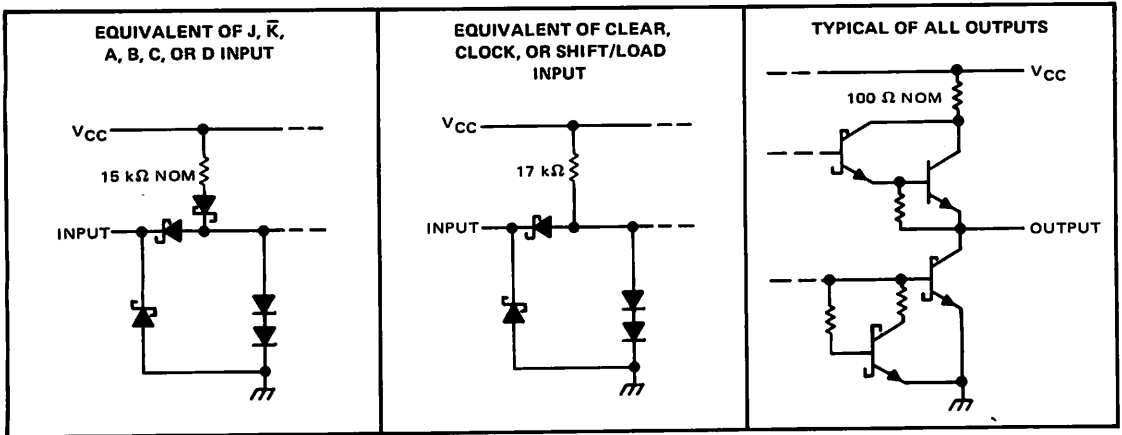
TYPES SN54195, SN54LS195A, SN54S195, SN74195, SN74LS195A, SN74S195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

schematics of inputs and outputs

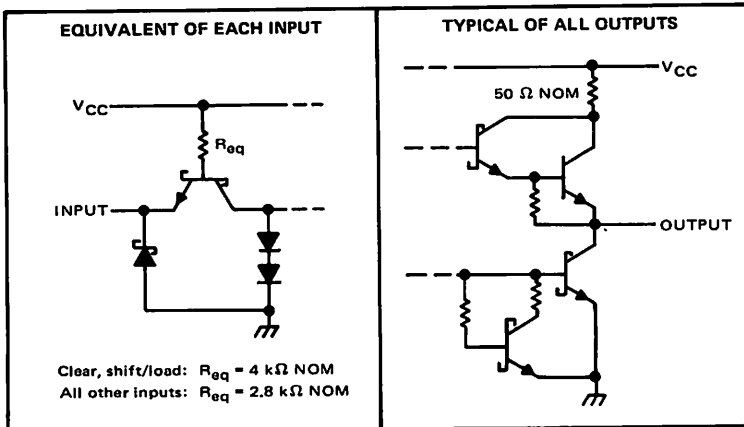
'195



'LS195A



'S195



3

TYPES SN54195, SN74195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

REVISED MARCH 1974

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Table with 2 columns: Parameter and Value. Parameters include Supply voltage (VCC), Input voltage, Operating free-air temperature range (SN54195, SN74195), and Storage temperature range.

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

Table with 4 columns: Parameter, SN54195 (MIN, NOM, MAX), SN74195 (MIN, NOM, MAX), and UNIT. Parameters include Supply voltage, High-level output current, Low-level output current, Clock frequency, Width of clock input pulse, Width of clear input pulse, Setup time, Shift/load, Shift/load release time, Serial and parallel data hold time, and Operating free-air temperature.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Table with 5 columns: PARAMETER, TEST CONDITIONS†, MIN, TYP‡, MAX, and UNIT. Parameters include V_IH, V_IL, V_I, V_OH, V_OL, I_I, I_IH, I_IL, I_OS, and I_CC.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at VCC = 5 V, TA = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, ICC is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, VCC = 5 V, TA = 25°C

Table with 5 columns: PARAMETER, TEST CONDITIONS, MIN, TYP, MAX, and UNIT. Parameters include f_max, t_PHL (high-to-low), t_PLH (low-to-high), and t_PHL (high-to-low).

TYPES SN54LS195A, SN74LS195A

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS195A	-55°C to 125°C
SN74LS195A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS195A			SN74LS195A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-400			-400			μ A
Low-level output current, I_{OL}		4			8			mA
Clock frequency, f_{clock}		0	20		0	20		MHz
Width of clock or clear pulse, $t_w(\text{clock})$		16			16			ns
Width of clear input pulse, $t_w(\text{clear})$		12			12			ns
Setup time, t_{setup} (see Figure 1)	Shift/load	25			25			ns
	Serial and parallel data	15			15			
	Clear inactive-state	25			25			
Shift/load release time, $t_{release}$ (see Figure 1)		10			10			ns
Serial and parallel data hold time, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		-55 125			0 70			$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS195A			SN74LS195A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage								V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}, I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-6		-40	-5		-42	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		14	21		14	21	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ See Figure 1}$	30	39		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			14	22	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			17	26	ns

TENTATIVE DATA

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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S-227

TYPES SN54S195, SN74S195

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

REVISED MARCH 1974

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S195	-55°C to 125°C
SN74S195	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S195			SN74S195			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-1			-1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		70	0		70	MHz
Width of clock input pulse, $t_w(\text{clock})$		7			7			ns
Width of clear input pulse, $t_w(\text{clear})$		12			12			ns
Setup time, t_{setup} (see Figure 1)	Shift/load	11			11			ns
	Serial and parallel data	5			5			
	Clear inactive-state	9			9			
Shift/load release time, t_{release} (see Figure 1)				6			6	ns
Serial and parallel data hold time, t_{hold} (see Figure 1)		3			3			ns
Operating free-air temperature, T_A		-55		125	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	SN54S195 SN74S195	2.5 2.7	3.4 3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$				0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$				50	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$				-2	mA
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$		-40		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2	SN54S195 SN74S195	70 70	99 109		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

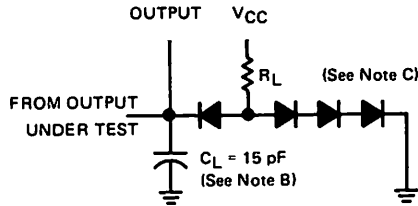
NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

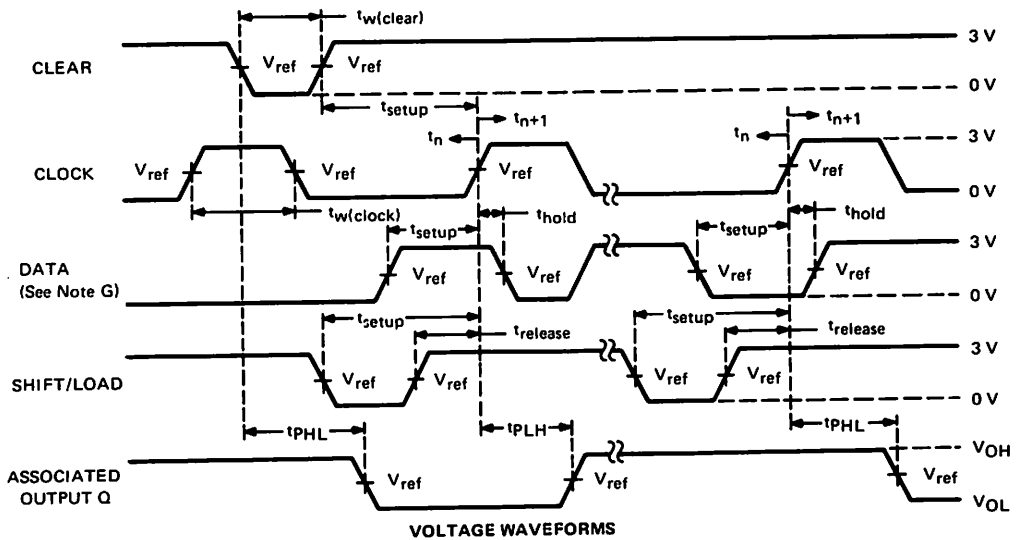
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	$C_L = 15 \text{ pF},$ $R_L = 280 \Omega,$ See Figure 1		70	105		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear				12.5	18.5	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock				8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock				11	16.5	ns

TYPES SN54195, SN54LS195A, SN54S195, SN74195, SN74LS195A, SN74S195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST



- NOTES: A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50 \Omega$ and $PRR \leq 1 \text{ MHz}$. For '195, $t_r \leq 7 \text{ ns}$ and $t_f \leq 7 \text{ ns}$. For 'LS195A, $t_r \leq 15 \text{ ns}$ and $t_f \leq 6 \text{ ns}$. For 'S195, $t_r = 2.5 \text{ ns}$ and $t_f = 2.5 \text{ ns}$. When testing t_{max} , vary the clock PRR.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064.
- D. A clear pulse is applied prior to each test.
- E. For '195 and 'S195, $V_{ref} = 1.5 \text{ V}$; for 'LS195A, $V_{ref} = 1.3 \text{ V}$.
- F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+4} with a functional test.
- G. J and K inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.
- H. t_n = bit time before clocking transition.
 t_{n+1} = bit time after one clocking transition.
 t_{n+4} = bit time after four clocking transitions.

FIGURE 1—SWITCHING TIMES

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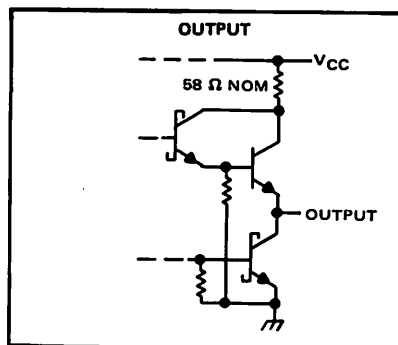
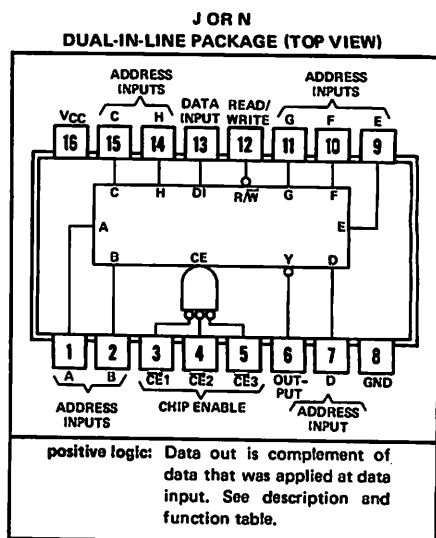
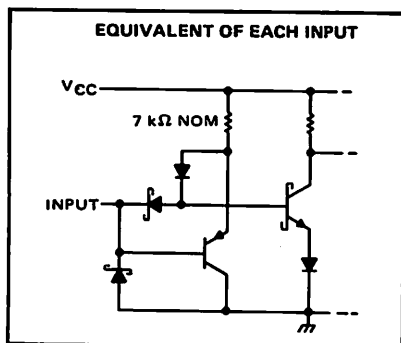
S-229

- **Plug In Replacement for SN74200**
- **Fully Decoded, Organized as 256 Words of One Bit Each**
- **Schottky-Clamped for High-Speed Memory Systems:**
 - Access from Chip-Enable Inputs . . . 13 ns Typical**
 - Access from Address Inputs . . . 42 ns Typical**
 - Power Dissipation . . . 1.95 mW/Bit Typical**
- **Three-State Output for Driving Bus-Organized Systems and/or Highly Capacitive Loads**
- **Compatible with Most TTL and DTL Logic Circuits**
- **Multiple Chip-Enable Inputs to Minimize External Decoding**

description

This 256-bit active-element memory is a monolithic transistor-transistor logic (TTL) array organized as 256 words of one bit each. It is fully decoded and has three gated chip-enable inputs to simplify decoding required to achieve the desired system organization. The SN74S201 features a three-state output and is functionally equivalent to both the SN74200 and the SN74S200.

schematics of inputs and outputs



write cycle

The complement of the information at the data input is written into the selected location when all chip-enable inputs and the read/write input are low. While the read/write input is low, the output is in the high-impedance state. When a number of outputs are bus-connected, this high-impedance output state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

read cycle

The stored information (complement of information applied at the data input during the write cycle) is available at the output when the read/write input is high and the three chip-enable inputs are low. When any one of the chip-enable inputs is high, the output will be in the high-impedance state.

FUNCTION TABLE

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE†	READ/ WRITE	
Write (Store Complement of Data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

H = high level, L = low level, X = irrelevant

† For chip-enable: $\overline{\text{L}}$ = all $\overline{\text{CE}}$ inputs low, H = one or more $\overline{\text{CE}}$ inputs high.

TENTATIVE DATA SHEET

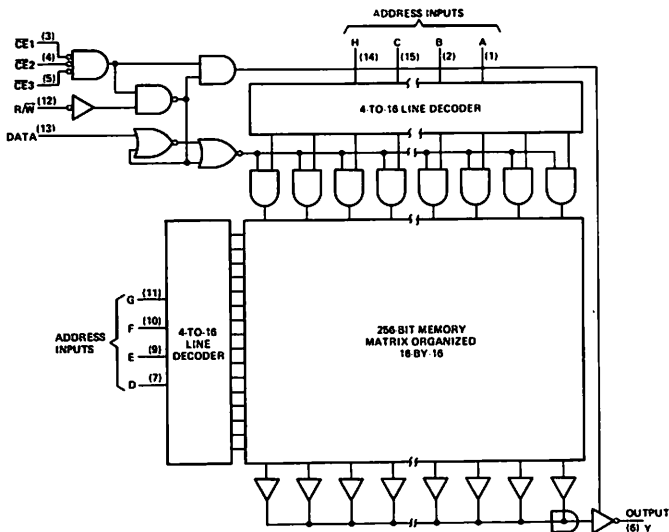
S-230

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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TYPE SN74S201 256-BIT RANDOM-ACCESS MEMORY WITH 3-STATE OUTPUT

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output voltage, I_{OH}				-10.3	mA
Low-level output current, I_{OL}				16	mA
Width of write-enable pulse (read/write low), t_w		65			ns
Setup time, t_{setup}	Address to read/write	0↓			ns
	Data to read/write	65↑			
	Chip enable to read/write	0↓			
Hold time, t_{hold}	Address from read/write	0↑			ns
	Data from read/write	0↑			
	Chip enable from read/write	0↑			
Operating free-air temperature, T_A		0		70	°C

↑↓ The arrow indicates the transition of the read/write input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

TYPE SN74S201

256-BIT RANDOM-ACCESS MEMORY WITH 3-STATE OUTPUT

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{IH} High-level input voltage		2			V
V _{IL} Low-level input voltage				0.8	V
V _I Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.2	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -10.3 mA	2.4	2.9		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA	0.38	0.45		V
I _{OZH} Off-state output current, high-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = 0.8 V, V _O = 2.4 V			40	µA
I _{OZL} Off-state output current, low-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = 0.8 V, V _O = 0.4 V			-40	µA
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1	mA
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.7 V			25	µA
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.5 V			-250	µA
I _{OS} Short-circuit output current§	V _{CC} = MAX	-30		-100	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 2	100		140	mA

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
t _{PLH} Propagation delay time, low-to-high-level output	C _L = 15 pF, R _L = 400 Ω, See Note 3	42	65		ns
t _{PHL} Propagation delay time, high-to-low-level output		42	65		
t _{ZH} Output enable time to high level		13	30		ns
t _{ZL} Output enable time to low level		13	30		
t _{ZH} Output enable time to high level		20	40		ns
t _{ZL} Output enable time to low level		20	40		
t _{HZ} Output disable time from high level	C _L = 5 pF, R _L = 400 Ω, See Note 3	10	20		ns
t _{LZ} Output disable time from low level		8	20		
t _{HZ} Output disable time from high level		11	35		ns
t _{LZ} Output disable time from low level		15	35		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Duration of the short circuit should not exceed one second.

NOTES: 2. I_{CC} is measured with all chip-enable inputs grounded, all other inputs at 4.5 V, and the output open.

3. Load circuit and voltage waveforms are the same as those shown for the SN54S189, SN74S189 page number S-214 except that for the input waveforms: t_r ≤ 7 ns, t_f ≤ 7 ns.

TYPES SN54246 THRU SN54249, SN54LS247 THRU SN54LS249, SN74246 THRU SN74249, SN74LS247 THRU SN74LS249 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

BULLETIN NO. 'DL-S 7412078, MARCH 1974

'246, '247, 'LS247
feature

'248, 'LS248
feature

'249, 'LS249
feature

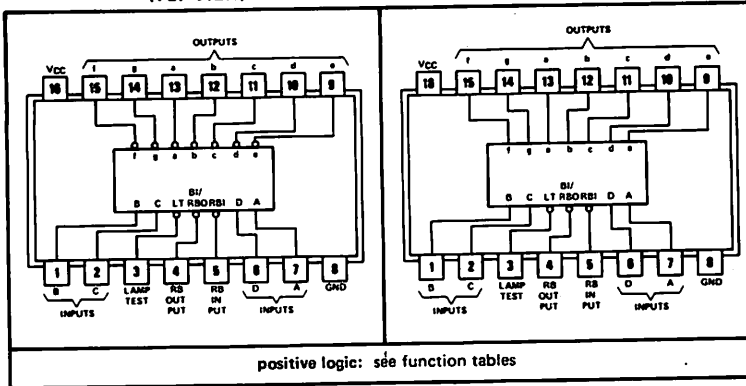
- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- Open-Collector Outputs
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

- All Circuit Types Feature Lamp Intensity Modulation Capability

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN54246	low	open-collector	40 mA	30 V	320 mW	J, W
SN54247	low	open-collector	40 mA	15 V	320 mW	J, W
SN54248	high	2-k Ω pull-up	6.4 mA	5.5 V	265 mW	J, W
SN54249	high	open-collector	10 mA	5.5 V	265 mW	J, W
SN54LS247	low	open-collector	12 mA	15 V	35 mW	J, W
SN54LS248	high	2-k Ω pull-up	2 mA	5.5 V	125 mW	J, W
SN54LS249	high	open-collector	4 mA	5.5 V	40 mW	J, W
SN74246	low	open-collector	40 mA	30 V	320 mW	J, N
SN74247	low	open-collector	40 mA	15 V	320 mW	J, N
SN74248	high	2-k Ω pull-up	6.4 mA	5.5 V	265 mW	J, N
SN74249	high	open-collector	10 mA	5.5 V	265 mW	J, N
SN74LS247	low	open-collector	24 mA	15 V	35 mW	J, N
SN74LS248	high	2-k Ω pull-up	6 mA	5.5 V	125 mW	J, N
SN74LS249	high	open-collector	8 mA	5.5 V	40 mW	J, N

'246, '247, 'LS247
(TOP VIEW)

'248, '249, 'LS248, 'LS249
(TOP VIEW)



description

The '246 through '248 are electrically and functionally identical to the SN5446A/SN7446A, SN5447A/SN7447A, and SN5448/SN7448, respectively, and have the same pin assignments as their equivalents. Also the 'LS247 and 'LS248 are electrically and functionally identical to the SN54LS47/SN74LS47 and SN54LS48/SN74LS48, respectively, and have the same pin assignments as their equivalents. They can be used interchangeably in present or future designs to offer designers a choice between two indicator fonts. The '249 and 'LS249 are 16-pin versions of the 14-pin SN5449 and SN54LS49/SN74LS49, respectively. Included in the '249 and 'LS249 circuits is the full functional capability for lamp test and ripple blanking, which is not available in the '49 and 'LS49 circuits. The '46A, '47A, '48, '49, 'LS47, 'LS48, and 'LS49 compose the *b* and the *q* without tails and the '246 through '249 and 'LS247, 'LS248, and 'LS249

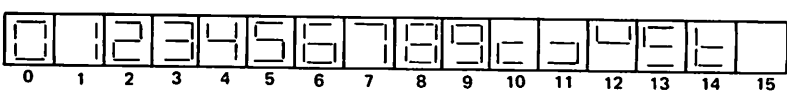
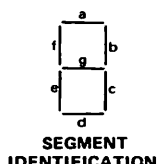
**TYPES SN54246 THRU SN54249, SN54LS247 THRU SN54LS249,
SN74246 THRU SN74249, SN74LS247 THRU SN74LS249
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

description (continued)

compose the 6 and the 9 with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The '246, '247, and 'LS247 feature active-low outputs designed for driving indicators directly, and the '248, '249, 'LS248, and 'LS249 feature active-high outputs for driving lamp buffers. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

All of these circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

Series 54 and Series 54LS devices are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74 and Series 74LS devices are characterized for operation from 0°C to 70°C.



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

'246, '247, 'LS247
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

- NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

TYPES SN54246 THRU SN54249, SN54LS247 THRU SN54LS249,
SN74246 THRU SN74249, SN74LS247 THRU SN74LS249
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

'248, '249, 'LS248, 'LS249
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	L	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	H	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	1
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

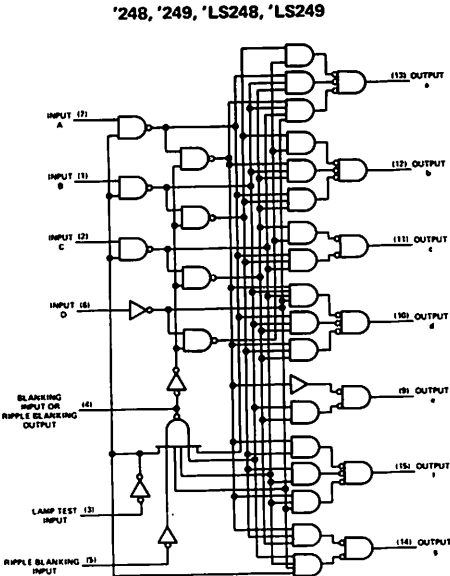
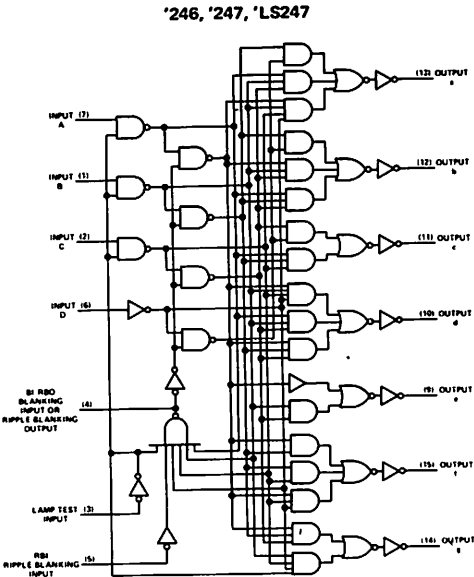
NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).

4. When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

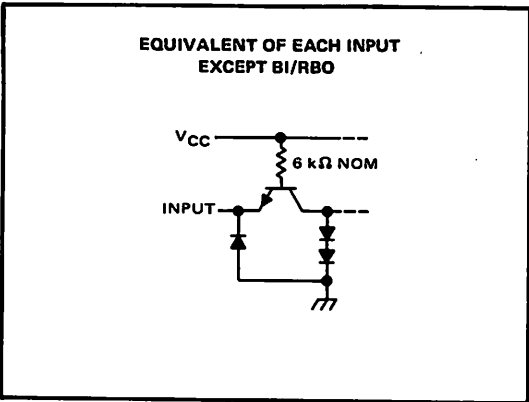


TYPES SN54246 THRU SN54249, SN74246 THRU SN74249

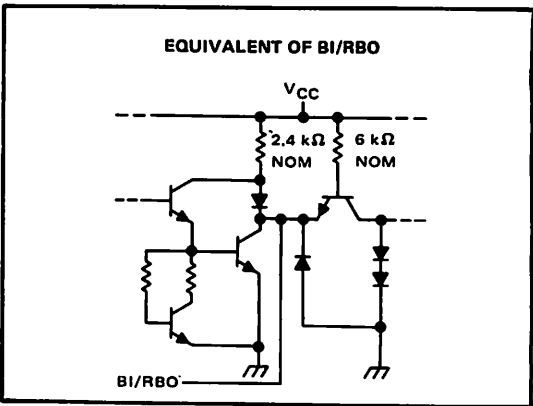
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

schematics of inputs and outputs

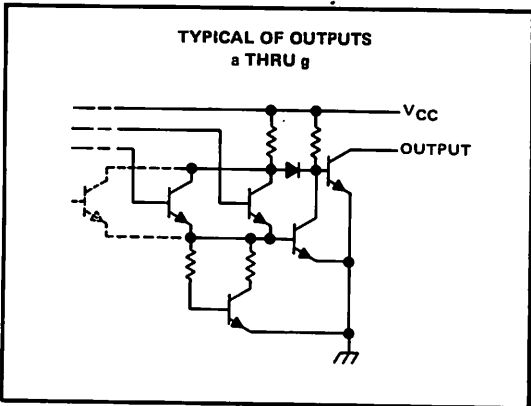
'246, '247, '248, '249



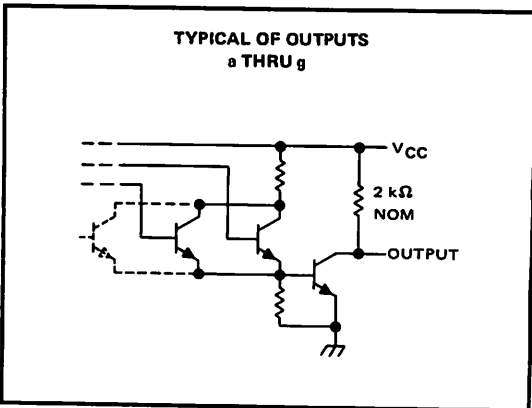
'246, '247, '248, '249



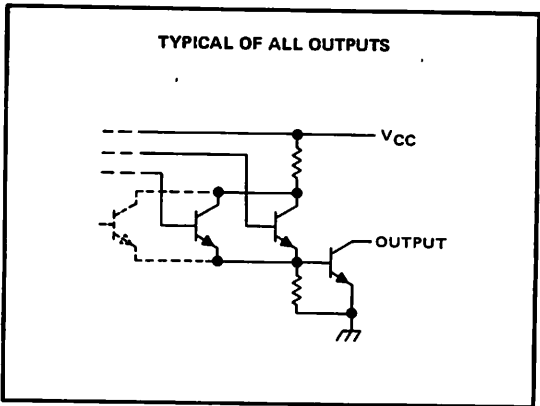
'246, '247



'248



'249

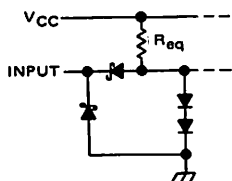


TYPES SN54LS247 THRU SN54LS249, SN74LS247 THRU SN74LS249 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

schematics of inputs and outputs

'LS247, 'LS248, 'LS249

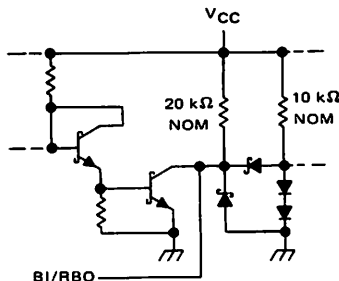
EQUIVALENT OF EACH INPUT
EXCEPT BI/RBO



LT and RBI: $R_{eq} = 20 \text{ k}\Omega \text{ NOM}$
A, B, C, and D: $R_{eq} = 25 \text{ k}\Omega \text{ NOM}$

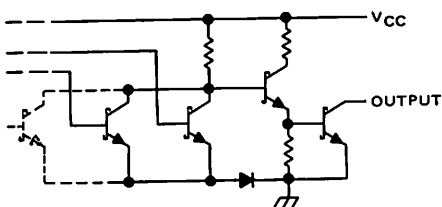
'LS247, 'LS248, 'LS249

EQUIVALENT OF BI/RBO



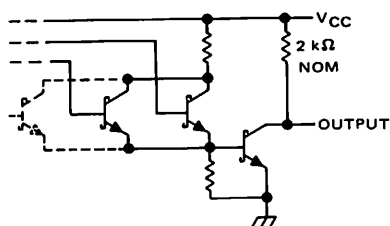
'LS247

TYPICAL OF OUTPUTS
a THRU g



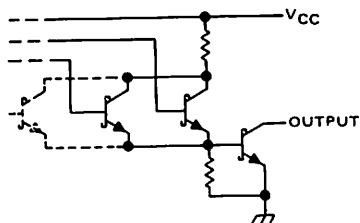
'LS248

TYPICAL OF OUTPUTS
a THRU g



'LS249

TYPICAL OF OUTPUTS
a THRU g



TYPES SN54246, SN54247, SN74246, SN74247
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

REVISED MARCH 1974

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54246, SN54247	-55°C to 125°C
SN74246, SN74247	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54246			SN54247			SN74246			SN74247			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			30			15			30			15	V
On-state output current, $I_{O(on)}$	a thru g			40			40			40			40	mA
High-level output current, I_{OH}	BI/RBO			-200			-200			-200			-200	μA
Low-level output current, I_{OL}	BI/RBO			8			8			8			8	mA
Operating free-air temperature, T_A		-55		125	-55		125	0		70	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				1.5 V	V
V_{OH}	High-level output voltage	BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -200 \mu\text{A}$		2.4	3.7		V
V_{OL}	Low-level output voltage	BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 8 \text{ mA}$		0.27	0.4		V
$I_{O(off)}$	Off-state output current	a thru g	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{O(off)} = \text{MAX}$				250	μA
$V_{O(on)}$	On-state output voltage	a thru g	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{O(on)} = 40 \text{ mA}$		0.3	0.4		V
I_I	Input current at maximum input voltage	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$				40	μA
I_{IL}	Low-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				-1.6	mA
		BI/RBO					-4	
I_{OS}	Short-circuit output current	BI/RBO	$V_{CC} = \text{MAX}$				-4	mA
I_{CC}	Supply current		$V_{CC} = \text{MAX}, \text{ See Note 2}$		64	103		mA

†For conditions shown as: MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	$C_L = 15 \text{ pF}, R_L = 120 \Omega,$ See Note 3				100	ns
t_{on}	Turn-on time from A input					100	
t_{off}	Turn-off time from RBI input					100	
t_{on}	Turn-on time from RBI input					100	ns

NOTE 3: Load circuit and voltage waveforms are shown on page S-87; t_{off} corresponds to tp_{LH} and t_{on} corresponds to tp_{HL} .

TYPES SN54LS247, SN74LS247

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Peak output current ($t_W \leq 1$ ms, duty cycle $\leq 10\%$)	200 mA
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54LS247	-55°C to 125°C
SN74LS247	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS247			SN74LS247			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			15			15	V
On-state output current, $I_{O(on)}$	a thru g			12			24	mA
High-level output current, I_{OH}	BI/RBO			-50			-50	μA
Low-level output current, I_{OL}	BI/RBO			1.6			3.2	mA
Operating free-air temperature, T_A		-55		125	0		70	$^\circ\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS247			SN74LS247			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_I	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$					-1.5			-1.5	V
V_{OH}	High-level output voltage	BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -50 \mu\text{A}$			2.4	4.2		2.4	4.2		V
V_{OL}	Low-level output voltage	BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 1.6 \text{ mA}$			0.25	0.4		0.25	0.4		V
			$I_{OL} = 3.2 \text{ mA}$						0.35	0.5		
$I_{O(off)}$	Off-state output current	a thru g	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{O(off)} = 15 \text{ V}$					250			250	μA
$V_{O(on)}$	On-state output voltage	a thru g	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{O(on)} = 12 \text{ mA}$			0.25	0.4		0.25	0.4		V
			$I_{O(on)} = 24 \text{ mA}$						0.35	0.5		
I_I	Input current at maximum input voltage		$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$					0.1			0.1	mA
I_{IH}	High-level input current		$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$					20			20	μA
I_{IL}	Low-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$					-0.36			-0.36	mA
		BI/RBO						-1			-1	
I_{OS}	Short-circuit output current	BI/RBO	$V_{CC} = \text{MAX}$			-0.3		-2	-0.3		-2	mA
I_{CC}	Supply current		$V_{CC} = \text{MAX}, \text{ See Note 2}$			7	13		7	13		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input			100	ns
t_{on}	Turn-on time from A input			100	ns
t_{off}	Turn-off time from RBI input			100	ns
t_{on}	Turn-on time from RBI input			100	ns

NOTE 4: Load circuit and voltage waveforms are shown on page S-88. t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL} .

TENTATIVE DATA

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TEXAS INSTRUMENTS
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S-239

TYPES SN54248, SN74248

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

REVISED MARCH 1974

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54248	-55°C to 125°C
SN74248	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminals.

recommended operating conditions

		SN54248			SN74248			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	a thru g			-400			-400	μA
	BI/RBO			-200			-200	
Low-level output current, I_{OL}	a thru g			6.4			6.4	mA
	BI/RBO			8			8	
Operating free-air temperature, T_A		-55		125	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage				0.8		V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5		V
V_{OH}	High-level output voltage	a thru g	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4	4.2		V
		BI/RBO		2.4	3.7		
I_O	Output current	a thru g	$V_{CC} = \text{MIN}, V_O = 0.85 \text{ V},$ Input conditions as for V_{OH}	-1.3	-2		mA
V_{OL}	Low-level output voltage		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = \text{MAX}$	0.27	0.4		V
I_I	Input current at maximum input voltage	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μA
I_{IL}	Low-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
		BI/RBO				-4	
I_{OS}	Short-circuit output current	BI/RBO	$V_{CC} = \text{MAX}$			-4	mA
I_{CC}	Supply current		$V_{CC} = \text{MAX},$ See Note 2		53	90	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input			100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input			100	

NOTE 5: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54LS248, SN74LS248

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS248	-55°C to 125°C
SN74LS248	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS248			SN74LS248			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	a thru g			-100			-100	μ A
	BI/RBO			-50			-50	
Low-level output current, I_{OL}	a thru g			2			6	mA
	BI/RBO			1.6			3.2	
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS248		SN74LS248		UNIT
				MIN	TYP‡	MAX	MIN	
V_{IH}	High-level input voltage			2			2	V
V_{IL}	Low-level input voltage					0.7		0.8 V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.5		-1.5 V
V_{OH}	High-level output voltage	a thru g and BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = \text{MAX}$	2.4	4.2		2.4	4.2 V
I_O	Output current	a thru g	$V_{CC} = \text{MIN}, V_O = 0.85 \text{ V}, \text{Input conditions as for } V_{OH}$	-1.3	-2		-1.3	-2 mA
V_{OL}	Low-level output voltage	a thru g	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 2 \text{ mA}$	0.25	0.4		0.25	0.4 V
			$I_{OL} = 6 \text{ mA}$				0.35	0.5
		BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 1.6 \text{ mA}$	0.25	0.4		0.25	0.4 V
			$I_{OL} = 3.2 \text{ mA}$				0.35	0.5
I_I	Input current at maximum input voltage	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1		0.1 mA
I_{IH}	High-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20		20 μ A
I_{IL}	Low-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.36		-0.36 mA
		BI/RBO				-1		-1
I_{OS}	Short-circuit output current	BI/RBO	$V_{CC} = \text{MAX}$	-0.3		-2	-0.3	-2 mA
I_{CC}	Supply current		$V_{CC} = \text{MAX}, \text{ See Note 2}$	25	38		25	38 mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}, R_L = 4 \text{ k}\Omega,$				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input	See Note 6				100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input	$C_L = 15 \text{ pF}, R_L = 6 \text{ k}\Omega,$				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input	See Note 6				100	

NOTE 6: Load circuit and voltage waveforms are shown on page S-88.

TENTATIVE DATA

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S-241

TYPES SN54249, SN74249
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Table with 2 columns: Parameter and Value. Parameters include Supply voltage (VCC), Input voltage, Current forced into any output, Operating free-air temperature range, and Storage temperature range.

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

Table with 4 columns: Parameter, SN54249 (MIN, NOM, MAX), SN74249 (MIN, NOM, MAX), and UNIT. Parameters include Supply voltage, High-level output voltage, High-level output current, Low-level output current, and Operating free-air temperature.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Table with 5 columns: PARAMETER, TEST CONDITIONS†, MIN, TYP‡, MAX, and UNIT. Parameters include input voltages, input clamp voltage, output voltages, output currents, input current, input currents, input current, short-circuit output current, and supply current.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at VCC = 5 V, TA = 25°C.

NOTE 2: ICC is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, VCC = 5 V, TA = 25°C

Table with 5 columns: PARAMETER, TEST CONDITIONS, MIN, TYP, MAX, and UNIT. Parameters include propagation delay times for high-to-low and low-to-high level outputs.

NOTE 5: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54LS249, SN74LS249

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Current forced into any output in the offstate	1 mA
Operating free-air temperature range: SN54LS249	-55°C to 125°C
SN74LS249	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS249			SN74LS249			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	a thru g			5.5			5.5	V
High-level output current, I_{OH}	BI/RBO			-50			-50	μ A
Low-level output current, I_{OL}	a thru g			4			8	mA
	BI/RBO			1.6			3.2	
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS249			SN74LS249			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_I	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$					-1.5			-1.5	V
V_{OH}	High-level output voltage	BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -50 \mu\text{A}$			2.4	4.2		2.4	4.2		V
I_{OH}	High-level output current	a thru g	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$					250			250	μ A
V_{OL}	Low-level output voltage	BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 1.6 \text{ mA}$			0.25	0.4		0.25	0.4		V
			$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 3.2 \text{ mA}$						0.35	0.5		
		a thru g	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$			0.25	0.4		0.25	0.4		V
			$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 8 \text{ mA}$						0.35	0.5		
I_I	Input current at maximum input voltage	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$					1			1	mA
I_{IH}	High-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$					20			20	μ A
I_{IL}	Low-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$					-0.36			-0.36	mA
		BI/RBO						-1			-1	
I_{OS}	Short-circuit output current	BI/RBO	$V_{CC} = \text{MAX}$			-0.3		-2	-0.3		-2	mA
I_{CC}	Supply current		$V_{CC} = \text{MAX}, \text{ See Note 2}$			8		15	8		15	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input	See Note 6				100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input	$C_L = 15 \text{ pF}, R_L = 6 \text{ k}\Omega,$				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input	See Note 6				100	

NOTE 6: Load circuit and voltage waveforms are shown on page S-88.

TENTATIVE DATA

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TYPES SN54LS257, SN54LS258, SN54S257, SN54S258, SN74LS257, SN74LS258, SN74S257, SN74S258 QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7411734, MARCH 1974

- Three-State Outputs Interface Directly with System Bus
- Schottky-Clamped for Significant Improvement in A-C Performance
- Fully Compatible with Most TTL Functions Including MSI
- Same Pin Assignments as SN54LS157, SN74LS157, SN54S157, SN74S157, and SN54LS158, SN74LS158, SN54S158, SN74S158
- Provides Bus Interface from Multiple Sources in High-Performance Systems

	AVERAGE PROPAGATION DELAY FROM DATA INPUT	TYPICAL POWER DISSIPATION [◇]
--	---	--

'LS257	12 ns	50 mW
'LS258	12 ns	35 mW
'S257	4.8 ns	320 mW
'S258	4 ns	280 mW

[◇]Off state (worst case)

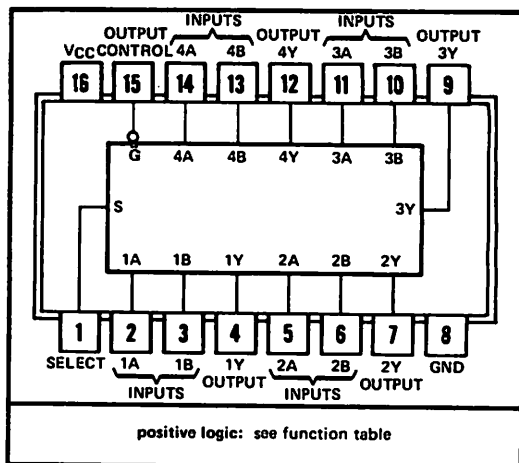
description

These Schottky-clamped high-performance multiplexers feature three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

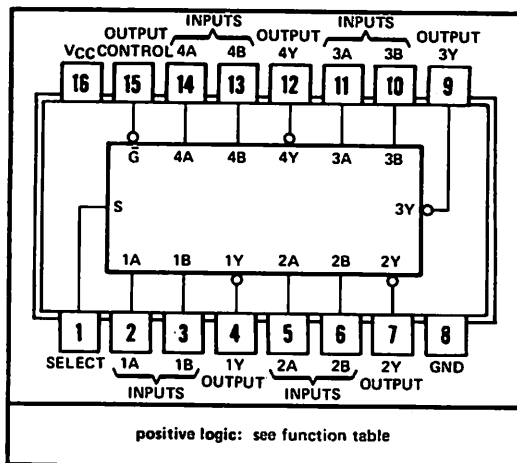
This three-state output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Series 54LS and 54S are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74LS and 74S are characterized for operation from 0°C to 70°C .

SN54LS257, SN54S257 ... J OR W PACKAGE
SN74LS257, SN74S257 ... J OR N PACKAGE
(TOP VIEW)



SN54LS258, SN54S258 ... J OR W PACKAGE
SN74LS258, SN74S258 ... J OR N PACKAGE
(TOP VIEW)



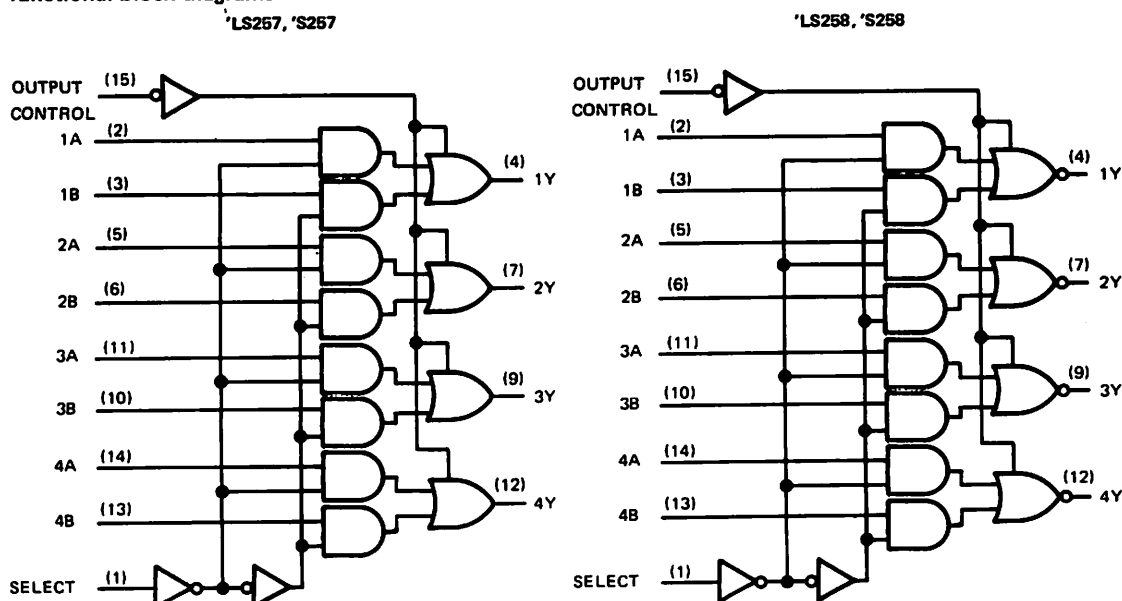
FUNCTION TABLE

OUTPUT CONTROL	SELECT	INPUTS		OUTPUT Y	
		A	B	'LS257 'S257	'LS258 'S258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

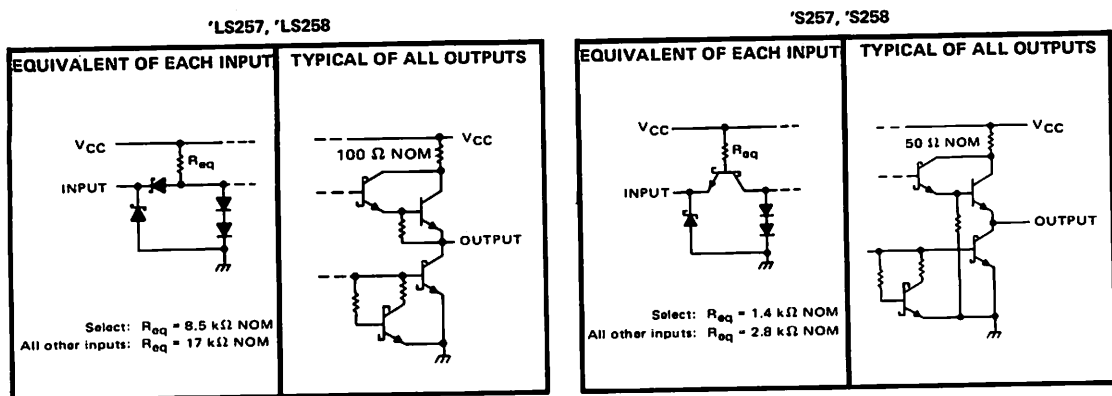
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

TYPES SN54LS257, SN54LS258, SN54S257, SN54S258, SN74LS257, SN74LS258, SN74S257, SN74S258 QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

functional block diagrams



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS257, 'LS258 Circuits	7 V
'S257, 'S258 Circuits	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS', SN54S' Circuits	-55°C to 125°C
SN74LS', SN74S' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54LS257, SN54LS258, SN74LS257, SN74LS258

QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = \text{MAX}$	2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 2.4 \text{ V}$			20			20	µA
I_{OZL}	Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 0.4 \text{ V}$			-20			-20	µA
I_I	Input current at maximum input voltage	S input			0.2			0.2	mA
		Any other			0.1			0.1	
I_{IH}	High-level input current	S input			40			40	µA
		Any other			20			20	
I_{IL}	Low-level input current	S input			-0.8			-0.8	mA
		Any other			-0.4			-0.4	
I_{QS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-6		-40	-5		-42	mA
I_{CC}	Supply current	All outputs high			5.9			5.9	mA
		All outputs low			9.2			9.2	
		All outputs off			10			10	
		All outputs high			4.1			4.1	
		All outputs low			6.2			6.2	
		All outputs off			7.0			7.0	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

NOTE 2: I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}, R_L = 2 \text{ k}\Omega$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS257			'LS258			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
tPLH	Data	Any	C _L = 15 pF, See Note 3	12	18		12	18	ns	
tPHL				12	18		12	18		
tPLH	Select	Any		14	21		14	21	ns	
tPHL				14	21		14	21		
tZH	Output Control	Any		20	30		20	30	ns	
tZL				20	30		20	30		
tHZ	Output Control	Any	C _L = 5 pF, See Note 3	14	21		14	21	ns	
tLZ			14	21		14	21			

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{ZH} = output enable time to high level

NOTE 3: Load circuit and waveforms are shown on page S-88.

t_{ZL} = output enable time to low level

t_{HZ} = output disable time from high level

t_{LZ} = output disable time from low level

TENTATIVE DATA

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TYPES SN54S257, SN54S258, SN74S257, SN74S258

QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54S257, SN54S258			SN74S257, SN74S258			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-2			-6.5	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S257, SN74S257			SN54S258, SN74S258			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage		0.8			0.8			V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.2			-1.2			V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	SN54S [§] 2.4 3.4			2.4 3.4			V
			SN74S [§] 2.4 3.2			2.4 3.2			
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$	0.5			0.5			V
I_{OZH}	Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 2.4 \text{ V}$	50			50			µA
I_{OZL}	Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 0.5 \text{ V}$	-50			-50			µA
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1			1			mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	S input 100			100			µA
			Any other 50			50			
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$	S input -4			-4			mA
			Any other -2			-2			
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	All outputs high 44 68			36 56			mA
			All outputs low 60 93			52 81			
			All outputs off 64 99			56 87			

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

NOTE 2: I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}, R_L = 280 \Omega$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S257, SN74S257		SN54S258, SN74S258		UNIT
				MIN	TYP	MAX	MIN	
tPLH	Data	Any	CL = 15 pF, See Note 4	5	7.5	4	6	ns
tPHL				4.5	6.5	4	6	
tPLH	Select	Any		8.5	15	8	12	ns
tPHL				8.5	15	7.5	12	
tZH	Output Control	Any	13	19.5	13	19.5	ns	
tZL			14	21	14	21		
tHZ	Output Control	Any	CL = 5 pF, See Note 4	5.5	8.5	5.5	8.5	ns
tLZ			9	14	9	14		

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{ZH} = output enable time to high level

NOTE 4: Load circuit and waveforms are shown on page S-87.

t_{ZL} = output enable time to low level

t_{HZ} = output disable time from high level

t_{LZ} = output disable time from low level

TYPES SN54LS261, SN74LS261

2-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS

BULLETIN NO. DL-S 7412123, MARCH 1974

- Fast Multiplication . . . 5-Bit Product in 26 ns Typ
- Power Dissipation . . . 110 mW Typical
- Latch Outputs for Synchronous Operation
- Expandable for m-Bit-by-n-Bit Applications
- Fully Compatible with Most TTL and Other Saturated Low-Level Logic Families
- Diode-Clamped Inputs Simplify System Design

description

These low-power Schottky circuits are designed to be used in parallel multiplication applications. They perform binary multiplication in two's-complement form, two bits at a time.

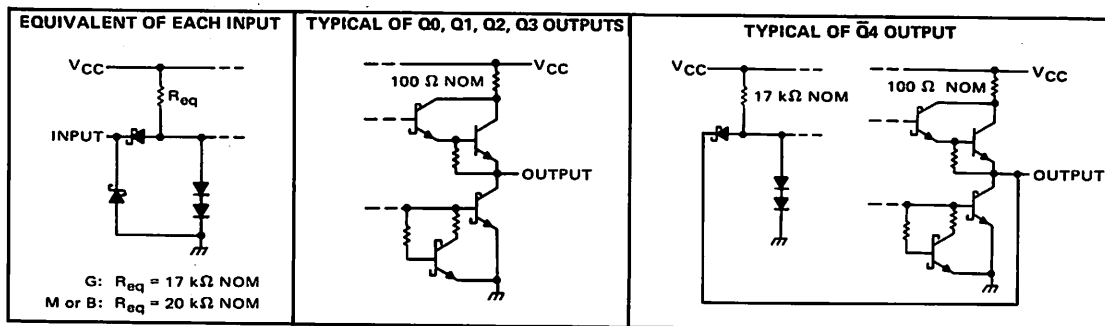
The M inputs are for the multiplier bits and the B inputs are for the multiplicand. The Q outputs represent the partial product as a recoded base-4 number. This recoding effectively reduces the Wallace-tree hardware requirements by a factor of two.

The outputs represent partial products in one's-complement form generated as a result of multiplication. A simple rounding scheme using two additional gates is needed for each partial product to generate two's complement.

The leading (most-significant) bit of the product is inverted for ease in extending the sign to square (left justify) the partial-product bits.

The SN54LS261 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74LS261 for operation from 0°C to 70°C .

schematics of inputs and outputs



TENTATIVE DATA SHEET

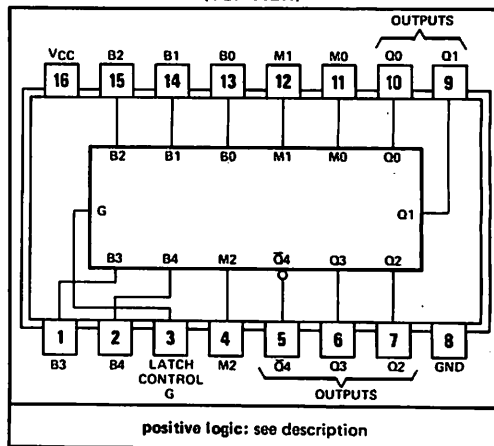
S-248

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SN54LS261 . . . J OR W PACKAGE
SN74LS261 . . . J OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

LATCH CONTROL G	INPUTS			OUTPUTS				
	MULTIPLIER			\bar{Q}_4	Q3	Q2	Q1	Q0
	M2	M1	M0	\bar{Q}_4	Q3	Q2	Q1	Q0
L	X	X	X	\bar{Q}_4	Q3	Q2	Q1	Q0
H	L	L	L	H	L	L	L	L
H	L	L	H	\bar{B}_4	B4	B3	B2	B1
H	L	H	L	\bar{B}_4	B4	B3	B2	B1
H	L	H	H	\bar{B}_4	B3	B2	B1	B0
H	H	L	L	B4	\bar{B}_3	\bar{B}_2	\bar{B}_1	\bar{B}_0
H	H	L	H	B4	\bar{B}_4	\bar{B}_3	\bar{B}_2	\bar{B}_1
H	H	H	L	B4	\bar{B}_4	\bar{B}_3	\bar{B}_2	\bar{B}_1
H	H	H	H	H	L	L	L	L

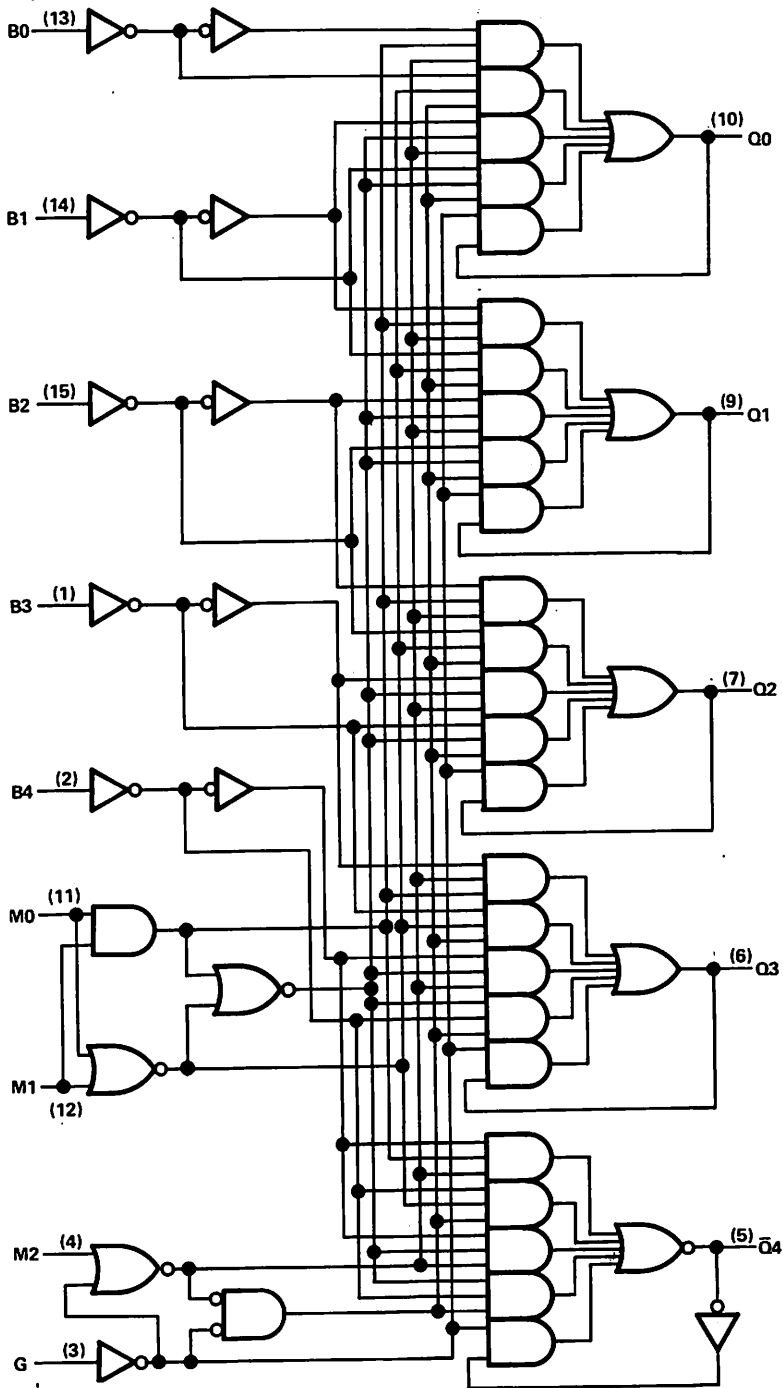
H = high level, L = low level, X = irrelevant

$\bar{Q}_4 \dots Q_0$ = The logic level of the same output before the high-to-low transition of G.

$B_4 \dots B_0$ = The logic level of the indicated multiplicand (B) input.

TYPES SN54LS261, SN74LS261 2-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS

functional block diagram



TYPES SN54LS261, SN74LS261

2-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS261	-55°C to 125°C
SN74LS261	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS261			SN74LS261			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-1			-1	mA
Low-level output current, I_{OL}				4			8	mA
Width of enable pulse, t_W		25			25			ns
Setup time, t_{setup}	Any M input	17↓			17↓			ns
	Any B input	15↓			15↓			
Hold time, t_{hold}	Any M input	0↓			0↓			ns
	Any B input	0↓			0↓			
Operating free-air temperature, T_A		-55		125	0		70	°C

↓The arrow indicates that the falling edge of the enable pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS261			SN74LS261			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IH} High-level input voltage		2			2			V	
V _{IL} Low-level input voltage				0.7			0.8	V	
V _I Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V	
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V	
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 4 mA		0.25	0.4	0.25		0.4	V
		I _{OL} = 8 mA				0.35		0.5	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA	
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.7 V			20			20	μA	
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA	
I _{OS} Short-circuit output current§	V _{CC} = MAX	-6		-40	-5		-42	mA	
I _{CC} Supply current	V _{CC} = MAX, All inputs at 0 V Outputs open	22	38		22	40		mA	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	Enable G	Any Q	CL = 15 pF, RL = 2 kΩ, See Note 2	22	35		ns
tPHL				20	30		ns
tPLH	Any M input	Any Q		25	40		ns
tPHL				22	35		ns
tPLH	Any B input	Any Q		27	42		ns
tPHL				24	37		ns

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output.

t_{PHL} ≡ propagation delay time, high-to-low-level output.

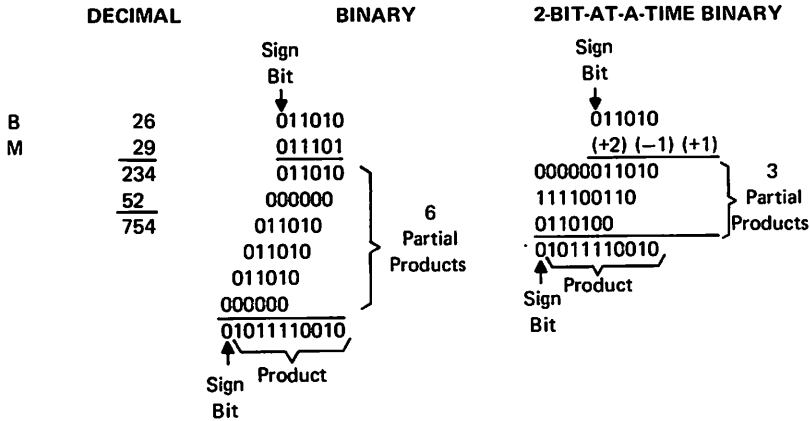
NOTE 2: Load circuit and voltage waveforms are shown on page S-88.

TYPES SN54LS261, SN74LS261

2-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS

TYPICAL APPLICATION DATA

Multiplication of the numbers 26 (multiplicand) by 29 (multiplier) in decimal, binary, and 2-bit-at-a-time-binary is shown here:

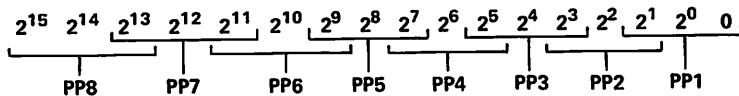


Two points should be noted in the two-bit-at-a-time-binary example above. First, in positioning the partial products beneath each other for final addition, each partial product is shifted two places to the left of the partial products above it instead of one place as is done in regular multiplication. Second, the msb of the partial product (the sign bit) is extended to the sign-bit column of the final answer.

A substantial reduction of multiplication time, cost, and power is obtained by implementing a parallel partial-product-generation scheme using a 2-bit-at-a-time algorithm, followed by a Wallace Tree summation.

Partial-product-generation rules of the algorithm are:

1. Examine two bits of multiplier M plus the next lower bit. For the first partial product (PP1) the next lower bit is zero.



TYPES SN54LS261, SN74LS261

2-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS

TYPICAL APPLICATION DATA

2. Generate partial product (PPI) as shown in the following table:

MULTIPLIER BITS FROM STEP 1			OPERATOR SYMBOL	TO OBTAIN PARTIAL PRODUCT
2 ²ⁱ⁻¹	2 ²ⁱ⁻²	2 ²ⁱ⁻³		
0	0	0	0	Replace multiplicand by zero
0	0	1	+1 B	Copy multiplicand
0	1	0	+1 B	Copy multiplicand
0	1	1	+2 B	Shift multiplicand left one bit
1	0	0	-2 B	Shift two's complement of multiplicand left one bit
1	0	1	-1 B	Replace multiplicand by two's complement
1	1	0	-1 B	Replace multiplicand by two's complement
1	1	1	0	Replace multiplicand by zero

- Weight the partial products by indexing each two places left relative to the next-less-significant product.
- Extend the most-significant bit of the partial product to the sign-bit place value of the final product.

EXAMPLE OF ALGORITHM

M = 29 = 011101	Operator Symbol	B = 26 = 011010
<pre> 011101 010 110 011 </pre>	+1 B 00000011010 -1B 111100110 +2 B 0110100	

The summation of these partial products was shown in the 2-bit-at-a-time binary multiplication example above.

The 'LS261 generates partial products according to this algorithm with two exceptions:

- The one's complement is generated for the cases requiring the two's complement. The two's complement can be obtained by adding one to the one's complement; this rounding can be done by using one NAND gate and one AND gate as shown in Figure B.
- The most-significant bit is complemented to reduce the hardware required to extend the sign bit. This extension can be accomplished by adding a hard-wired logic 1 in bit position 2²ⁱ⁺¹⁵ of each partial product and also in bit position 2¹⁶ of the first partial product (PP1).

TYPES SN54LS261, SN74LS261 **2-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS**

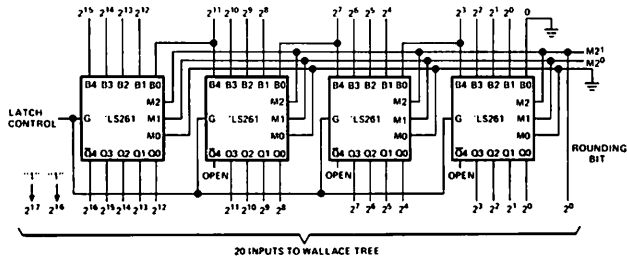


FIGURE A—FIRST PARTIAL PRODUCT, PP1

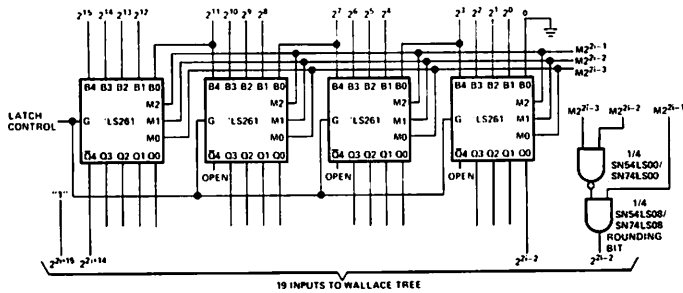


FIGURE B—OTHER PARTIAL PRODUCTS, PPi

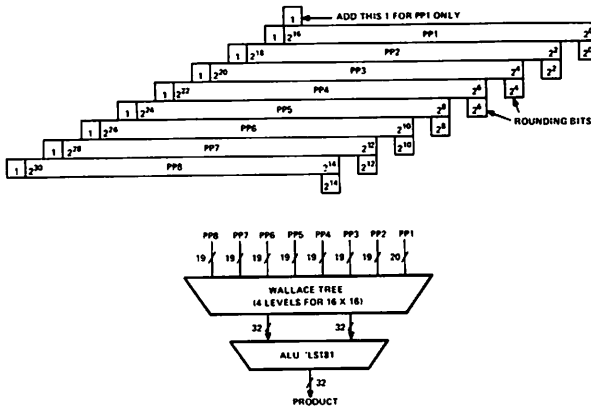


FIGURE C—MANIPULATION OF PARTIAL PRODUCTS FOR ENTRY INTO WALLACE TREE

In general, the 4 x 2 bit 'LS261 can be expanded for use in 4m x 2n bit multipliers. Partial-product generation uses m x n 'LS261s, m x n ÷ 16 'LS00s, and m x n ÷ 16 'LS08s. The size of the Wallace tree and ALU requirements vary depending on the size of the problem. The count for the 16 x 16 bit multiplier is:

32	SN54LS261/SN74LS261
2	SN54LS00/SN74LS00
2	SN54LS08/SN74LS08
56	SN54H183/SN74H183
7	SN54LS181/SN74LS181
2	SN54LS182/SN74LS182

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**TTL
LSI**

TYPES SN54S270, SN74S270, SN74S271 2048-BIT READ-ONLY MEMORIES WITH OPEN-COLLECTOR OUTPUTS

BULLETIN NO. DL-S 7412080, MARCH 1974

- Full Schottky Clamping for High Performance:
Address Access Time . . . 45 ns Typical
Chip-Select Time . . . 15 ns Typical
Power Dissipation . . . 0.25 mW/Bit Typical
- 'S270 Is Organized as 512 Words by 4 Bits
- 'S271 Is Organized as 256 Words by 8 Bits and Is in a 20-Pin Package for 0.300-Inch Row Spacing
- Ideal for Microprogramming, Reference Tables, and High-Speed Code Converters
- Open-Collector Outputs Permit Expansion
- SN54S370, SN74S370 and SN74S371 Are Functionally Equivalent But Have 3-State Outputs.

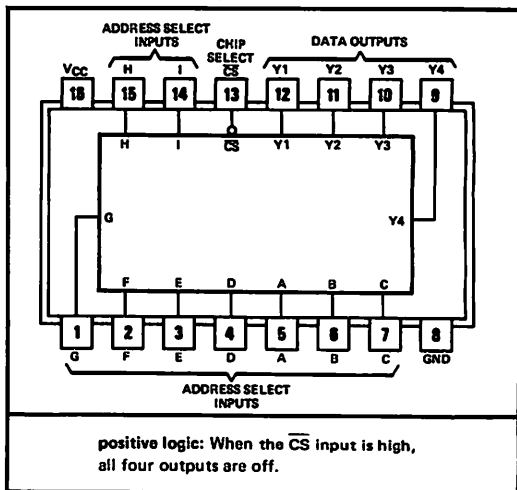
description

The SN54S270, SN74S270, and SN74S271 are 2048-bit monolithic custom-programmed read-only memories. The 'S270 is organized as 512 words of four bits each and the 'S271 is organized as 256 words of eight bits each. These Schottky-clamped, high-speed transistor-transistor-logic (TTL) memory arrays are addressed in straight binary with full on-chip decoding. Overriding chip-select inputs are provided which, when one or more is taken high, will inhibit the function causing all outputs to remain high. Data, as specified by the customer, are permanently programmed into the monolithic structure for the 2048 bit locations.

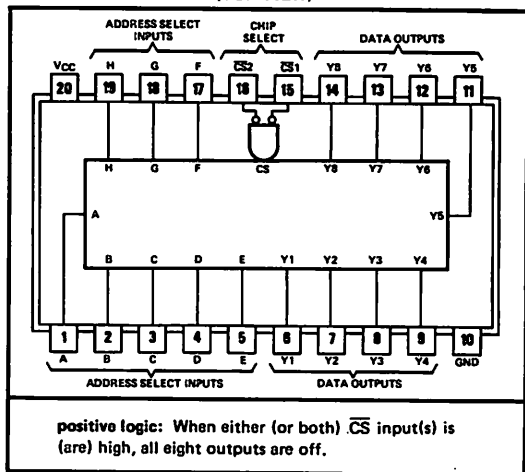
The memory matrix consists of 32 transistors comprising the X plane with each transistor having 64 emitters. Each of the 64 bit lines that comprise the Y plane of the matrix is connected to one emitter from each of the 32 transistors. The address of a word is accomplished through the buffered binary select inputs coincident with low-level voltages at all chip-select inputs. Five binary select inputs are decoded internally in the X plane to select one of the 32 matrix transistors. In the 'S270 the four remaining select inputs are internally decoded in the Y plane to select four of the 64 bit lines. These selected bit lines appear as a four-bit word output. In the 'S271 the three remaining select inputs are internally decoded in the Y plane to select eight of the 64 bit lines. These selected bit lines appear as an eight-bit word output.

The customer can specify the output logic level desired at each of the 2048 bit locations by completing the supplementary ordering data and a set of data cards punched in accordance with the data format shown under ordering instructions. Upon receipt of the order, Texas Instruments will assign a special device number to the device programmed according to the customer's order. The completed device will be marked with the TI special device number. It is important that the customer specify not only the output levels desired at all 2048 bit locations, but also the other information requested.

SN54S270 . . . J PACKAGE
SN74S270 . . . J OR N PACKAGE
(TOP VIEW)



SN74S271 . . . N PACKAGE
(TOP VIEW)



TENTATIVE DATA SHEET

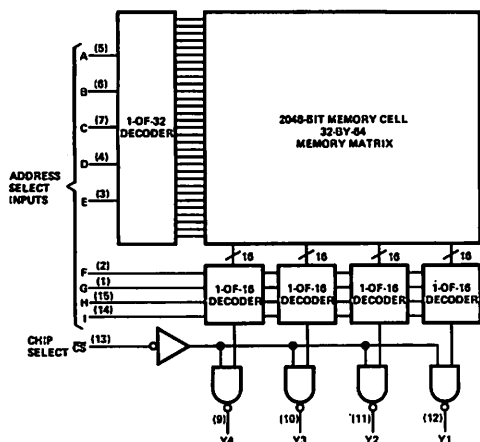
S-254

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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TYPES SN54S270, SN74S270, SN74S271 2048-BIT READ-ONLY MEMORIES WITH OPEN-COLLECTOR OUTPUTS

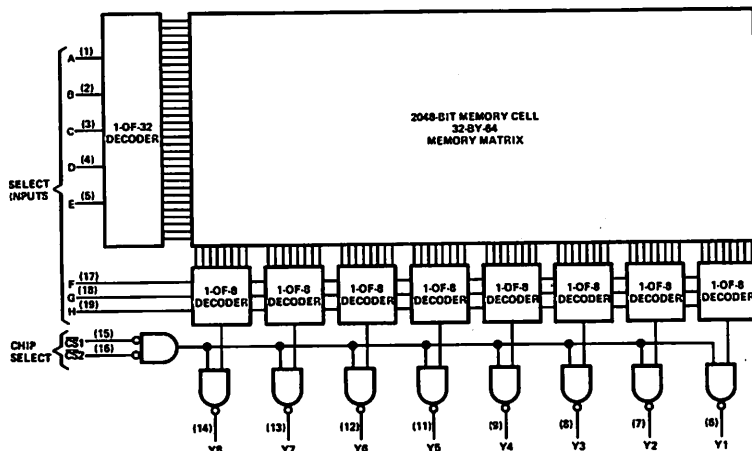
SN54S270/SN74S270 functional block diagram and word selection



WORD-SELECT TABLE									
WORD	INPUTS								
	I	H	G	F	E	D	C	B	A
0	L	L	L	L	L	L	L	L	L
1	L	L	L	L	L	L	L	L	H
2	L	L	L	L	L	L	L	H	L
3	L	L	L	L	L	L	L	H	H
4	L	L	L	L	L	L	H	L	L
5	L	L	L	L	L	L	H	H	L
6	L	L	L	L	L	L	H	H	L
7	L	L	L	L	L	L	H	H	H
8	L	L	L	L	L	H	L	L	L
Words 9 thru 506 omitted									
507	H	H	H	H	H	H	L	H	H
508	H	H	H	H	H	H	H	L	L
509	H	H	H	H	H	H	H	L	H
510	H	H	H	H	H	H	H	L	L
511	H	H	H	H	H	H	H	H	H

Word selection is accomplished in a conventional 9-bit positive-logic binary code with the A select input being the least-significant bit progressing alphabetically through the select inputs to I which is the most-significant bit.

SN74S271 functional block diagram and word selection



WORD-SELECT TABLE									
WORD	INPUTS								
	H	G	F	E	D	C	B	A	
0	L	L	L	L	L	L	L	L	
1	L	L	L	L	L	L	L	H	
2	L	L	L	L	L	L	H	L	
3	L	L	L	L	L	L	H	H	
4	L	L	L	L	L	H	L	L	
5	L	L	L	L	L	H	L	H	
6	L	L	L	L	L	H	H	L	
7	L	L	L	L	L	H	H	H	
8	L	L	L	L	H	L	L	L	
Words 9 thru 250 omitted									
251	H	H	H	H	H	L	H	H	
252	H	H	H	H	H	H	L	L	
253	H	H	H	H	H	H	L	H	
254	H	H	H	H	H	H	L	L	
255	H	H	H	H	H	H	H	H	

Word selection is accomplished in a conventional 8-bit positive-logic binary code with the A select input being the least-significant bit progressing alphabetically through the select inputs to H which is the most-significant bit.

TYPES SN54S270, SN74S270, SN74S271
2048-BIT READ-ONLY MEMORIES WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Table with 2 columns: Parameter and Value. Parameters include Supply voltage (VCC), Input voltage, Off-state output voltage, Operating free-air temperature range, and Storage temperature range.

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

Table with 5 columns: Parameter, SN54S270 (MIN, NOM, MAX), SN74S270/SN74S271 (MIN, NOM, MAX), and UNIT. Parameters include Supply voltage, High-level output voltage, Low-level output current, and Operating free-air temperature.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Table with 5 columns: PARAMETER, TEST CONDITIONS, SN54S270 (MIN, TYP, MAX), SN74S270/SN74S271 (MIN, TYP, MAX), and UNIT. Parameters include input/output voltages, currents, and capacitance.

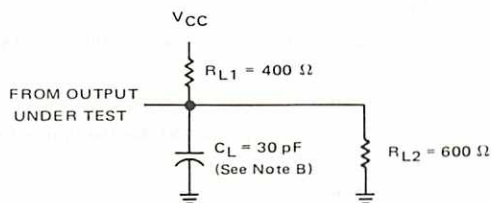
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at VCC = 5 V, TA = 25°C.
NOTE 2: With outputs open and CS input(s) grounded, ICC is measured first by selecting a word that contains the maximum number of programmed high-level outputs; then by selecting a word that contains the maximum number of programmed low-level outputs.

switching characteristics, VCC = 5 V, TA = 25°C

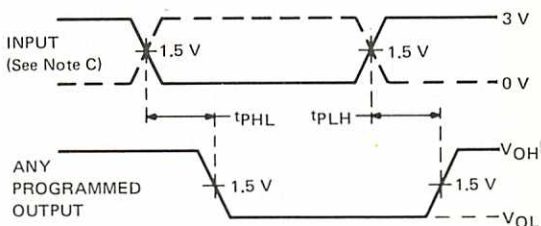
Table with 5 columns: PARAMETER, TEST CONDITIONS, MIN, TYP, MAX, and UNIT. Parameters include propagation delay times for different output transitions.

TYPES SN54S270, SN74S270, SN74S271 2048-BIT READ-ONLY MEMORIES WITH OPEN-COLLECTOR OUTPUTS

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

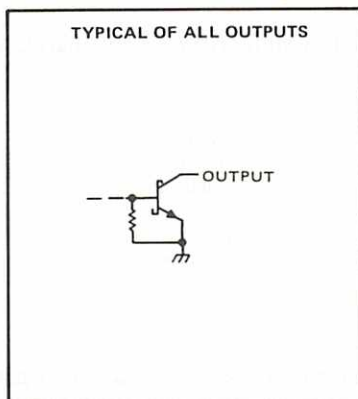
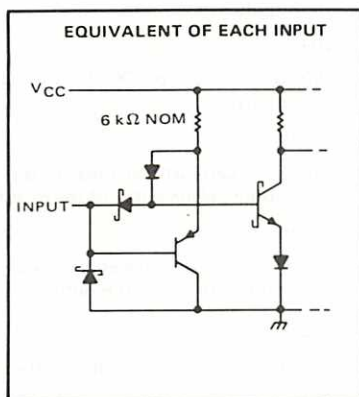


VOLTAGE WAVEFORMS

- NOTES: A. The input pulse generator has the following characteristics: $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$, $PRR \leq 1 \text{ MHz}$, $Z_{out} \approx 50 \Omega$.
B. C_L includes probe and jig capacitance.
C. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.

FIGURE 1—PROPAGATION DELAY TIMES

schematics of inputs and outputs



TYPES SN54S270, SN74S270, SN74S271

2048-BIT READ-ONLY MEMORIES WITH OPEN-COLLECTOR OUTPUTS

ORDERING INSTRUCTIONS

Programming instructions for these read-only memories are solicited in the form of a sequenced deck of 64 standard 80-column data cards providing the information requested under "data card format," accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete function table for the requested part. This function table, showing output conditions for each of the words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the function table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the words specified and describes the levels at the outputs. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

SUPPLEMENTARY ORDERING DATA

Submit the following information with the data cards:

- Customer's name and address
- Customer's purchase order number
- Customer's drawing number.

The following information will be furnished to the customer by Texas Instruments:

- TI part number
- TI sales order number
- Date received.

'S270 DATA CARD FORMAT (64 CARDS)

Column

- 1-3 Punch a right-justified integer representing the binary input address (000-504) for the first set of outputs described on the card.
- 4 Punch a "-" (Minus sign)
- 5-7 Punch a right-justified integer representing the binary input address (007-511) for the last set of outputs described on the card.
- 8-9 Blank
- 10-13 Punch "H", "L", or "X" for bits four, three, two, and one (outputs Y4, Y3, Y2, and Y1 in that order) for the first set of

outputs specified on the card. H = high-voltage-level output, L = low-voltage-level output, X = output level irrelevant.

- 14 Blank
- 15-18 Punch "H", "L", or "X" for the second set of outputs.
- 19 Blank
- 20-23 Punch "H", "L", or "X" for the third set of outputs.
- 24 Blank
- 25-28 Punch "H", "L", or "X" for the fourth set of outputs.
- 29 Blank
- 30-33 Punch "H", "L", or "X" for the fifth set of outputs.
- 34 Blank
- 35-38 Punch "H", "L", or "X" for the sixth set of outputs.
- 39 Blank
- 40-43 Punch "H", "L", or "X" for the seventh set of outputs.
- 44 Blank
- 45-48 Punch "H", "L", or "X" for the eighth set of outputs.
- 49 Blank
- 50-51 Punch a right-justified integer representing the current calendar day of the month.
- 52 Blank
- 53-55 Punch an alphabetic abbreviation representing the current month.
- 56 Blank
- 57-58 Punch the last two digits of the current year.
- 59 Blank
- 60-61 Punch "SN"
- 62-66 Punch a left-justified integer representing the Texas Instruments part number. This is supplied by the factory through a TI sales representative.
- 67-68 Blank
- 69-80 Preferably these columns should be punched to reflect the customer's part or specification-control number. This information is not essential.

TYPES SN54S270, SN74S270, SN74S271 2048-BIT READ-ONLY MEMORIES WITH OPEN-COLLECTOR OUTPUTS

SN74S271 DATA CARD FORMAT (64 CARDS)

Column

- | | | | |
|-------|---|-------|---|
| 1- 3 | Punch a right-justified integer representing the binary input address (000-252) for the first set of outputs described on the card. | 37-44 | Punch "H", "L", or "X" for the fourth set of outputs. |
| 4 | Punch a "-" (Minus sign) | 45-49 | Blank |
| 5- 7 | Punch a right-justified integer representing the binary input address (003-255) for the last set of outputs described on the card. | 50-51 | Punch a right-justified integer representing the current calendar day of the month. |
| 8- 9 | Blank | 52 | Blank |
| 10-17 | Punch "H", "L", or "X" for bits eight, seven, six, five, four, three, two, and one (outputs Y8, Y7, Y6, Y5, Y4, Y3, Y2, and Y1 in that order) for the first set of outputs specified on the card. H = high-voltage-level output, L = low-voltage-level output, X = output level irrelevant. | 53-55 | Punch an alphabetic abbreviation representing the current month. |
| 18 | Blank | 56 | Blank |
| 19-26 | Punch "H", "L", or "X" for the second set of outputs. | 57-58 | Punch the last two digits of the current year. |
| 27 | Blank | 59 | Blank |
| 28-35 | Punch "H", "L", or "X" for the third set of outputs. | 60-61 | Punch "SN" |
| 36 | Blank | 62-66 | Punch a left-justified integer representing the Texas Instruments part number. This is supplied by the factory through a TI sales representative. |
| | | 67-68 | Blank |
| | | 69-80 | Preferably these columns should be punched to reflect the customer's part or specification-control number. This information is not essential. |

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**TTL
MSI**

TYPE SN74273 **OCTAL D-TYPE FLIP-FLOP WITH CLEAR**

BULLETIN NO. DL-S 7412091, MARCH 1974

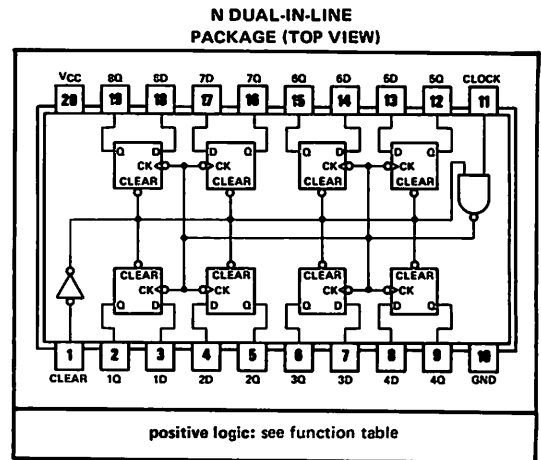
- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
Buffer/Storage Registers
Shift Registers
Pattern Generators

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 25 MHz while maximum clock frequency is typically 35 megahertz. Typical power dissipation is 39 milliwatts per flip-flop.



**FUNCTION TABLE
(EACH FLIP-FLOP)**

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

H = high level (steady state)

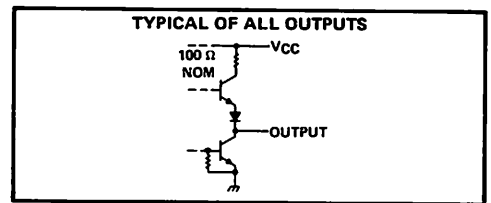
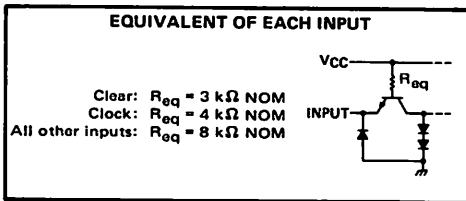
L = low level (steady state)

X = irrelevant

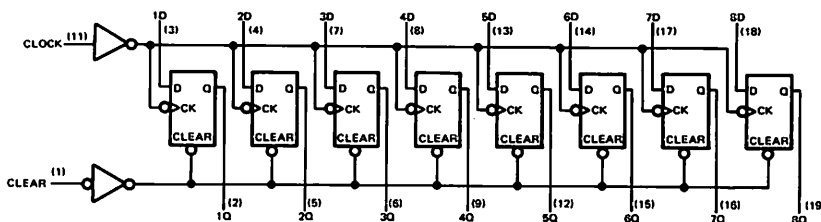
↑ = transition from low to high level

Q₀ = the level of Q before the indicated steady-state input conditions were established.

schematics of inputs and output



functional block diagram



TENTATIVE DATA SHEET

S-260

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TYPE SN74273

OCTAL D-TYPE FLIP-FLOP WITH CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			-800	μ A
Low-level output current, I_{OL}			16	mA
Clock frequency, f_{clock}	0		25	MHz
Width of clock or clear pulse, t_w	20			ns
Setup time, t_{setup}	Data input	20†		ns
	Clear inactive state	25†		ns
Data hold time, t_{hold}	5†			ns
Operating free-air temperature, T_A	0		70	°C

†The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$			0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	Clear			80	μ A
	Clock or D			40	
I_{IL} Low-level input current	Clear			-3.2	mA
	Clock or D			-1.6	
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-18		-57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		62	94	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 400 \Omega, \text{ See Note 3}$	25	35		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			20	30	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			21	30	ns

NOTE 3: Load circuit and voltage waveforms are shown on page S-87.

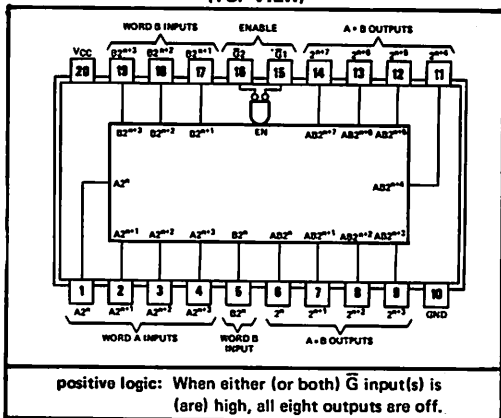
TTL
LSI

TYPES SN54S275, SN74S274, SN74S275 4-BIT-BY-4-BIT BINARY MULTIPLIER WITH 3-STATE OUTPUTS 7-BIT-SLICE WALLACE TREES WITH 3-STATE OUTPUTS

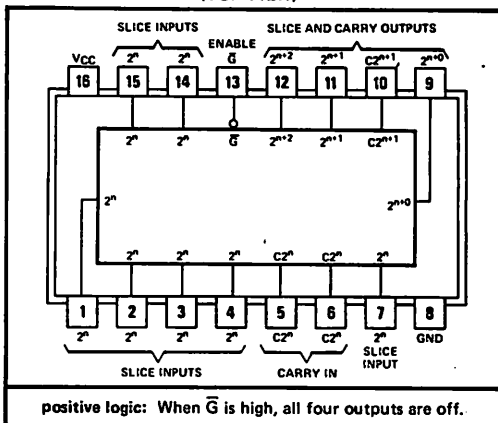
BULLETIN NO. DL-S 7412121, MARCH 1974

SN74S274 . . . N PACKAGE
(TOP VIEW)

- 'S274 Provides 8-Bit Product in Typically 45 ns
- 'S274 Can Provide Sub-Multiple Products for n-Bit-by-n-Bit Binary Numbers
- 'S275 Accepts 7 Bit-Slice Inputs and 2 Carry Inputs for Reduction to 4 Lines in Typically 45 ns
- These New High-Complexity Functions Can Reduce Package Count by Nearly 50% in Most Parallel Multiplier Designs
- When Combined With SN74H183 and Schottky Look-Ahead Adders, Multiplication Times Are Typically:
 - 16-Bit Product in 75 ns
 - 32-Bit Product in 116 ns



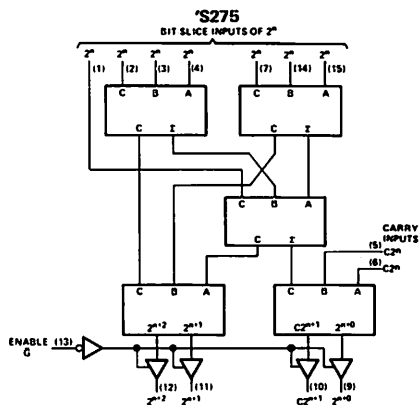
SN54S275 . . . J PACKAGE
SN74S275 . . . J OR N PACKAGE
(TOP VIEW)



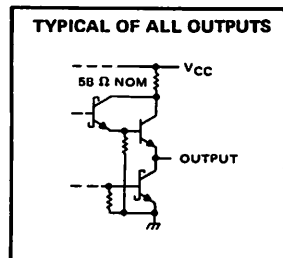
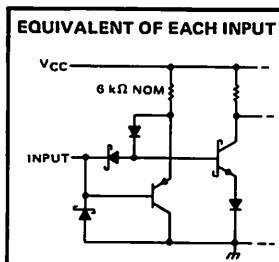
description

These high-complexity Schottky-clamped TTL circuits are designed specifically to reduce the delay time required to perform high-speed parallel binary multiplication and significantly reduce package count. The 'S274 is a basic 4-bit-by-4-bit parallel multiplier in a single package, and as such, no additional components are required to obtain an 8-bit product. The 'S275 expandable bit-slice Wallace tree has been designed to accept up to seven bit-slice inputs and two carry inputs from previous slices for reduction to four lines. For word lengths longer than 4 bits, a number of 'S274 multipliers can be combined to generate sub-multiple partial products. These partial products can then be combined in Wallace trees to obtain the final product. See Typical Application Data.

functional block diagram



schematics of inputs and outputs



NOTE: When one of the C_2^n carry inputs is not used, it must be grounded. If neither C_2^n carry input is used, both C_2^n inputs are grounded and the C_2^{n+1} output is normally left open.

TENTATIVE DATA SHEET

S-262

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TYPES SN54S275, SN74S274, SN74S275

4-BIT-BY-4-BIT BINARY MULTIPLIER WITH 3-STATE OUTPUTS

7-BIT-SLICE WALLACE TREES WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54S275	-55°C to 125°C
SN74S274, SN74S275	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S275			SN74S274 SN74S275			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-2			-6.5	mA
Low-level output current, I_{OL}			12			12	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S275			SN74S274 SN74S275			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = \text{MAX}$	2.4	3.4		2.4	3.2		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 12 \text{ mA}$			0.5			0.5	V
I_{OZH} Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_O = 2.4 \text{ V}$			50			50	μA
I_{OZL} Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_O = 0.5 \text{ V}$			-50			-50	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			25			25	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.5 \text{ V}$			-0.25			-0.25	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-30		-100	-30		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$		105	155		105	155	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

TYPES SN54S275, SN74S274, SN74S275

4-BIT-BY-4-BIT BINARY MULTIPLIER WITH 3-STATE OUTPUTS

7-BIT-SLICE WALLACE TREES WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B ('S274), or Any Slice or Carry ('S275)	Any	$C_L = 30\text{ pF}$, $R_L = 400\ \Omega$, See Figure 1		45		ns
t_{PHL}					45		
t_{ZH}	Any Enable	Any	$C_L = 5\text{ pF}$, $R_L = 400\ \Omega$, See Figure 1		15		ns
t_{ZL}					15		
t_{HZ}					10		ns
t_{LZ}					10		

[†] t_{PLH} \equiv Propagation delay time, low-to-high-level output
 t_{PHL} \equiv Propagation delay time, high-to-low-level output
 t_{ZH} \equiv Output enable time to high level
 t_{ZL} \equiv Output enable time to low level
 t_{HZ} \equiv Output disable time from high level
 t_{LZ} \equiv Output disable time from low level

PARAMETER MEASUREMENT INFORMATION

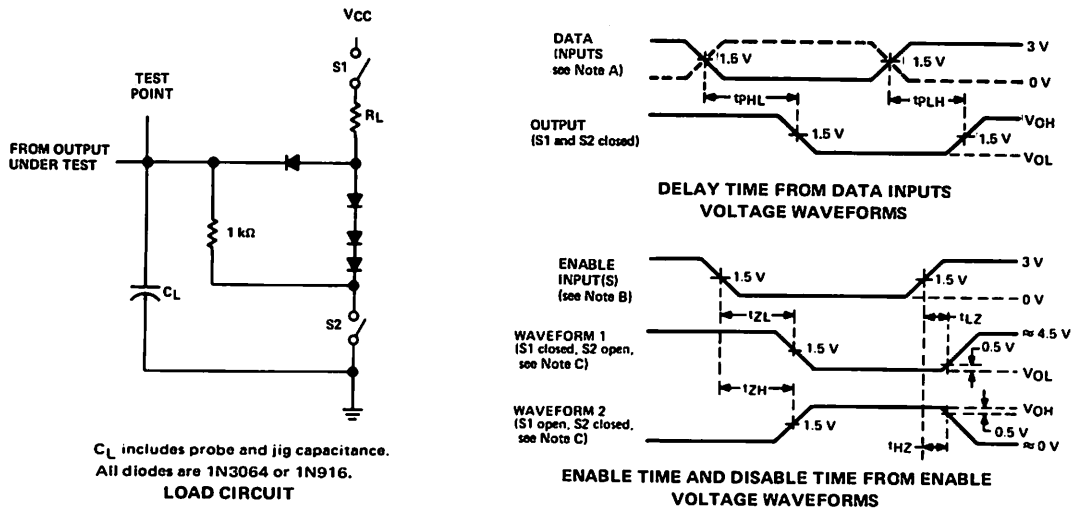


FIGURE 1—SWITCHING TIMES

NOTES: A. When measuring delay times from data inputs, the enable input(s) are low.
 B. When measuring delay times from enable input(s), the data inputs are steady-state.
 C. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
 D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r < 2.5\text{ ns}$, $t_f < 2.5\text{ ns}$, $PRR < 1\text{ MHz}$, and $Z_{out} \approx 50\ \Omega$.

TYPES SN54S275, SN74S274, SN74S275 **4-BIT-BY-4-BIT BINARY MULTIPLIER WITH 3-STATE OUTPUTS** **7-BIT-SLICE WALLACE TREES WITH 3-STATE OUTPUTS**

TYPICAL APPLICATION DATA

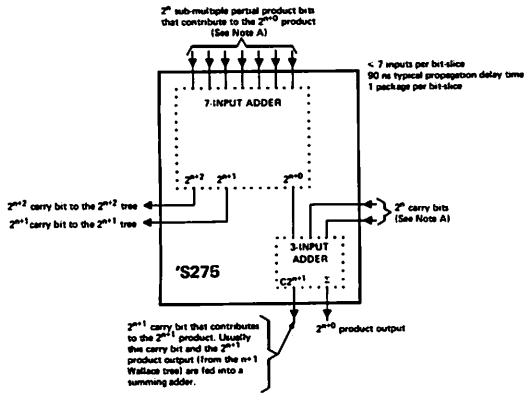


FIGURE 2—BASIC BIT-SLICE WALLACE TREE

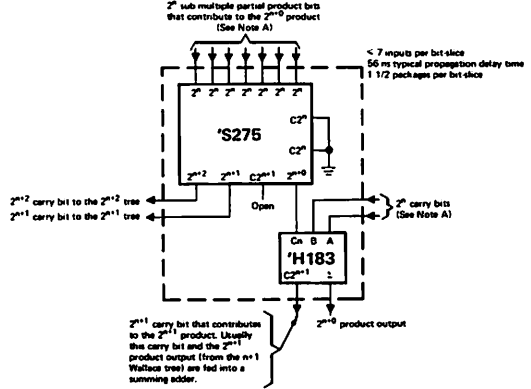


FIGURE 3—HIGH-SPEED BIT-SLICE WALLACE TREE

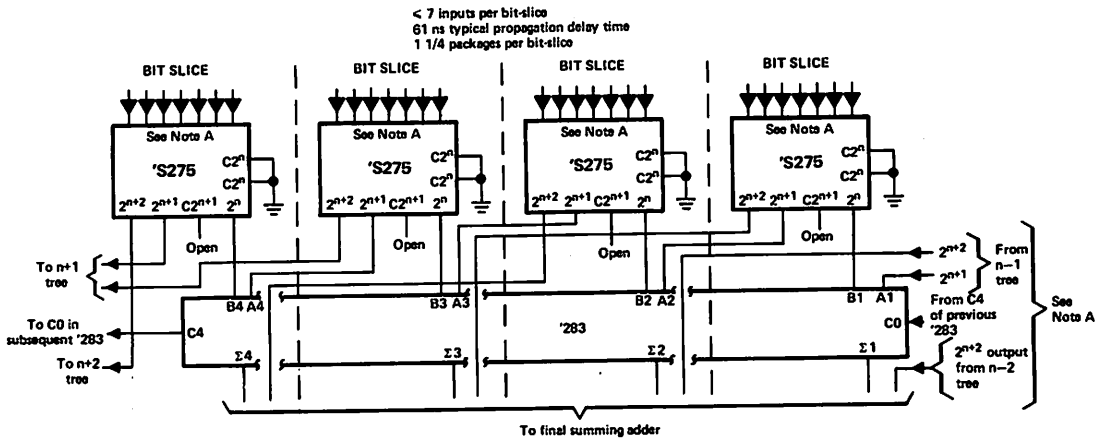


FIGURE 4—MODERATE-SPEED BIT-SLICE WALLACE TREE

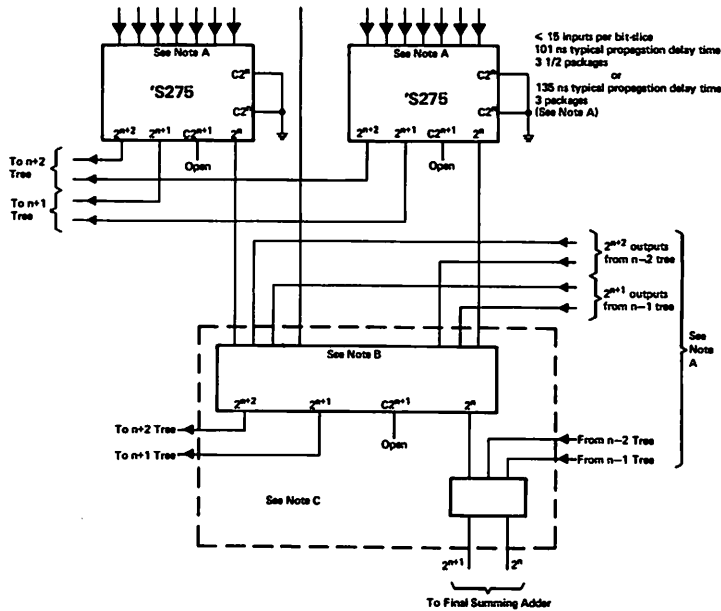
NOTE A: All unused inputs must be grounded.

TYPES SN54S275, SN74S274, SN74S275

4-BIT-BY-4-BIT BINARY MULTIPLIER WITH 3-STATE OUTPUTS

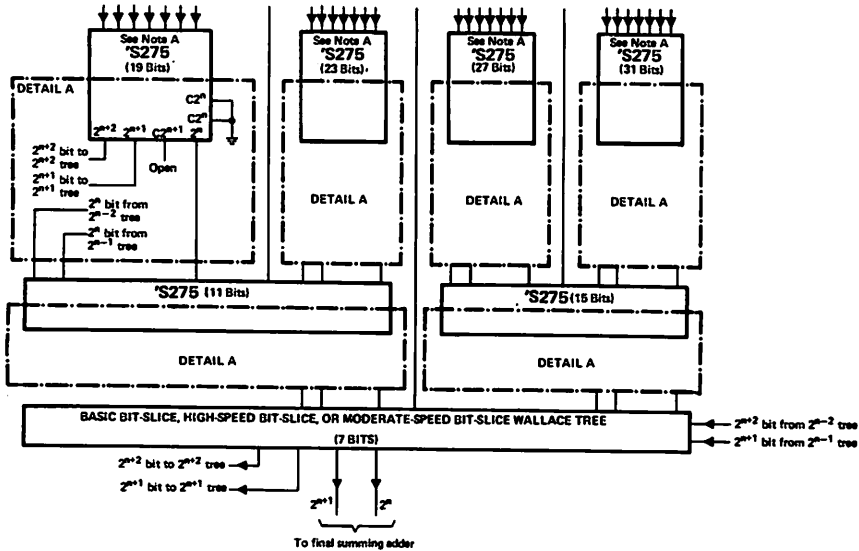
7-BIT-SLICE WALLACE TREES WITH 3-STATE OUTPUTS

TYPICAL APPLICATION DATA



- NOTES:
- A. Ground unused inputs.
 - B. These outputs from preceding trees may go to any of the inputs of the 'S275.
 - C. The circuit within the dotted lines may be either the basic bit-slice Wallace tree or the high-speed Wallace tree. In the latter case both carry inputs of the '275 must be grounded.

FIGURE 5—15-BIT-SLICE WALLACE TREE FOR 32-BIT X 32-BIT MULTIPLIER



- NOTES:
- A. Ground unused inputs.
 - B. The number of bits in parentheses is the maximum number of bits this tree can combine if the remaining 'S275's (all having a higher number in the parentheses) were not connected.

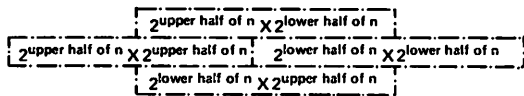
FIGURE 6—7-TO-31-BIT-SLICE WALLACE TREE FOR UP TO 64-BIT X 64-BIT MULTIPLIERS

TYPES SN54S275, SN74S274, SN74S275

4-BIT-BY-4-BIT BINARY MULTIPLIER WITH 3-STATE OUTPUTS

7-BIT-SLICE WALLACE TREES WITH 3-STATE OUTPUTS

TYPICAL APPLICATION DATA



NOTE A: The left-hand half of each rectangle is the portion of word one used to obtain the product shown within the rectangle. Similarly, the right-hand half of each rectangle is the portion of word two used.

FIGURE 7—UNIVERSAL METHOD OF ADDING $\frac{n}{2}$ -BIT PRODUCTS TO OBTAIN AN n -BIT PRODUCT

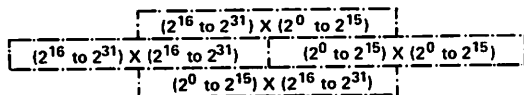


FIGURE 8—METHOD OF ADDING 32-BIT PRODUCTS TO OBTAIN A 64-BIT PRODUCT

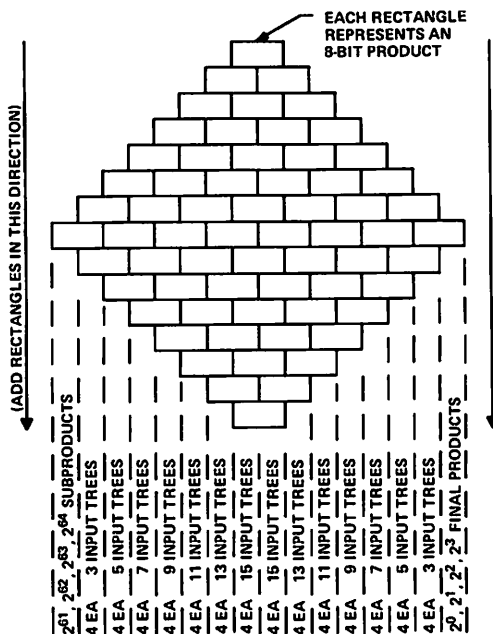
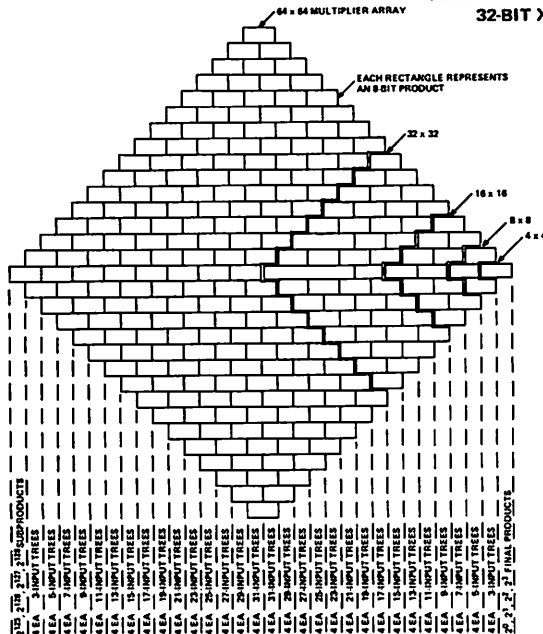


FIGURE 9—FINAL PRODUCTS AND ARRAY SUBPRODUCT ADDITIONS FOR 32-BIT X 32-BIT MULTIPLIER

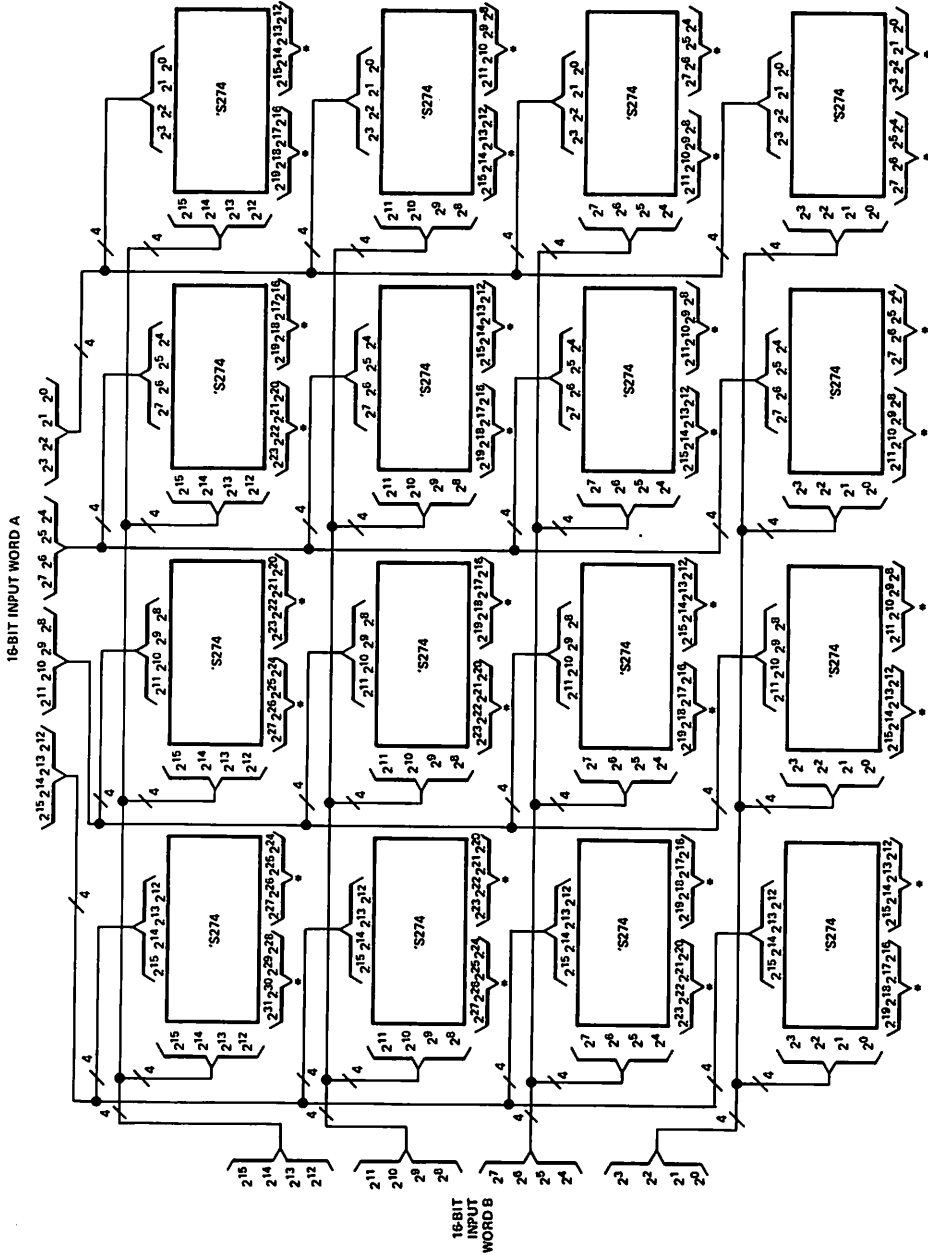


NOTE A: See Note B of Figure 6 for designing trees with any number of inputs up to 31.

FIGURE 10—ARRAY ARRANGEMENT FOR VARIOUS MULTIPLIERS INCLUDING ARRAY SUBPRODUCT ADDITIONS FOR 64-BIT X 64-BIT MULTIPLIER

TYPES SN54S275, SN74S274, SN74S275
4-BIT-BY-4-BIT BINARY MULTIPLIER WITH 3-STATE OUTPUTS
7-BIT-SLICE WALLACE TREES WITH 3-STATE OUTPUTS

TYPICAL APPLICATION DATA



* This 4-bit binary number is a partial product. See Figure 11, Sheets 2 and 3 for diagram of summation process.

FIGURE 11—16-BIT X 16-BIT MULTIPLIER
(SHEET 1 OF 3—INPUT CONNECTIONS)

TYPES SN54S275, SN74S274, SN74S275 **4-BIT-BY-4-BIT BINARY MULTIPLIER WITH 3-STATE OUTPUTS** **7-BIT-SLICE WALLACE TREES WITH 3-STATE OUTPUTS**

TYPICAL APPLICATION DATA

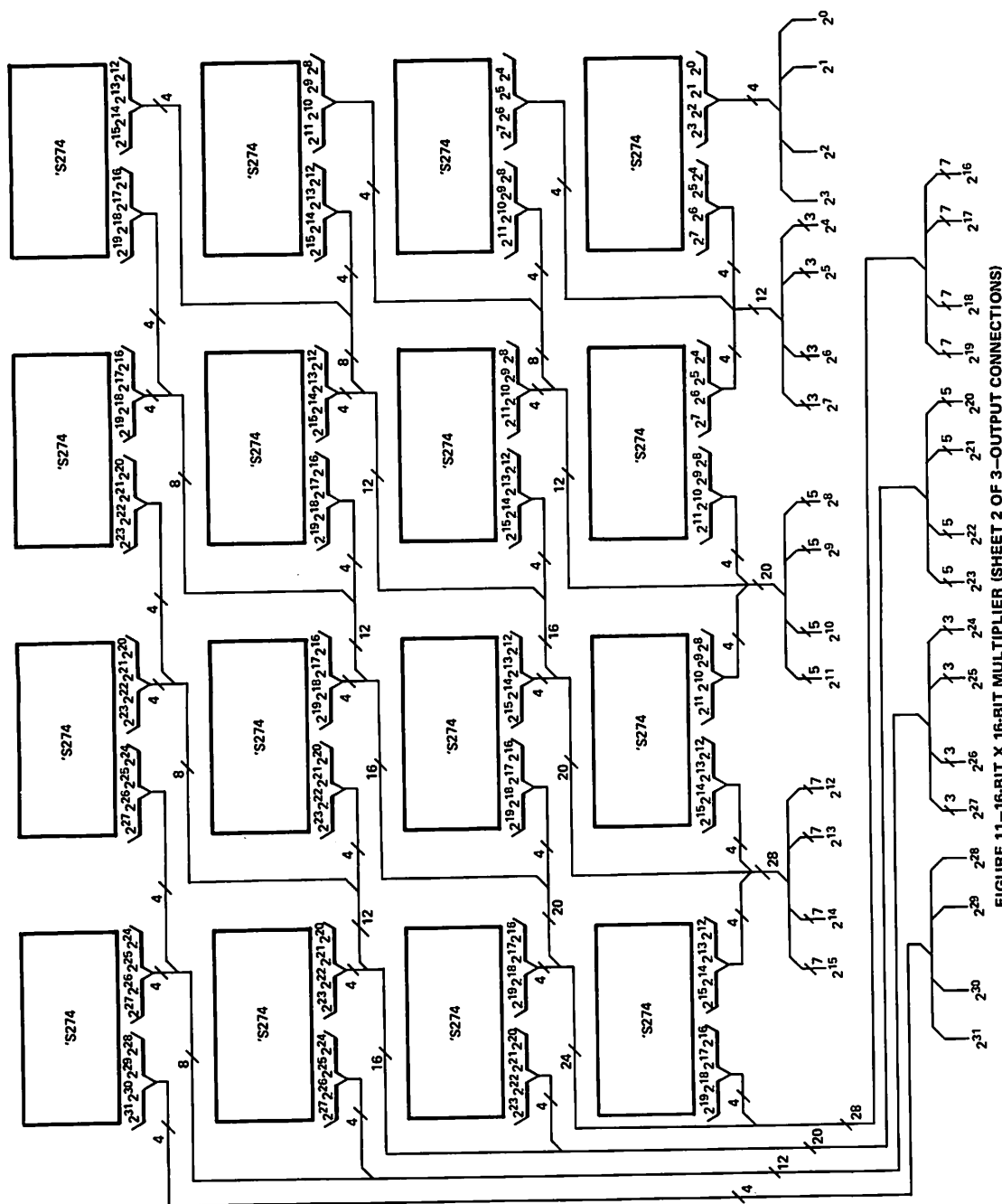
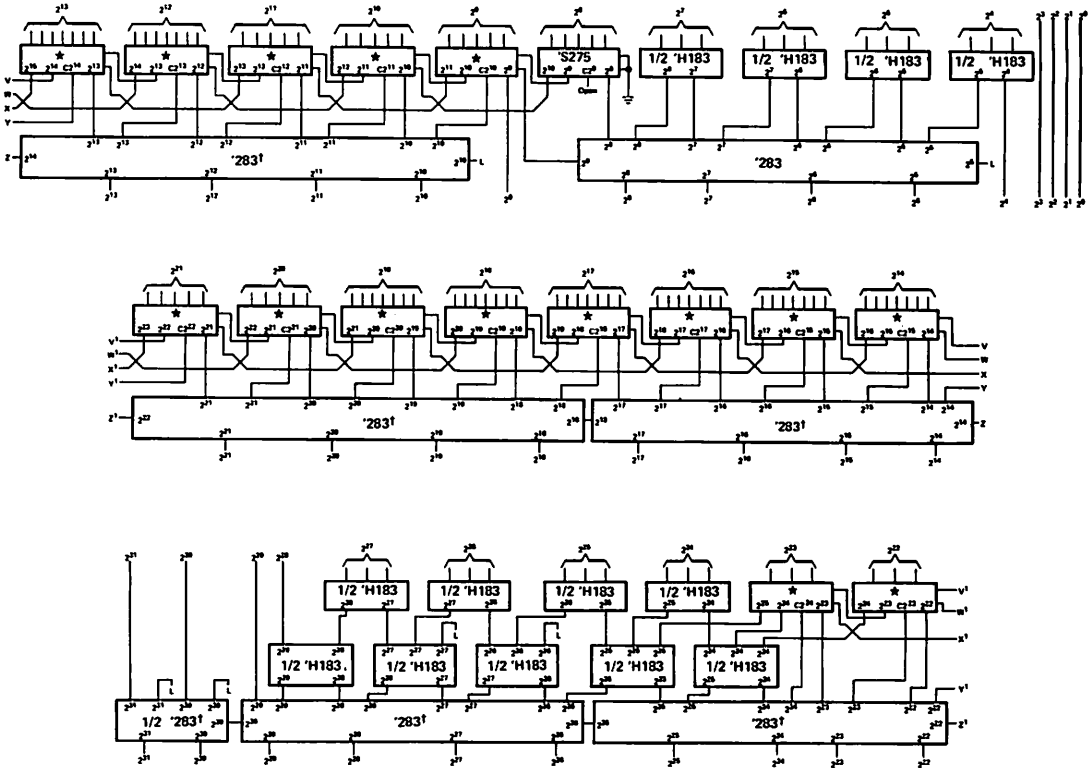


FIGURE 11-16-BIT X 16-BIT MULTIPLIER (SHEET 2 OF 3-OUTPUT CONNECTIONS)

TYPES SN54S275, SN74S274, SN74S275
4-BIT-BY-4-BIT BINARY MULTIPLIER WITH 3-STATE OUTPUTS¹
7-BIT-SLICE WALLACE TREES WITH 3-STATE OUTPUTS

TYPICAL APPLICATION DATA



*Each starred block may be either a basic bit-slice Wallace tree ('S275 only) or a high-speed bit-slice Wallace tree ('S275 plus 1/2 'H183). In either case the function of the terminal is the same as the similarly located terminal of the basic bit-slice (Figure 2) or high-speed bit-slice Wallace tree (Figure 3). Also for either tree, when only five inputs of the seven-input adder of the 'S275 are used, the remaining two inputs must be grounded. When the high-speed adder is used, the C2ⁿ inputs of the 'S275 must be grounded.

[†]For improved performance, SN74S181 ALUs with SN74S182 look-ahead generators can be substituted for the SN74283 adders. Typically, the multiplication time will be reduced by 32 nanoseconds.

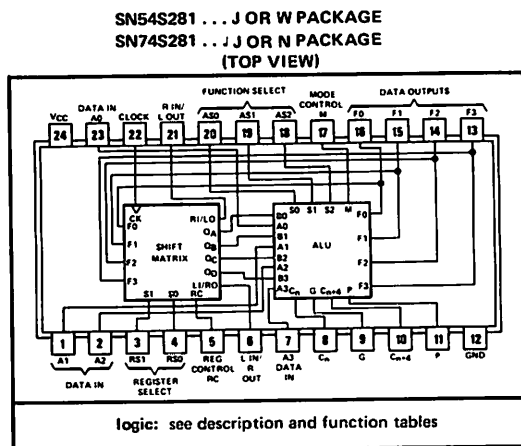
FIGURE 11—16-BIT X 16-BIT MULTIPLIER
(SHEET 3 OF 3—SUMMING PARTIAL PRODUCTS)

TYPES SN54S281, SN74S281

4-BIT PARALLEL BINARY ACCUMULATORS

BULLETIN NO. DLS 7412065, FEBRUARY 1974

- Full 4-Bit Binary Accumulator in a Single Package
- 15 Arithmetic/Logic-Type Operations:
 - Add
 - Subtract ($B-A$ or $A-B$)
 - Complement
 - Increment
 - Transfer
 - Plus 10 Other Functions
- Full Shifting Capabilities:
 - Logic Shift (Left or Right)
 - Arithmetic Shift (Left or Right) for Sign Bit Protection
 - Hold
 - Parallel Load
- Expandable to Handle n-Bit Words with Full Carry Look-Ahead
- Logic Mode Operation Provides Seven Boolean Functions of the Two Variables



description

These Schottky-clamped four-bit accumulators integrate high-performance versions of an arithmetic logic unit/function generator and a shift/storage matrix on a single monolithic circuit bar. The arithmetic logic unit (ALU) portion, similar to the SN54S181/SN74S181 circuit, incorporates the capability to perform 16 arithmetic/logic-type operations as detailed in Table 1. The accumulator includes an exchange of subtract operands by which either $A-B$ or $B-A$ can be accomplished directly. The ALU is controlled by three function-select inputs (AS_0 , AS_1 , AS_2) and a mode-control input (M). When the mode-control input is high, the ALU is placed in a logic mode which performs any of seven logic functions on two binary variables as detailed in Table 2. Full carry look-ahead is provided for fast, simultaneous carry generation for the full four binary bits. The carry input (C_n) and propagate and generate outputs (P , G) are implemented for direct use with the SN54S182/SN74S182 look-ahead carry generators. This permits systems to be implemented with the added advantage of full look-ahead across any word length to minimize the accumulator delay times. Once data is loaded into the accumulator, the typical add time with full look-ahead is 29 nanoseconds for 16-bit words.

The shift/storage matrix is analogous in its capabilities to the SN54S194/SN74S194 universal bidirectional shift register with the added advantages of multiplexed input/output (I/O) cascading lines which comprehend arithmetic shift functions having a sign bit, such as 2's complements. The matrix can be used to perform either logic or arithmetic shifts in either direction (left or right), parallel load, or hold. Control of the register is accomplished with three inputs: register control (RC) and register selection (RS_0 , RS_1). The cascading input/output lines incorporate three-state outputs multiplexed with an input. The least-significant cascading bit is combined with the A_0 , F_0 circuitry to provide the shift-right input and the shift-left output (RI/LO), and the most significant bit is coupled with the A_3 , F_3 circuitry to provide the shift-left input and the shift-right output (LI/RO).

Series 54S circuits are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74S circuits are characterized for operation from 0°C to 70°C .

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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TYPES SN54S281, SN74S281
4-BIT PARALLEL BINARY ACCUMULATORS

FUNCTION TABLES

TABLE 1—ARITHMETIC FUNCTIONS
Mode Control (M) = Low

ALU SELECTION			ACTIVE-HIGH DATA	
AS2	AS1	AS0	C _n = H (with carry)	C _n = L (no carry)
L	L	L	F ₀ = L, F ₁ = F ₂ = F ₃ = H	F _n = H
L	L	H	F = B MINUS A	F = B MINUS A MINUS 1
L	H	L	F = A MINUS B	F = A MINUS B MINUS 1
L	H	H	F = A PLUS B PLUS 1	F = A PLUS B
H	L	L	F = B PLUS 1	F _n = B _n
H	L	H	F = \overline{B} PLUS 1	$\overline{F_n} = \overline{B_n}$
H	H	L	F = A PLUS 1	F _n = A _n
H	H	H	F = \overline{A} PLUS 1	$\overline{F_n} = \overline{A_n}$

TABLE 2—LOGIC FUNCTIONS
Mode Control (M) = High
Carry Input (C_n) = X (Irrelevant)

ALU SELECTION			ACTIVE-HIGH DATA FUNCTION
AS2	AS1	AS0	
L	L	L	F _n = L
L	X	H	F _n = A _n ⊕ B _n
L	H	L	F _n = A _n ⊕ B _n
H	L	L	F _n = A _n B _n
H	L	H	F _n = A _n + B _n
H	H	L	F _n = $\overline{A_n B_n}$
H	H	H	F _n = A _n + B _n

TABLE 3—SHIFT-MODE FUNCTIONS
C_n = M = S0 = S1 = L, and S2 = H

REGISTER SELECTION		REGISTER CONTROL	SHIFT-MATRIX INPUTS				CLOCK INPUT	INPUT/OUTPUT RI/LO	SHIFT-MATRIX OUTPUTS (INTERNAL)				INPUT/OUTPUT LI/RO
RS1	RS0	INPUT	F0	F1	F2	F3			Q _A	Q _B	Q _C	Q _D	
L	L	X	f0	f1	f2	f3	↑	Z	f0	f1	f2	f3	Z
L	H	L	Q _{Bn}	Q _{Cn}	Q _{Dn}	li	↑	Q _{Bn}	Q _{Bn}	Q _{Cn}	Q _{Dn}	li	li
L	H	H	Q _{A0}	Q _{Cn}	Q _{Dn}	li	↑	Q _{Bn}	Q _{Bn}	Q _{Cn}	li	Q _{D0}	li
H	L	L	ri	Q _{An}	Q _{Bn}	Q _{Cn}	↑	ri	ri	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}
H	L	H	ri	Q _{An}	Q _{Bn}	Q _{D0}	↑	ri	ri	Q _{An}	Q _{Bn}	Q _{D0}	Q _{Cn}
H	H	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	↑	Z	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Z
X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	L	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	X

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
Z = high impedance (output off)
↑ = transition from low to high level
f0, f1, f2, f3, ri, li = the level of steady-state conditions at F0, F1, F2, F3, RI/LO, or LI/RO respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent transition of the clock

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S281 (see Note 2)	−55°C to 125°C
SN74S281	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54S281 in the W package operating at free-air temperatures above 110°C requires a heat sink that provides thermal resistance from case to free-air, R_{θCA}, of not more than 20°C/W.

TYPES SN54S281, SN74S281

4-BIT PARALLEL BINARY ACCUMULATORS

recommended operating conditions

		SN54S281			SN74S281			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Any output except LI/RO and RI/LO	-1			-1			mA
	LI/RO and RI/LO	-2			-2			
Low-level output current, I_{OL}	Any output except LI/RO and RI/LO	20			20			mA
	LI/RO and RI/LO	10			10			
Clock frequency, f_{clock} (for shifting)		0			0			MHz
Width of clock pulse, $t_w(\text{clock})$		8			8			
Data setup time with respect to clock, t_{setup}		0†			0†			ns
Data hold time with respect to clock, t_{hold}		18†			18†			
Operating free-air temperature, T_A (see Note 2)		-55			0			70 °C

†The arrow indicates that the rising edge of the clock pulse is used for reference.

NOTE 2: An SN54S281 in the W package operating at free-air temperatures above 110°C requires a heat sink that provides thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 20°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54S281			SN74S281			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage					2			V	
V _{IL}	Low-level input voltage					0.8			V	
V _I	Input clamp voltage	Any input except LI/RO and RI/LO	V _{CC} = MIN, I _I = -18 mA			-1.2			V	
V _{OH}	High-level output voltage	Any output except LI/RO and RI/LO	V _{CC} = MIN, V _{IH} = 2 V,			2.5 3.4			V	
		LI/RO, RI/LO	V _{IL} = 0.8 V, I _{OH} = MAX			2.4 3.4				
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = MAX			0.5			V	
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 5.5 V			1			mA	
I _{IH}	High-level input current	RS0, RS1	V _{CC} = MAX, V _I = 2.7 V, See Note 3			50			μA	
		M, Clock				150				
		LI/RO, RI/LO				200				
		AS2				300				
		All others				250				
I _{IL}	Low-level input current	RS0, RS1, LI/RO	V _{CC} = MAX, V _I = 0.5 V See Note 3			-2			mA	
		RI/LO				-3				
		M, Clock				-4				
		AS0, AS1				-6				
		All others				-8				
I _{OS}	Short-circuit output current‡		V _{CC} = MAX			-40 -110 -40 -110			mA	
I _{CC}	Supply current	V _{CC} = MAX, T _A = 125°C	W package only	190			144 230 144 230			mA
		V _{CC} = MAX	All packages	144 230						

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 3. When testing input current at the RI/LO or LI/RO terminals, the output under test must be in the high-impedance (off) state.

TENTATIVE DATA SHEET

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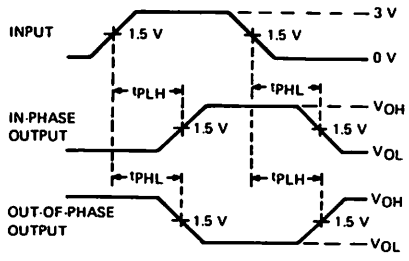
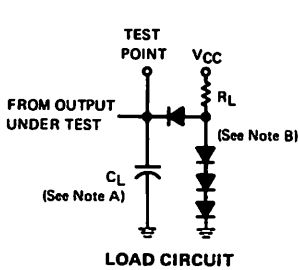
TYPES SN54S281, SN74S281
4-BIT PARALLEL BINARY ACCUMULATORS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	C _n	C _{n+4}	C _L = 15 pF, I/O outputs: R _L = 560 Ω, Other outputs: R _L = 280 Ω, See Figure 1	10	20	ns	
tPHL				10	20		
tPLH	Any A	C _{n+4}		18	30	ns	
tPHL				18	30		
tPLH	C _n	Any F		10	20	ns	
tPHL				10	20		
tPLH	Any A	G		14	24	ns	
tPHL				14	24		
tPLH	Any A	P		12	20	ns	
tPHL				12	20		
tPLH	A _i	F _i		20	35	ns	
tPHL				20	35		
tPLH	A ₀	RI/LO		30	45	ns	
tPHL				30	45		
tPLH	A ₃	LI/RO		30	45	ns	
tPHL				30	45		
tPLH	F ₀	RI/LO		7	11	ns	
tPHL				7	11		
tPLH	F ₃	LI/RO		7	11	ns	
tPHL				7	11		
tPLH	Any AS	Any F or C _{n+4}		28	45	ns	
tPHL				28	45		
tPLH	Any AS	P or G		20	33	ns	
tPHL				20	33		
tPLH	Clock	Any F		30	45	ns	
tPHL				30	45		
tPLH	Clock	RI/LO or LI/RO		35	55	ns	
tPHL				35	55		

[†] t_{PLH} \equiv Propagation delay time, low-to-high-level output
 t_{PHL} \equiv Propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulse is supplied by a generator having the following characteristics: $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$, $PRR \leq 1\text{ MHz}$, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.

FIGURE 1

TENTATIVE DATA SHEET

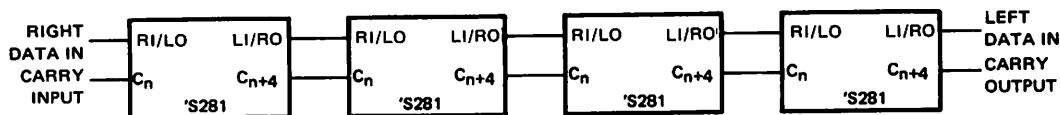
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TYPES SN54S281, SN74S281

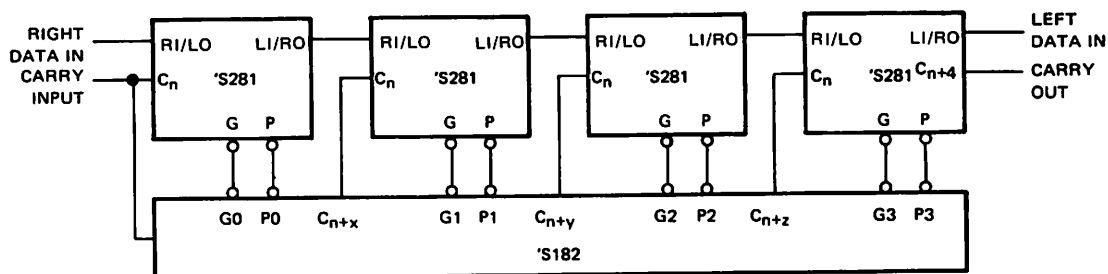
4-BIT PARALLEL BINARY ACCUMULATORS

TYPICAL APPLICATION DATA



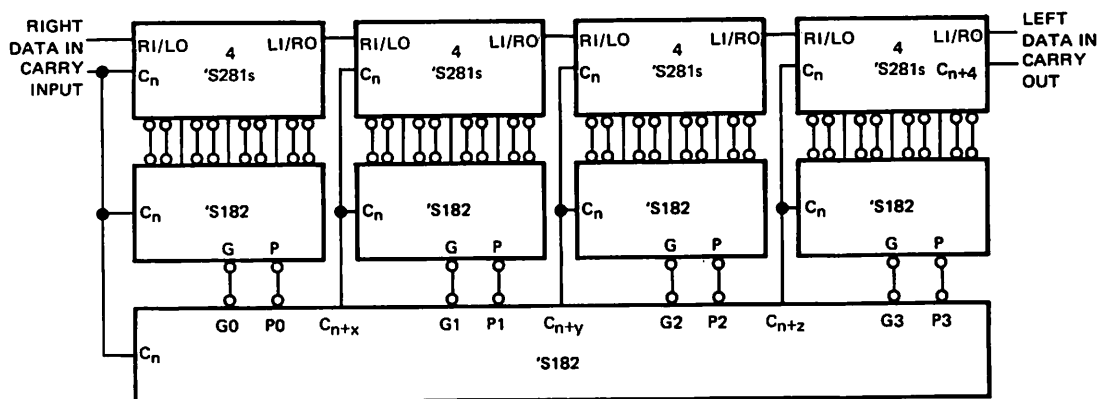
ENTER AND STORE TIME: 38 ns typical
EACH SUCCESSIVE ADDITION TO STORED DATA: 44 ns typical

FIGURE A—16-BIT BINARY ACCUMULATOR USING FOUR SN54S281/SN74S281 CIRCUITS IN RIPPLE-CARRY MODE



ENTER AND STORE TIME: 37 ns typical
EACH SUCCESSIVE ADDITION TO STORED DATA: 29 ns typical

FIGURE B—16-BIT BINARY ACCUMULATOR USING FOUR SN54S281/SN74S281 CIRCUITS AND ONE SN54S182/SN74S182 IN FULL LOOK-AHEAD CARRY MODE



ENTER AND STORE TIME: 42 ns typical
EACH SUCCESSIVE ADDITION TO STORED DATA: 34 ns typical

FIGURE C—64-BIT BINARY ACCUMULATOR USING 16 SN54S281/SN74S281 CIRCUITS AND FIVE SN54S182/SN74S182 CIRCUITS FOR FULL CARRY LOOK-AHEAD

A inputs and F outputs of 'S281 are not shown.

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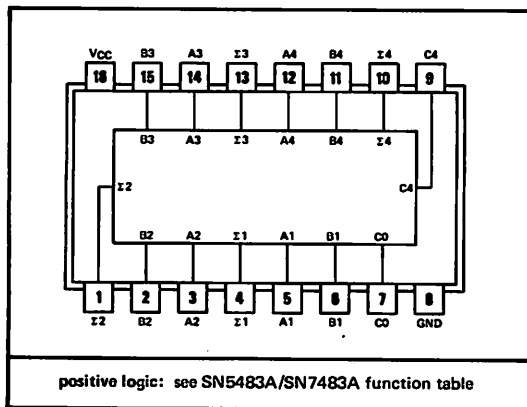
S-275

TYPES SN54283, SN54LS283, SN74283, SN74LS283 4-BIT BINARY FULL ADDERS WITH FAST CARRY

BULLETIN NO. DL-S 7411832, MARCH 1974

- Full-Carry Look-Ahead across the Four Bits
- Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry
- Supply Voltage and Ground on Corner Pins to Simplify P-C Board Layout

SN54283, SN54LS283 . . . J OR W PACKAGE
SN74283, SN74LS283 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see SN5483A/SN7483A function table

description

The '283 and 'L283 adders are electrically and functionally identical to the '83A and 'LS83A respectively; only the arrangement of the terminals has been changed.

These improved full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Designed for medium-speed applications, the circuits utilize transistor-transistor logic that is compatible with most other TTL families and other saturated low-level logic families.

function table and schematics of inputs and outputs

Same as SN5483A/SN7483A and SN54LS83A/SN74LS83A, see pages S-115 and S-116.

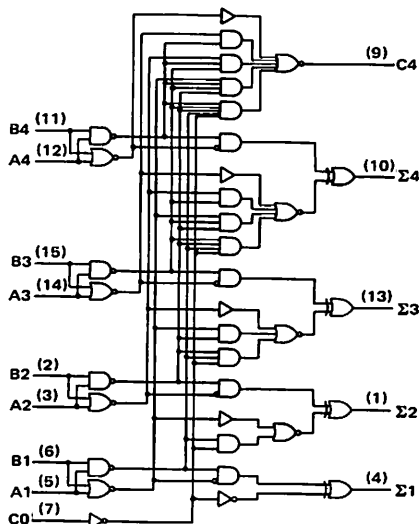
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '283	5.5 V
'LS283	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54283, SN54LS283	-55°C to 125°C
SN74283, SN74LS283	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '283 only between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4.

functional block diagram



TYPES SN54283, SN74283

4-BIT BINARY FULL ADDERS WITH FAST CARRY

recommended operating conditions

			SN54283			SN74283			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Any output except C4		-800			-800			μA
	Output C4		-400			-400			
Low-level output current, I_{OL}	Any output except C4		16			16			mA
	Output C4		8			8			
Operating free-air temperature, T_A			-55			0			$^{\circ}C$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54283			SN74283			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage			0.8			0.8		V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$		-1.5			-1.5		V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4	3.6		2.4	3.6		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = \text{MAX}$		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1			1		mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		40			40		μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.6			-1.6		mA
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-20	-55		-18	-55		mA
	Output C4		-20	-70		-18	-70		
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ All B low, other inputs at 4.5 V		56			56		mA
		Outputs open All inputs at 4.5 V		66	99		66	110	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$.

§ Only one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	C0	Any Σ	CL = 15 pF, RL = 400 Ω, See Note 3	14	21	ns	
tPHL				12	21		
tPLH	Ai or Bi	Σi		16	24	ns	
tPHL				16	24		
tPLH	C0	C4	CL = 15 pF, RL = 780 Ω, See Note 3	9	14	ns	
tPHL				11	16		
tPLH	Ai or Bi	C4		9	14	ns	
tPHL				11	16		

¶ t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

NOTE 3: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54LS283, SN74LS283
4-BIT BINARY FULL ADDERS WITH FAST CARRY

recommended operating conditions

	SN54LS283			SN74LS283			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS283			SN74LS283			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage			0.7			0.8		V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5			-1.5		V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.4	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_I	Input current at maximum input voltage	Any A or B C0		0.2			0.2		mA
		$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1		
I_{IH}	High-level input current	Any A or B C0		40			40		μ A
		$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20		
I_{IL}	Low-level input current	Any A or B C0		-0.8			-0.8		mA
		$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4			-0.4		
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-6	-40		-5	-42		mA
I_{CC}	Supply current	All inputs grounded	22	39		22	39		mA
		All B low, other inputs at 4.5 V	19	34		19	34		
		All inputs at 4.5 V	19	34		19	34		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Only one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
tPLH	C0	Any Σ	CL = 15 pF, See Note 4	RL = 2 kΩ,		16	24	ns
tPHL						15	24	
tPLH	Ai or Bi	Σi				15	24	ns
tPHL						15	24	
tPLH	C0	C4				11	17	ns
tPHL						11	17	
tPLH	Ai or Bi	C4				11	17	ns
tPHL						12	17	

¶ t_{PLH} \equiv Propagation delay time, low-to-high-level output

t_{PHL} \equiv Propagation delay time, high-to-low-level output

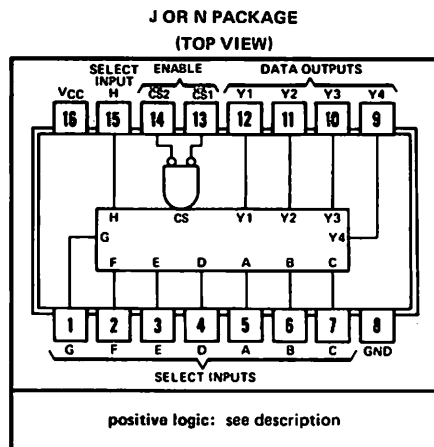
NOTE 4: Load circuit and voltage waveforms are shown on page S-88.

TYPE SN74S287

1024-BIT PROGRAMMABLE READ-ONLY MEMORY WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7412090, MARCH 1974—REVISED MAY 1974

- Provides the Versatility of Custom Designs Virtually "Off the Shelf"
- Applications Include:
 - Microprogramming
 - Look-up Tables for any Fixed Program
 - Parallel Code Converters
 - Sequence, Routine, and Subroutine Generators
 - Random-Logic Function Generator
- Schottky-Clamped for High Performance:
 - Chip-Select Access Time . . . 15 ns Typ
 - Address Access Time . . . 40 ns Typ
- Interchangeable with Most Other 256-Word-by-4-Bit TTL PROMs/ROMs
- Bus-Driving, 3-State Outputs for Easy Word Expansion
- SN74S387 Is Functionally Equivalent but Has Open-Collector Outputs
- Fully Decoded, Low-Current P-N-P Inputs
- Fully Compatible with Most TTL and Other Saturated Low-Level Logic Families



description

The SN74S287 is a field-programmable, 1024-bit, read-only memory organized as 256 words of four bits each. This monolithic, high-speed, Schottky-clamped TTL memory array is addressed in eight-bit binary with full on-chip decoding. Two overriding chip-select inputs are provided which, when either one or both are high, cause all four three-state outputs to assume a high-impedance state. This memory features p-n-p input transistors, which reduce the low-level-input-current requirement to a maximum of -0.25 milliamperes, only one-eighth that of a Series 74S standard load. The organization is expandable with no additional output buffering, as shown in Table 1 below.

The address of a four-bit word is accomplished through the buffered binary select inputs in coincidence with a low level at both chip-select inputs. Where multiple 'S287 devices are used in a memory system, the chip-select inputs allow easy decoding of additional address bits.

Data can be electronically programmed, as desired, at any of the 1024 bit locations in accordance with the programming procedure specified. Prior to programming, the memory contains a high-logic-level output condition at all bit locations. The programming procedure open-circuits metal links which results in a low-logic-level output at the selected locations. The procedure is irreversible; once altered, the output for that bit is permanently programmed to provide a low logic level. Outputs never having been altered may later be programmed to supply a low-level output. Operation of the device within the recommended operating conditions will not alter the memory content.

The three-state output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs (see Table 1), yet it retains the fast-rise-time characteristic of the TTL totem-pole output.

TABLE 1
WORD CAPACITY vs 74S LOADS

SERIES 74S LOADS	MAX NO. OF COMBINED OUTPUTS†	MAX NO. OF WORDS
1	129	33 024
2	128	32 768
3	120	30 720
4	80	20 480
5	40	10 240

†Total number of outputs connected to each common bus

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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TYPE SN74S287

1024-BIT PROGRAMMABLE READ-ONLY MEMORY WITH 3-STATE OUTPUTS

step-by-step programming procedure

1. Apply steady-state supply voltage ($V_{CC} = 5$ volts) and address the word to be programmed. See recommended conditions for programming on the following page.
2. Verify that the bit location needs to be programmed. (With the load circuit of Figure A, an unprogrammed output will be at 2 volts or greater; a programmed output will be at 0.8 volts or less.) If a bit is already programmed, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to both chip-select inputs.
4. Only one bit location is programmed at a time. Apply the load circuit of Figure A to the outputs not being programmed; then, ground the output to be programmed as a low logic level.
5. Ramp V_{CC} to 10.5 volts nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to both chip-select inputs. This should occur between 10 microseconds and 1 millisecond after V_{CC} has reached its 10.5-volt level. See programming sequence of Figure B.
7. After the X program pulse time (1 millisecond) is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within 10 microseconds to 1 millisecond after the chip-select inputs reach a high logic level, V_{CC} should be ramped down to 5 volts at which level verification can be accomplished.
9. The chip-select inputs may be taken to a low logic level (to permit program verification) 10 microseconds or more after V_{CC} reaches its steady-state value of 5 volts.
10. At a Y pulse duty cycle of 10% or less, repeat steps 1 through 8 for each output where a bit at this address is desired to be programmed.

NOTES: A) V_{CC} should be removed between program pulses to reduce total average power dissipation and resultant chip temperatures. See Figure B.

B) When verification indicates that a bit did not program (output is 2 volts or greater), repeat steps 3 through 9. If the bit did not program after the second application of a 1 millisecond X pulse, repeat steps 3 through 9 using an X pulse time of 50 to 75 milliseconds. Regardless of the X duration, the total average pulse time of Y should be no more than 10% of the programming cycle.

C) The circuit shown in Figure A, or equivalent, is used to limit voltage to 6 volts or less for outputs not being programmed.

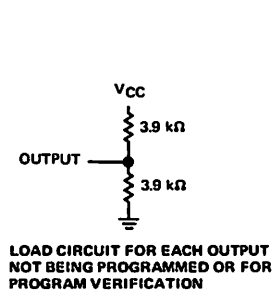


FIGURE A

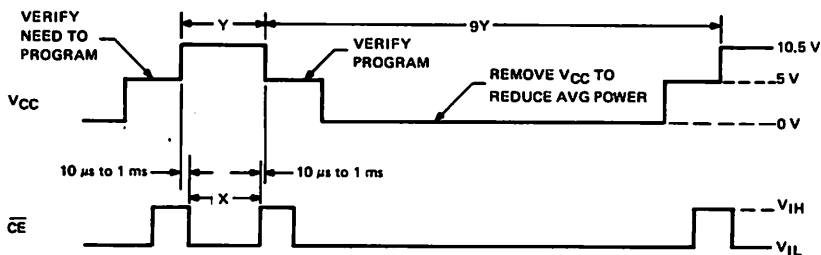


FIGURE B

TYPE SN74S287

1024-BIT PROGRAMMABLE READ-ONLY MEMORY WITH 3-STATE OUTPUTS

recommended conditions for programming

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 1)	Steady state	4.75	5	5.25	V
	Program pulse	10	10.5	11 [†]	
Input voltage	High level	2.4		5	V
	Low level	0		0.5	
Output conditions for programming	To a high logic level	See Figure A			V
	To a low logic level		0	-0.8	
Duration of programming pulse X (see Figure B)		1		75	ms

NOTE 1: All voltage values are with respect to network ground terminal.

[†] Absolute maximum rating

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 2)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. This rating applies at all times except during programming.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			-6.5	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = \text{MAX}$	2.4	3.2		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$			0.5	V
I_{OZH} Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_O = 2.4 \text{ V}$			50	μA
I_{OZL} Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_O = 0.5 \text{ V}$			-50	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			25	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.5 \text{ V}$			-250	μA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-30		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 3		110	150	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

NOTE 3: I_{CC} is measured with outputs open and both \overline{CS} inputs grounded.

TYPE SN74S287 1024-BIT PROGRAMMABLE READ-ONLY MEMORY WITH 3-STATE OUTPUTS

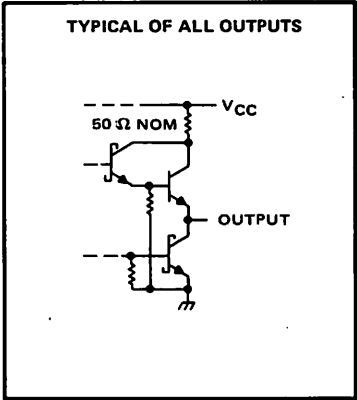
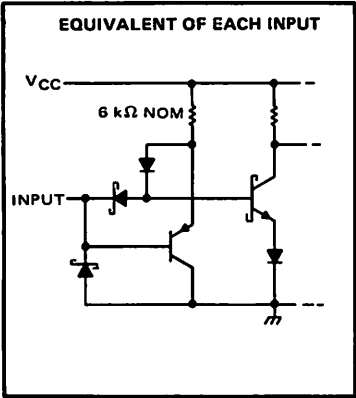
switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Address	Any	$C_L = 30\text{ pF}$, See Notes 4 and 5		42	60	ns
t_{PHL}					42	60	
t_{ZH}	Chip select	Any			15	30	ns
t_{ZL}					15	30	
t_{HZ}	Chip select	Any	$C_L = 5\text{ pF}$, See Notes 4 and 5		12		ns
t_{LZ}					12		

[†] t_{PLH} \equiv propagation delay time, low-to-high-level output
 t_{PHL} \equiv propagation delay time, high-to-low-level output
 t_{ZH} \equiv output enable time to high level
 t_{ZL} \equiv output enable time to low level
 t_{HZ} \equiv output disable time from high level
 t_{LZ} \equiv output disable time from low level

NOTES: 4. When measuring times from address inputs, both $\overline{CS1}$ and $\overline{CS2}$ are low. When measuring times from chip-select inputs, the address inputs are held steady.
5. Load circuit and waveforms are shown on page S-87.

schematics of inputs and outputs



TYPES SN54S289, SN74S289

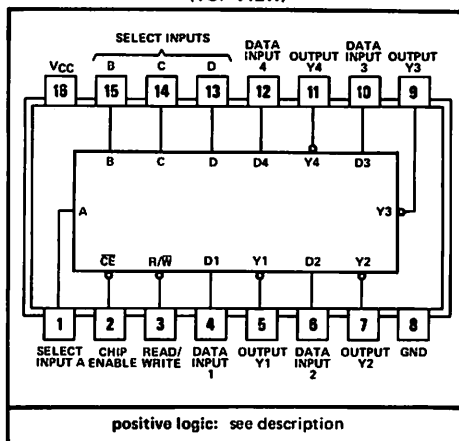
64-BIT RANDOM-ACCESS MEMORIES

WITH OPEN-COLLECTOR OUTPUTS

BULLETIN NO. DL-S 7412108, MARCH 1974

- Schottky-Clamped for High-Speed Buffer/Scratchpad Memory Systems:
Access from Chip-Enable Inputs . . . 12 ns Typ
Access from Address Inputs . . . 25 ns Typ
- Open-Collector Outputs for Controlled-Impedance Bus Lines
- SN54S189, SN74S189 Are Functionally Equivalent But Have Three-State Outputs
- SN54S289 Is Guaranteed for Operation Over the Full Military Temperature Range of -55°C to 125°C
- Compatible with Most TTL and DTL Logic Circuits
- Chip-Enable Input Simplifies Word Expansion
- Direct Replacement for Intel 3101A in Most Applications

SN54S289 . . . J OR W PACKAGE
SN74S289 . . . J OR N PACKAGE
(TOP VIEW)



description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature p-n-p input transistors that reduce the low-level input current requirement to a maximum of -0.25 milliamperes, only one-eighth that of a Series 54S/74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

write cycle

The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are at a high logic level (off).

read cycle

The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable input is low. When the chip-enable input is high, the outputs are high (off).

FUNCTION TABLE

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	H
Read	L	H	Stored Data
Inhibit	H	X	H

H = high level, L = low level, X = irrelevant

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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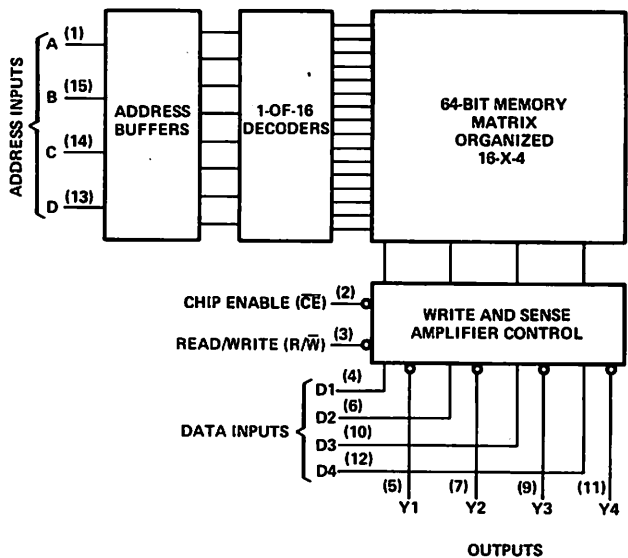
TYPES SN54S289, SN74S289

64-BIT RANDOM-ACCESS MEMORIES WITH OPEN-COLLECTOR OUTPUTS

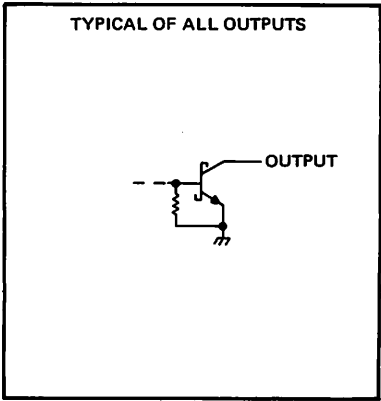
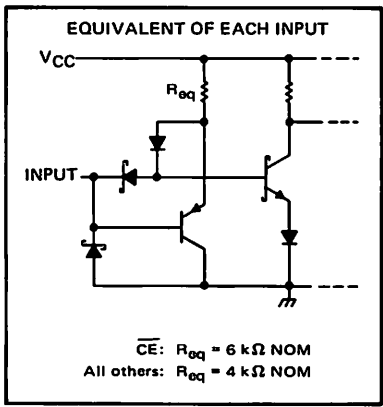
description (continued)

The fast access time of the 'S289 makes it particularly attractive for implementing high-performance memory functions requiring access times on the order of 25 nanoseconds. The unique functional capability of the 'S289 outputs being high during writing combined with the data inputs being inhibited during reading means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

functional block diagram



schematics of inputs and outputs



TYPES SN54S289, SN74S289

64-BIT RANDOM-ACCESS MEMORIES WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54S289	-55°C to 125°C
SN74S289	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54S289			SN74S289			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				16			16	mA
Width of write-enable pulse (read/write low), t_W		25			25			ns
Setup time, t_{setup} (see Figure 1)	Address to read/write	0↓			0↓			ns
	Data to read/write	25↑			25↑			
	Chip enable to read/write	0↓			0↓			
Hold time, t_{hold} (see Figure 1)	Address from read/write	0↑			0↑			ns
	Data from read/write	0↑			0↑			
	Chip enable from read/write	0↑			0↑			
Operating free-air temperature, T_A		-55		125	0		70	°C

†‡The arrow indicates the transition of the read/write input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S289		SN74S289		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IH}	High-level input voltage			2			2	V
V _{IL}	Low-level input voltage					0.8		0.8
V _I	Input clamp voltage	V _{CC} = MIN, I _I = −18 mA				−1.2		−1.2
I _{OH}	High-level output current	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V	V _{OH} = 2.4 V			40		40
			V _{OH} = 5.5 V			100		100
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA				0.5		0.45
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V				1		1
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V				25		25
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5 V				−250		−250
I _{CC}	Supply current	V _{CC} = MAX, See Note 2				75	105	75
								105

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTES: 1. All voltage values are with respect to network ground terminal.

2. I_{CC} is measured with the read/write and chip-enable inputs grounded, all other inputs at 4.5 V, and the outputs open.

TYPES SN54S289, SN74S289

64-BIT RANDOM-ACCESS MEMORIES WITH OPEN-COLLECTOR OUTPUTS

switching characteristics over recommended operating ranges of V_{CC} and T_A (unless otherwise noted)

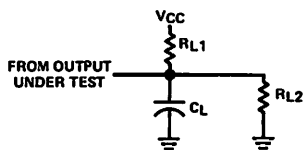
PARAMETER [§]		TEST CONDITIONS	SN54S289			SN74S289			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
t_{PLH}	Access times from address	$C_L = 30 \text{ pF}$, $R_{L1} = 300 \Omega$, $R_{L2} = 600 \Omega$, See Figure 1	25	50		25	35		ns
t_{PHL}	Disable time from chip enable		25	50		25	35		
t_{PLH}	Enable time from chip enable		12	25		12	17		ns
t_{PHL}	Enable time from chip enable		12	25		12	17		ns
t_{SR}	Sense-recovery time		22	40		22	35		ns

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

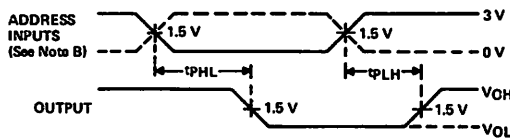
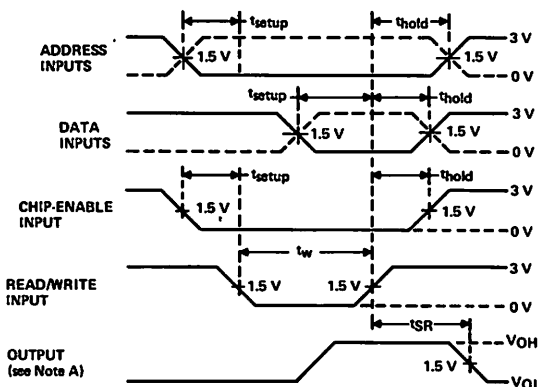
[§] $t_{PLH} \equiv$ propagation delay time, low-to-high-level output; $t_{PHL} \equiv$ propagation delay time, high-to-low-level output

$t_{SR} \equiv$ recovery time for valid data after writing

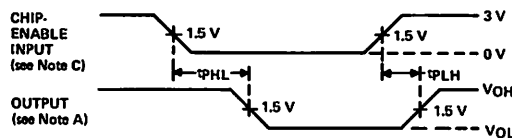
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS
VOLTAGE WAVEFORMS



ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP ENABLE
VOLTAGE WAVEFORMS

- NOTES: A. Waveform shown is for the output with internal conditions such that the output is low except when disabled.
B. When measuring delay times from address inputs, the chip-enable input is low and the read/write input is high.
C. When measuring delay times from chip-onable input, the address inputs are steady-state and the read/write input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r < 2.5 \text{ ns}$, $t_f < 2.5 \text{ ns}$, $\text{PRR} < 1 \text{ MHz}$, and $Z_{out} \approx 50 \Omega$.

FIGURE 1

TYPES SN54290, SN54293, SN54LS290, SN54LS293 SN74290, SN74293, SN74LS290, SN74LS293 DECADE AND 4-BIT BINARY COUNTERS

BULLETIN NO. DL-S 7411833, MARCH 1974

'290, 'LS290 . . . DECADE COUNTERS
'293, 'LS293 . . . 4-BIT BINARY COUNTERS

- GND and VCC on Corner Pins
(Pins 7 and 14 Respectively)

description

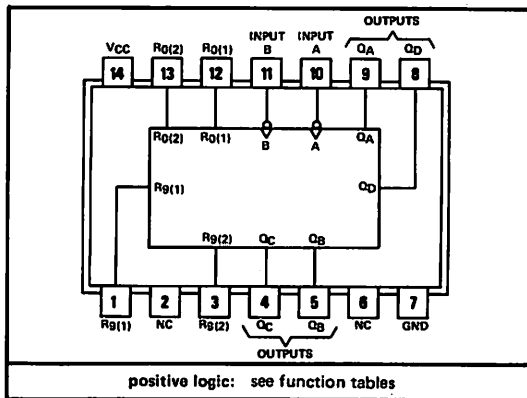
The SN54290/SN74290, SN54LS290/SN74LS290, SN54293/SN74293, and SN54LS293/SN74LS293 counters are electrically and functionally identical to the SN5490A/SN7490A, SN54LS90/SN74LS90, SN5493A/SN7493A, and SN54LS93/SN74LS93, respectively. Only the arrangement of the terminals has been changed for the '290, 'LS290, '293, and 'LS293.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '290 and 'LS290 and divide-by-eight for the '293 and 'LS293.

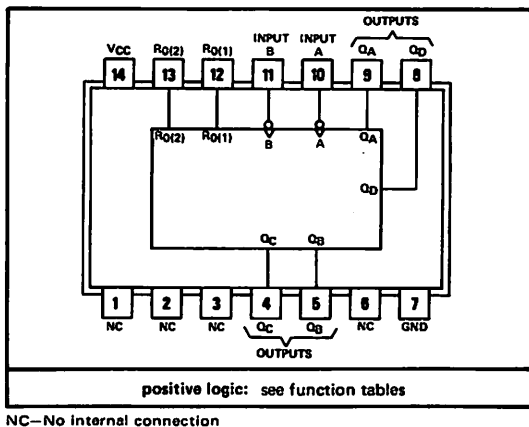
All of these counters have a gated zero reset and the '290 and 'LS290 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '290 and 'LS290 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

SN54290, SN54LS290 . . . J OR W PACKAGE
SN74290, SN74LS290 . . . J OR N PACKAGE
(TOP VIEW)



SN54293, SN54LS293 . . . J OR W PACKAGE
SN74293, SN74LS293 . . . J OR N PACKAGE
(TOP VIEW)



TYPES SN54290, SN54293, SN54LS290, SN54LS293, SN74290, SN74293, SN74LS290, SN74LS293 DECADE AND 4-BIT BINARY COUNTERS

**'290, 'LS290
BCD COUNT SEQUENCE
(See Note A)**

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

**'290, 'LS290
BI-QUINARY (5-2)
(See Note B)**

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

**'290, 'LS290
RESET/COUNT FUNCTION TABLE**

RESET INPUTS				OUTPUT			
R ₀ (1)	R ₀ (2)	R ₉ (1)	R ₉ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

**'293, 'LS293
COUNT SEQUENCE
(See Note C)**

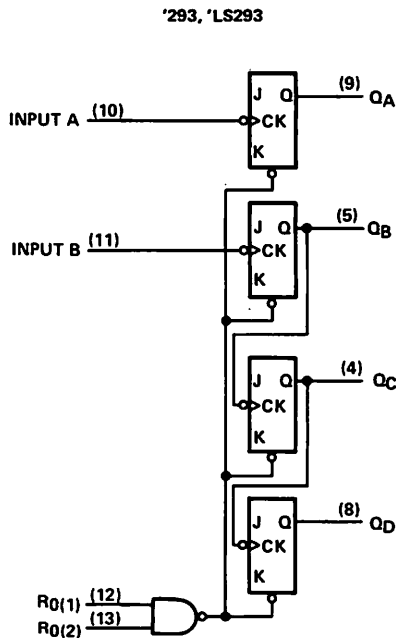
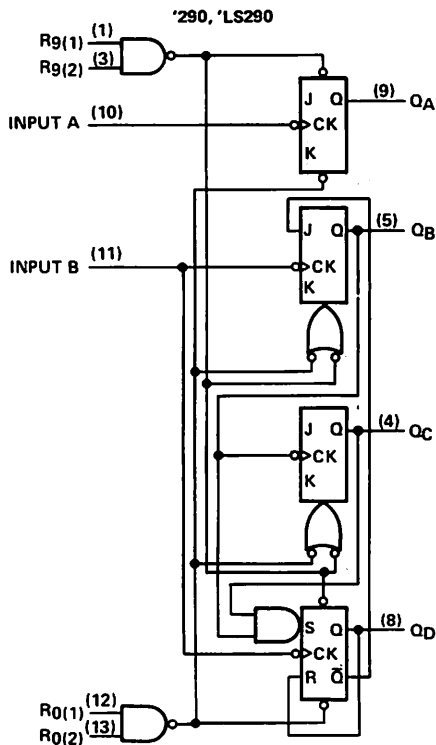
COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

**'293, 'LS293
RESET/COUNT FUNCTION TABLE**

RESET INPUTS		OUTPUT			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

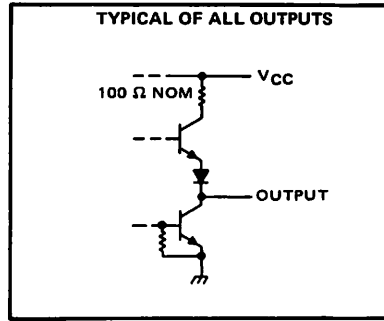
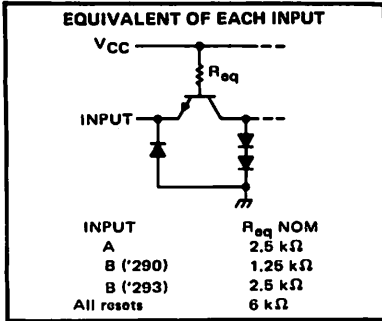
functional block diagrams



The J and K inputs shown without connection are for reference only and are functionally at a high level.

TYPES SN54290, SN54293, SN74290, SN74293 DECADE AND 4-BIT BINARY COUNTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Intermitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54' Circuits	-55°C to 125°C
SN74' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

- NOTES: 1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_0 inputs, and for the '290 circuit, it also applies between the two R_0 inputs.

recommended operating conditions

		SN54'			SN74'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-800			-800			μ A
Low-level output current, I_{OL}		16			16			mA
Count frequency, f_{count}	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup time, t_{setup}		25			25			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

TYPES SN54290, SN54293, SN74290, SN74293
DECADE AND 4-BIT BINARY COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'290			'293			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
V _I	Input clamp voltage	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 µA	2.4	3.4		2.4	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA¶		0.2	0.4		0.2	0.4	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	High-level input current	Any reset			40			40	µA
		A input			80			80	
		B input			120			80	
I _{IL}	High-level input current	Any reset			-1.6			-1.6	mA
		A input			-3.2			-3.2	
		B input			-4.8			-3.2	
I _{OS}	Short-circuit output current§	V _{CC} = MAX	SN54'	-20	-57	-20		-57	mA
			SN74'	-18	-57	-18		-57	
I _{CC}	Supply current	V _{CC} = MAX, See Note 3		29	42		26	39	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

¶Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER ^o	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'290			'293			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	A	Q _A	C _L = 15 pF, R _L = 400 Ω, See Note 4	32	42		32	42		MHz
	B	Q _B		16			16			
t _{PLH}	A	Q _A		10	16		10	16		ns
t _{PHL}				12	18		12	18		
t _{PLH}	A	Q _D		32	48		46	70		ns
t _{PHL}				34	50		46	70		
t _{PLH}	B	Q _B		10	16		10	16		ns
t _{PHL}				14	21		14	21		
t _{PLH}	B	Q _C		21	32		21	32		ns
t _{PHL}				23	35		23	35		
t _{PLH}	B	Q _D		21	32		34	51		ns
t _{PHL}				23	35		34	51		
t _{PHL}	Set-to-0	Any		26	40		26	40		ns
t _{PLH}	Set-to-9	Q _A , Q _D		20	30					ns
t _{PHL}		Q _B , Q _C		26	24					

°f_{max} ≡ maximum count frequency

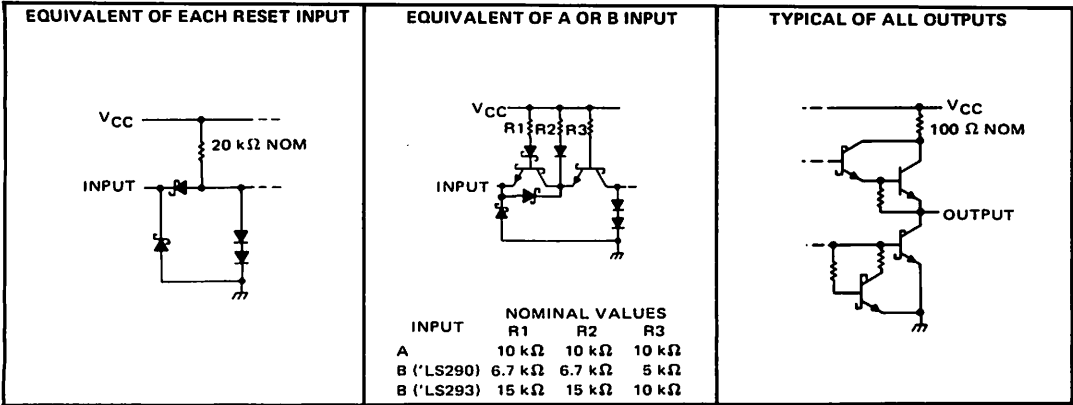
τ_{PLH} ≡ propagation delay time, low-to-high-level output

τ_{PHL} ≡ propagation delay time, high-to-low-level output

NOTE 4: Load circuit and voltage waveforms are the same as those shown for the '90A and '93A, page S-135.

TYPES SN54LS290, SN54LS293, SN74LS290, SN74LS293
DECADE AND 4-BIT BINARY COUNTERS

schematics of inputs and outputs



3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 5)	7 V
Input voltage: R inputs	7 V
A and B inputs	5.5 V
Operating free-air temperature range: SN54LS290, SN54LS293	-55°C to 125°C
SN74LS290, SN74LS293	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 5: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-400			-400			μA
Low-level output current, I_{OL}		4			4			mA
Count frequency, f_{count}	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15		15	15		15	ns
	B input	30		30	30		30	
	Reset inputs	15		15	15		15	
Reset inactive-state setup time, t_{setup}		25		25	25		25	ns
Operating free-air temperature, T_A		-55		125	0		70	°C

TENTATIVE DATA

374 This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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TYPES SN54LS290, SN54LS293, SN74LS290, SN74LS293
DECADE AND 4-BIT BINARY COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _I	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max			I _{OL} = 4 mA¶			I _{OL} = 4 mA¶	V
					I _{OL} = 8 mA¶			I _{OL} = 8 mA¶	
I _I	Input current at maximum input voltage	Any reset			V _{CC} = MAX, V _I = 7 V			0.1	mA
		A input						0.4	
		B of 'LS290			V _{CC} = MAX, V _I = 5.5 V			0.8	
		B of 'LS293						0.4	
I _{IH}	High-level input current	Any reset			V _{CC} = MAX, V _I = 2.7 V			20	µA
		A input						80	
		B of 'LS290						160	
		B of 'LS293						80	
I _{IL}	Low-level output current	Any reset			V _{CC} = MAX, V _I = 0.4 V			-0.4	mA
		A input						-2.4	
		B of 'LS290						-3.2	
		B of 'LS293						-1.6	
I _{OS}	Short-circuit output current§	V _{CC} = MAX	-6		-40	-5		-42	mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 3			'LS290	9	15	9	mA
					'LS293	9	15	9	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

¶Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS290			'LS293			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	A	Q _A	C _L = 15 pF, R _L = 400 Ω, See Note 6	32	42		32	42		MHz
	B	Q _B		16			16			
t _{PLH}	A	Q _A			10	16		10	16	ns
t _{PHL}		Q _A			12	18		12	18	
t _{PLH}	A	Q _D			32	48		46	70	ns
t _{PHL}		Q _D			34	50		46	70	
t _{PLH}	B	Q _B			10	16		10	16	ns
t _{PHL}		Q _B			14	21		14	21	
t _{PLH}	B	Q _C			21	32		21	32	ns
t _{PHL}		Q _C			23	35		23	35	
t _{PLH}	B	Q _D			21	32		34	51	ns
t _{PHL}		Q _D			23	35		34	51	
t _{PHL}	Set-to-0	Any			26	40		26	40	ns
t _{PLH}	Set-to-9	Q _A , Q _D			20	30				ns
t _{PHL}		Q _B , Q _C			26	24				

*f_{max} ≡ maximum count frequency

t_{PLH} ≡ propagation delay time, low-to-high-level output

t_{PHL} ≡ propagation delay time, high-to-low-level output

NOTE 6: Load circuit and voltage waveforms are the same as those shown for the 'LS90 and 'LS93, page S-135.

TENTATIVE DATA

S-292

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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374

TYPES SN54LS295A, SN74LS295A

4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7411780, MARCH 1974

- Three-State Versions of SN54LS95B and SN74LS95B Parallel-In, Parallel-Out Registers
- Schottky-Diode-Clamped Transistors
- Low Power Dissipation . . . 70 mW Typical (Enabled)
- Applications:
 - N-Bit Serial-To-Parallel Converter
 - N-Bit Parallel-To-Serial Converter
 - N-Bit Storage Register

description

These 4-bit registers feature parallel inputs, parallel outputs, and clock, serial, mode, and output control inputs. The registers have three modes of operation:

Parallel (broadside) load

Shift right (the direction Q_A toward Q_D)

Shift left (the direction Q_D toward Q_A)

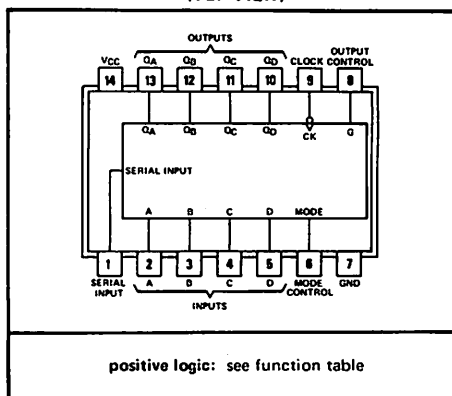
Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

Shift right is accomplished when the mode control is low; shift left is accomplished when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D.

When the output control is high, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a low logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected.

The SN54LS295A is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74LS295A is characterized for operation from 0°C to 70°C .

SN54LS295A . . . J OR W PACKAGE
SN74LS295A . . . J OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

MODE CONTROL		INPUTS				OUTPUTS			
		CLOCK	SERIAL	PARALLEL				Q_A	Q_B
				A	B	C	D	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}
H	↓	X	X	a	b	c	d	Q_{C0}	Q_{D0}
H	↓	X	X	Q_{B}^{\dagger}	Q_{C}^{\dagger}	Q_{D}^{\dagger}	d	Q_{A0}	Q_{B0}
L	H	X	X	X	X	X	X	Q_{C0}	Q_{D0}
L	↓	H	X	X	X	X	X	Q_{A0}	Q_{B0}
L	↓	L	X	X	X	X	X	Q_{C0}	Q_{D0}

When the output control is low, the outputs are disabled to the high-impedance state; however, sequential operation of the registers is not affected.

[†]Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level.

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the indicated steady-state input conditions were established.

Q_{An} , Q_{Bn} , Q_{Cn} , Q_{Dn} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the most-recent ↓ transition of the clock.

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES SN54LS295A, SN74LS295A
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS
WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Table with 2 columns: Parameter and Value. Parameters include Supply voltage (VCC), Input voltage, Operating free-air temperature range for SN54LS295A and SN74LS295A, and Storage temperature range.

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

Table with 4 columns: Parameter, SN54LS295A (MIN, NOM, MAX), SN74LS295A (MIN, NOM, MAX), and UNIT. Parameters include Supply voltage, High-level output current, Low-level output current, Clock frequency, Width of clock pulse, Setup time, Hold time, and Operating free-air temperature.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Table with 5 columns: PARAMETER, TEST CONDITIONS†, SN54LS295A (MIN, TYP‡, MAX), SN74LS295A (MIN, TYP‡, MAX), and UNIT. Parameters include input/output voltages, currents, and supply current under various test conditions.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at VCC = 5 V, TA = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: ICC is measured with the outputs open, the serial input and mode control at 4.5 V, and the data inputs grounded under the following conditions:
A. Output control at 4.5 V and a momentary 3 V, then ground, applied to clock input.
B. Output control and clock input grounded.

TYPES SN54LS295A, SN74LS295A

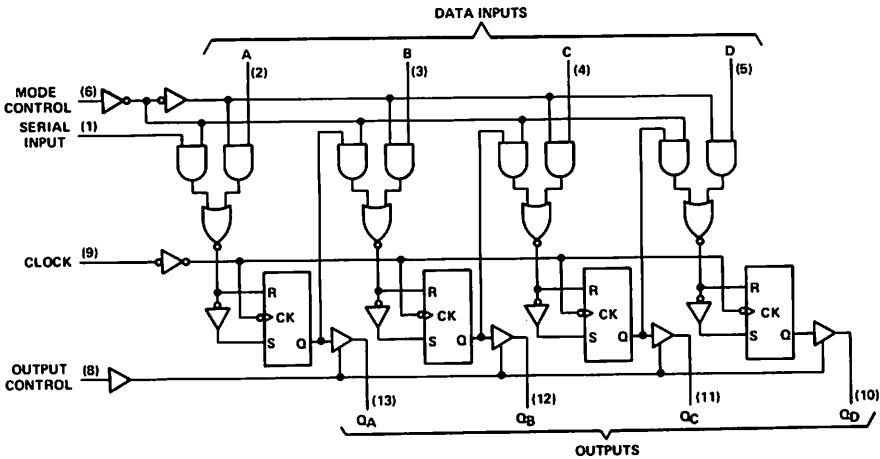
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$

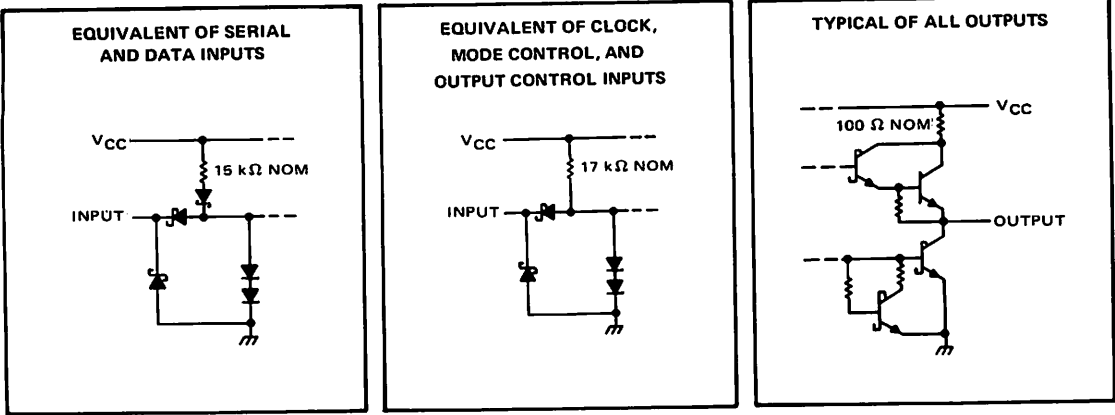
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15\text{ pF}$, See Note 3	20	28		MHz
t_{PLH} Propagation delay time, low-to-high-level output		40	60		ns
t_{PHL} Propagation delay time, high-to-low-level output		47	70		ns
t_{ZH} Output enable time to high level		15	25		ns
t_{ZL} Output enable time to low level		21	30		ns
t_{HZ} Output disable time from high level	$C_L = 5\text{ pF}$, See Note 3	39	60		ns
t_{LZ} Output disable time from low level		32	50		ns

NOTE 3: Load circuit and voltage waveforms are shown on page S-88.

functional block diagram



schematics of inputs and outputs



- Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock
- Applications:
 - Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data
 - Implement Separate Registers Capable of Parallel Exchange of Contents Yet Retain External Load Capability
 - Universal Type Register for Implementing Various Shift Patterns; Even Has Compound Left-Right Capabilities

description

These monolithic quadruple two-input multiplexers with storage provide essentially the equivalent functional capabilities of two separate MSI functions (SN54157/SN74157 or SN54LS157/SN74LS157 and SN54175/SN74175 or SN54LS175/SN74LS175) in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

Typical power dissipation is 195 milliwatts for the '298 and 65 milliwatts for the 'LS298. SN54298 and SN54LS298 are characterized for operation over the full military temperature range of -55°C to 125°C ; SN74298 and SN74LS298 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q _A	Q _B	Q _C	Q _D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

H = high level (steady state)

L = low level (steady state)

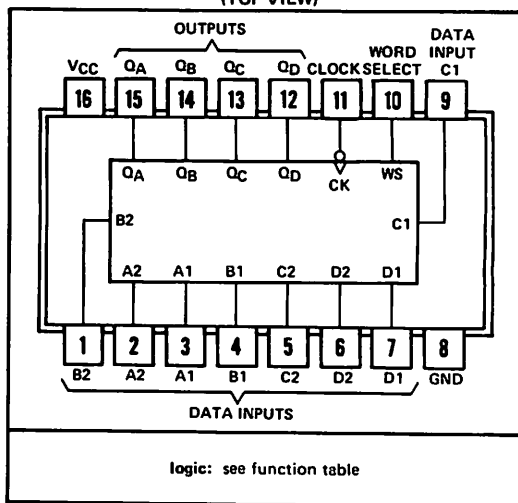
X = irrelevant (any input, including transitions)

↓ = transition from high to low level

a1, a2, etc. = the level of steady-state input at A1, A2, etc.

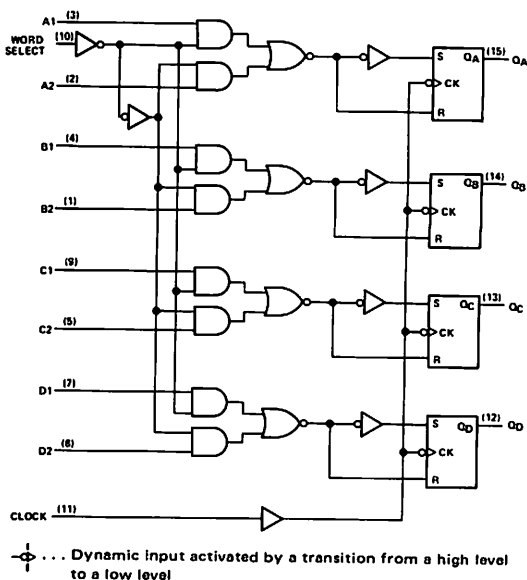
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most-recent ↓ transition of the clock input.

SN54298, SN54LS298 ... J OR W PACKAGE
SN74298, SN74LS298 ... J OR N PACKAGE
(TOP VIEW)



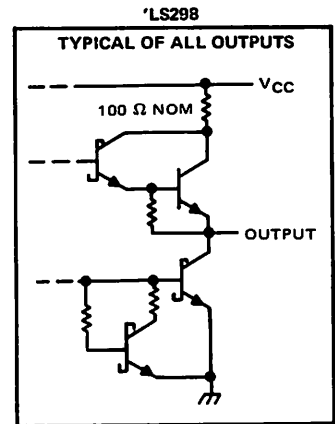
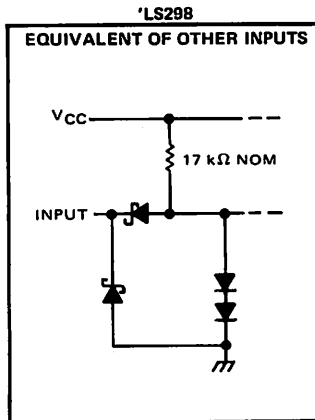
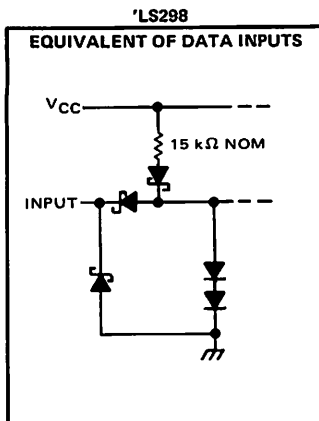
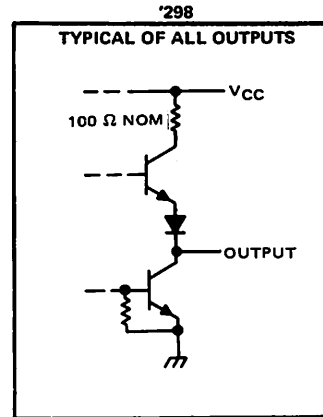
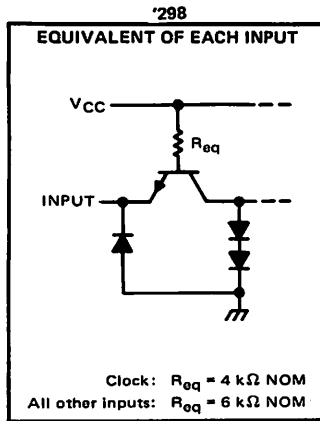
logic: see function table

functional block diagram



TYPES SN54298, SN54LS298, SN74298, SN74LS298 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

schematics of inputs and outputs



TYPES SN54298, SN74298
QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Table with 2 columns: Parameter and Value. Parameters include Supply voltage (VCC), Input voltage, Operating free-air temperature range (SN54298, SN74298), and Storage temperature.

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

Table with 4 columns: Parameter, SN54298 (MIN, NOM, MAX), SN74298 (MIN, NOM, MAX), and UNIT. Parameters include Supply voltage (VCC), High-level output current (IOH), Low-level output current (IOL), Width of clock pulse (tw), Setup time (tsetup), Hold time (thold), and Operating free-air temperature (TA).

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Table with 5 columns: PARAMETER, TEST CONDITIONS†, MIN, TYP‡, MAX, and UNIT. Parameters include Vih, Vil, Vi, Voh, Vol, Ii, Iih, Iil, Ios, and Icc.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at VCC = 5 V, TA = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: With all outputs open and all inputs except clock low, ICC is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

switching characteristics, VCC = 5 V, TA = 25°C

Table with 5 columns: PARAMETER, TEST CONDITIONS, MIN, TYP, MAX, and UNIT. Parameters include tPLH and tPHL.

NOTE 3: Load circuit and waveforms are shown on page S-87.

TYPES SN54LS298, SN74LS298

QUADRUPL 2-INPUT MULTIPLEXERS WITH STORAGE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS298	-55°C to 125°C
SN74LS298	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS298			SN74LS298			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μ A
Low-level output current, I_{OL}				4			8	mA
Width of clock pulse, high or low level, t_W		20			20			ns
Setup time, t_{setup}	Data	15			15			ns
	Word select	25			25			
Hold time, t_{hold}	Data	5			5			ns
	Word select	0			0			
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS298			SN74LS298			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$							
	$I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$I_{OL} = 8 \text{ mA}$				0.35	0.5		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-6		-40	-5		-42	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	13		21	13		21	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Note more than one output should be shorted at a time.

NOTE 2: With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Note 4	18	27		ns
t_{PHL} Propagation delay time, high-to-low-level output		21	32		

NOTE 4: Load circuit and waveforms are shown on page S-88.

TENTATIVE DATA

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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S-299

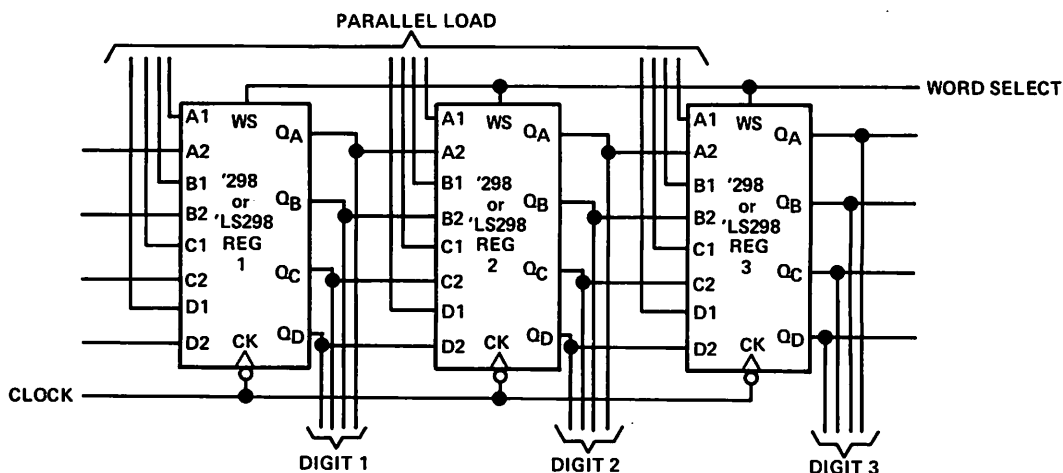
TYPES SN54298, SN54LS298, SN74298, SN74LS298

QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

TYPICAL APPLICATION DATA

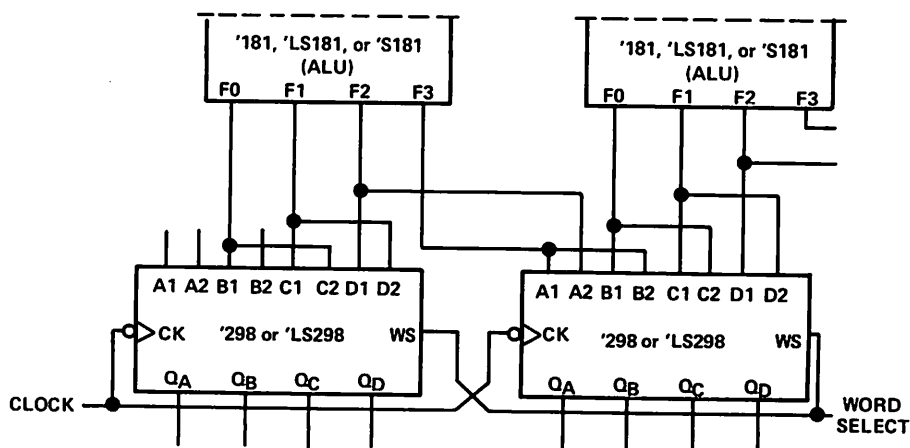
This versatile multiplexer/register can be connected to operate as a shift register that can shift N-places in a single clock pulse.

The following figure illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.



When the word-select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2 and etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered in the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the '298 or 'LS298 is a register that can be designed specifically for supporting multiplier or division operations. The example below is a one place/two-place shift register.



When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALU's) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

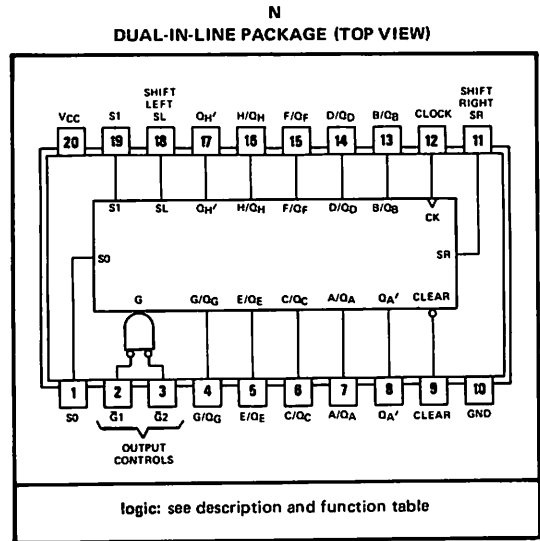
TTL
LSI

TYPE SN74S299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTER

BULLETIN NO. DL-S 7412115, MARCH 1974

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operation:
Hold (Store) Shift Left
Shift Right Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- High Performance:
Access (Read) Time from Clock, Clear, and Read Enable Inputs . . . 12 ns Typical
Guaranteed Shift (Clock) Frequency . . . 50MHz
- Applications:
Stacked or Push-Down Registers,
Buffer Storage, and
Accumulator Registers



description

This Schottky TTL eight-bit universal register features multiplexed inputs/outputs to achieve full eight bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

FUNCTION TABLE

MODE	INPUTS						INPUTS/OUTPUTS								OUTPUTS			
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q _A	B/Q _B	C/Q _C	D/Q _D	E/Q _E	F/Q _F	G/Q _G	H/Q _H	Q _A '	Q _H '
		S1	S0	G ₁ [†]	G ₂ [†]		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}
	H	X	X	L	L	L	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	H	Q _{Gn}
	H	L	H	L	L	↑	X	L	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	L	Q _{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	H	Q _{Bn}	H
	H	H	L	L	L	↑	L	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	L	Q _{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

[†]When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, X = irrelevant (any input, including transitions)
Q_{A0}, Q_{B0} . . . Q_{H0} = the level of the respective internal Q outputs before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn} . . . Q_{Hn} = the level of Q_A, Q_B . . . Q_H, respectively before the most-recent ↑ transition of the clock.
a . . . h = the level of the steady-state input at inputs A through H, respectively, is loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

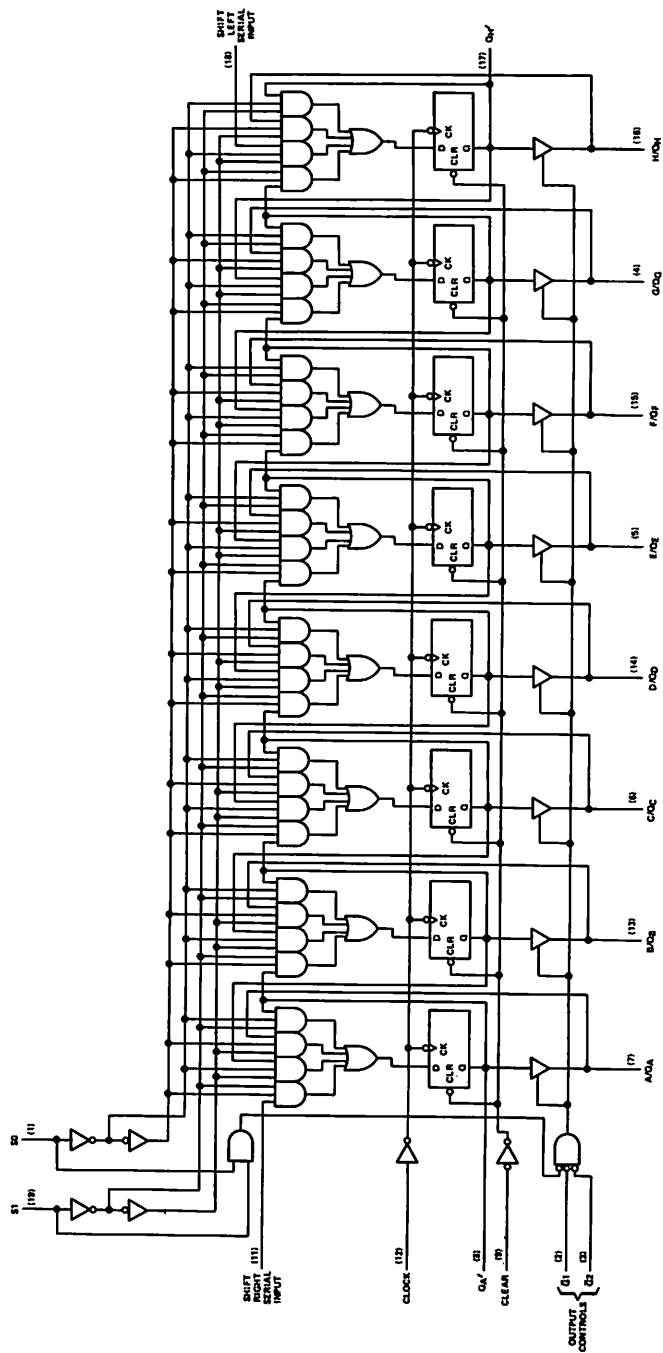
TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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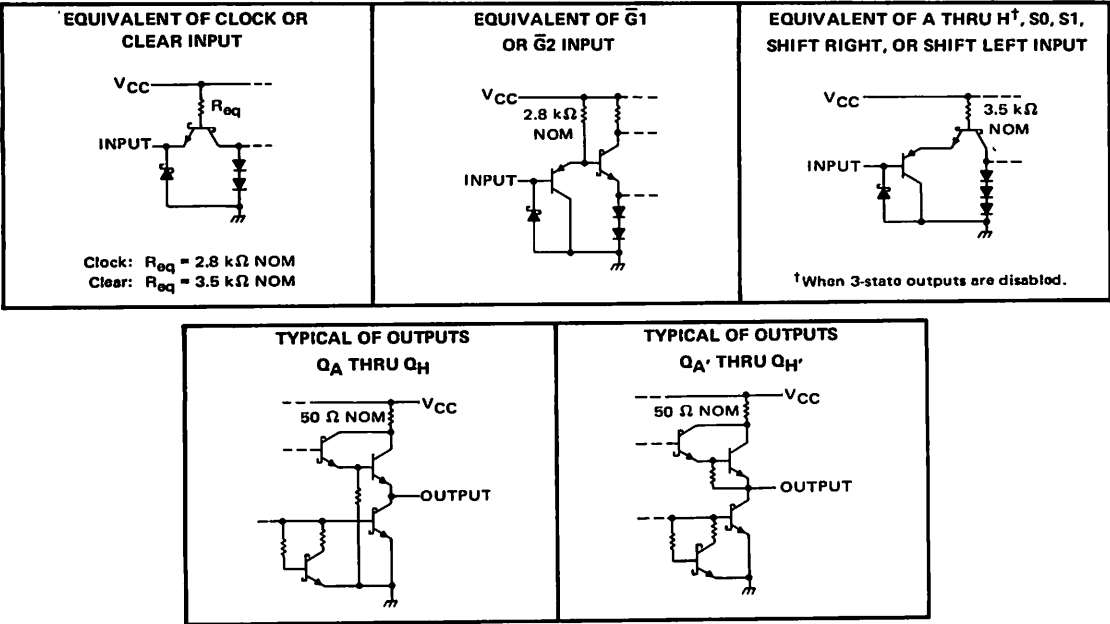
S-301

3



TYPE SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTER

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			-6.5	mA
	Q_A' or Q_H'			-0.5	
Low-level output current, I_{OL}	Q_A thru Q_H			20	mA
	Q_A' or Q_H'			6	
Clock frequency, f_{clock}		0		50	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	10			ns
	Clock low	10			
Setup time, t_{setup}	Select	5†			ns
	High-level data [◊]	5†			
	Low-level data [◊]	5†			
	Clear inactive-state	10†			
Hold time, t_{hold}	Select	10†			ns
	Data [◊]	5†			
Operating free-air temperature, T_A		0		70	°C

[◊]Data includes the two serial inputs and the eight input/output data lines.

TYPE SN74S299
8-BIT UNIVERSAL SHIFT/STORAGE REGISTER

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{IH}	High-level input voltage		2			V
V _{IL}	Low-level input voltage				0.8	V
V _I	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.2	V
V _{OH}	High-level output voltage	Q _A thru Q _H	V _{CC} = MIN, V _{IH} = 2 V,	2.4	3.2	V
		Q _A ' or Q _H '	V _{IL} = 0.8 V, I _{OH} = MAX	2.7	3.4	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = MAX			0.5	V
I _{OZH}	Off-state output current, high-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.4 V		100	μA
I _{OZL}	Off-state output current, low-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.5 V		-250	μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1	mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V			50	μA
I _{IL}	Low-level input current	Clock or clear	V _{CC} = MAX, V _I = 0.5 V		-2	mA
		Any other			-250	μA
I _{OS}	Short-circuit output current §	Q _A thru Q _H	V _{CC} = MAX	-40	-100	mA
		Q _A ' or Q _H '		-20	-100	
I _{CC}	Supply current	V _{CC} = MAX		150	240	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			See Note 2	50	70		ns
t _{PLH}	Clock	Q _A ' or Q _H '	C _L = 15 pF, R _L = 1 kΩ,		15		ns
t _{PHL}			See Note 2		15		
t _{PHL}	Clear	Q _A ' or Q _H '			15		ns
t _{PLH}	Clock	Q _A thru Q _H	C _L = 50 pF, R _L = 280 Ω, See Note 2		15		ns
t _{PHL}					15		
t _{PHL}	Clear	Q _A thru Q _H			15		ns
t _{ZH}	$\bar{G}1, \bar{G}2$	Q _A thru Q _H			10		ns
t _{ZL}					12		
t _{HZ}	$\bar{G}1, \bar{G}2$	Q _A thru Q _H	C _L = 5 pF, R _L = 280 Ω, See Note 2		8		ns
t _{LZ}					8		

¶ f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{ZH} = output enable time to high level

t_{ZL} = output enable time to low level

t_{HZ} = output disable time from high level

t_{LZ} = output disable time from low level

NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. See load circuits and waveforms on page S-87.

TTL
MSI

TYPE SN74351

DUAL DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7412116, MARCH 1974

- Dual 8-Line-to-1-Line Multiplexer That Can Replace Two SN54151, SN74151 Multiplexers in Some Applications
- Four Common Data Lines Permit Simultaneous Interdigitation with Parallel-to-Serial Conversion
- 4-Bit Organization Is Easily Adapted to Handle Binary or BCD
- Three-State Outputs Can Be Connected Directly to System Bus Lines
- Enable Input Controls Impedance Levels of the 12 Data Inputs and Two Outputs

description

The SN74351 comprises two 8-line-to-1-line data selectors/multiplexers with full decoding on one monolithic chip. Symmetrically switching, complementary decode generators minimize decoder skew during changes at the select inputs and ensure that potentially erroneous effects are minimized at the data outputs. Four data inputs are exclusive to each multiplexer and four are common to both. A common enable input is provided which, when high, causes both outputs to assume the high-impedance (off) state and simultaneously diverts the majority of the input current, which reduces the load significantly on the data input drivers. A low logic level at the enable input activates both outputs so that each will assume the complement of the level of the selected input.

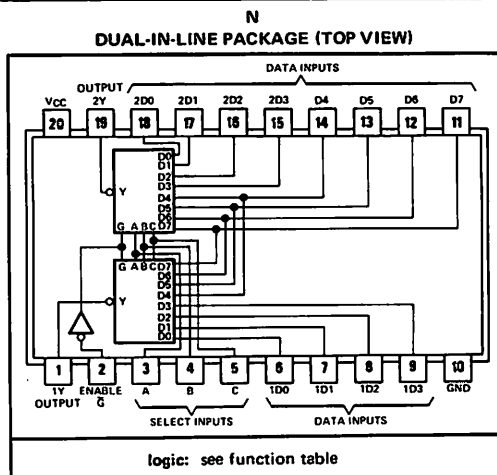
FUNCTION TABLE

INPUTS				OUTPUTS	
ENABLE	SELECT			1Y	2Y
\bar{G}	C	B	A	1Y	2Y
H	X	X	X	Z	Z
L	L	L	L	$\bar{1D0}$	$\bar{2D0}$
L	L	L	H	$\bar{1D1}$	$\bar{2D1}$
L	L	H	L	$\bar{1D2}$	$\bar{2D2}$
L	L	H	H	$\bar{1D3}$	$\bar{2D3}$
L	H	L	L	$\bar{1D4}$	$\bar{2D4}$
L	H	L	H	$\bar{1D5}$	$\bar{2D5}$
L	H	H	L	$\bar{1D6}$	$\bar{2D6}$
L	H	H	H	$\bar{1D7}$	$\bar{2D7}$

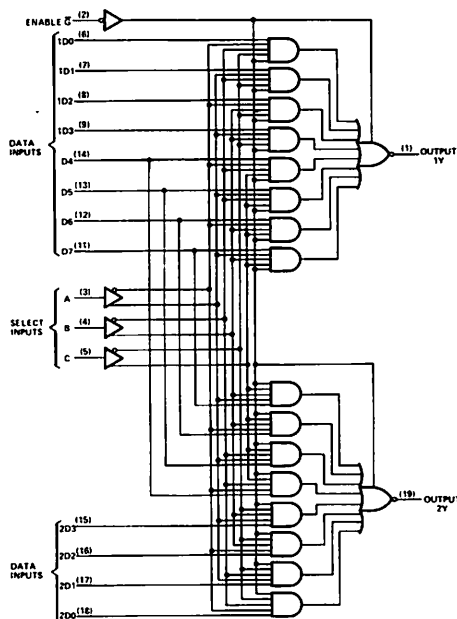
H = high level, L = low level, X = irrelevant

Z = high impedance (off)

$\bar{1D0}, \bar{1D1}, \dots, \bar{1D7}$ = The complement of the level of the respective D input



functional block diagram



TENTATIVE DATA SHEET

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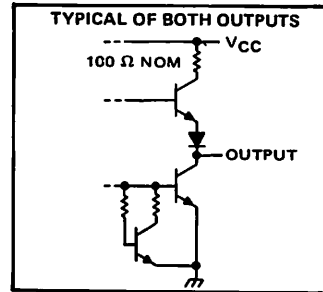
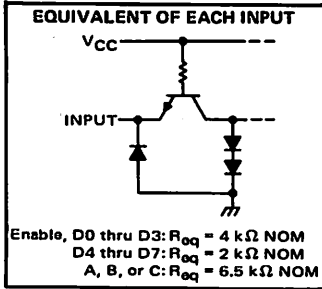
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S-305

TYPE SN74351

DUAL DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			-2	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12\text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{ V}, V_{IL} = 0.8\text{ V}, I_{OH} = -2\text{ mA}$	2.4 3.4				V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{ V}, V_{IL} = 0.8\text{ V}, I_{OL} = 16\text{ mA}$	0.2 0.4				V
I_{OZH}	Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{ V}, V_O = 2.4\text{ V}$				40	μA
I_{OZL}	Off state output current, low level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{ V}, V_O = 0.4\text{ V}$				-40	μA
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{ V}$				1	mA
I_{IH}	High-level input current	Enable, any select, any D0 thru D3	$V_{CC} = \text{MAX}, V_I = 2.4\text{ V}$			40	μA
		D4 thru D7				80	
		Any D				-40	μA
I_{IL}	Low-level input current	Enable, any select, any D0 thru D3	$V_{CC} = \text{MAX}, V_I = 0.4\text{ V}$			-1.6	mA
		D4 thru D7				-3.2	
		Any D	$V_{CC} = \text{MAX}, V_I = 0.5, V_{I(\text{enable})} = 2\text{ V}$			-40	μA
I_{OS}	Short-circuit output current‡	$V_{CC} = \text{MAX}$		-18		-55	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2			44	66	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with the enable input grounded, other inputs and both outputs open.

TYPE SN74351

DUAL DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER †	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A, B, or C	Y	C _L = 50 pF, R _L = 400 Ω, See Note 3		20		ns
t _{PHL}					20		
t _{PLH}	Any D	Y			10		ns
t _{PHL}					10		
t _{ZH}	G̅	Y			13		ns
t _{ZL}					20		
t _{HZ}	G̅	Y	C _L = 5 pF, R _L = 400 Ω, See Note 3		6		ns
t _{LZ}					10		

[†] t_{PLH} \equiv propagation delay time, low-to-high-level output

t_{PHL} \equiv propagation delay time, high-to-low-level output

t_{ZH} \equiv output enable time to high level

t_{ZL} \equiv output enable time to low level

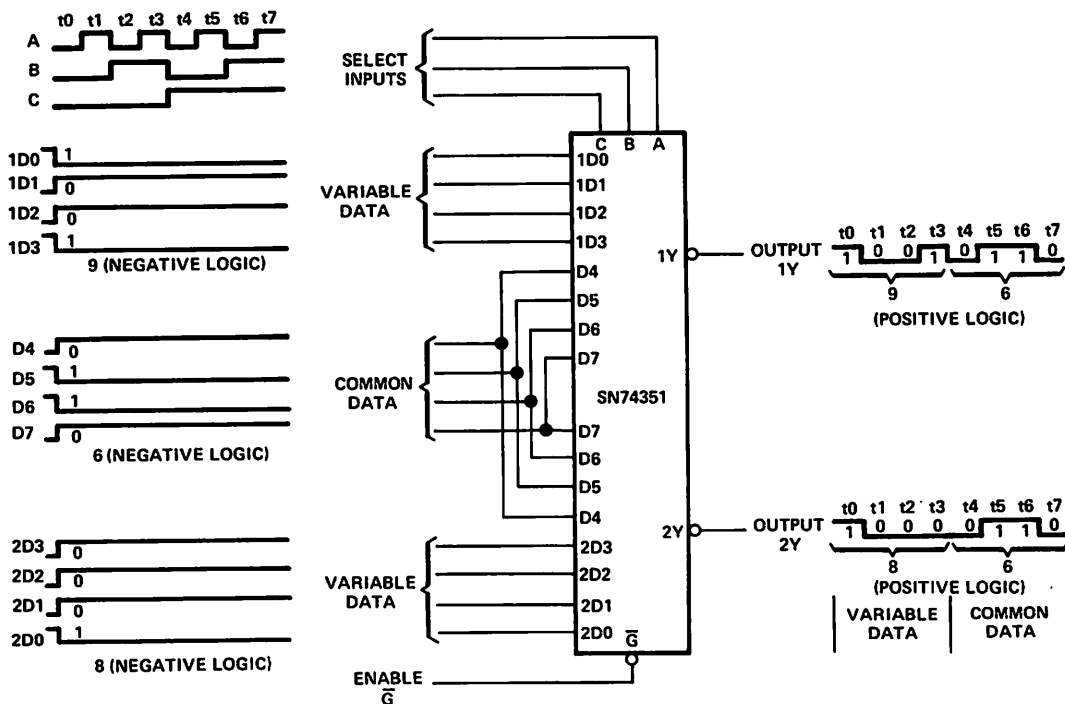
t_{HZ} \equiv output disable time from high level

t_{LZ} \equiv output disable time from low level

NOTE 3: Load circuit and voltage waveforms are shown on page S-87.

TYPICAL APPLICATION DATA

This application illustrates how common data can be interdigitated onto two serial data lines. It is useful for transmitting prefixes, suffixes, addresses, or similar functions.



TYPES SN54S370, SN74S370, SN74S371

2048-BIT READ-ONLY MEMORIES WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7412083, MARCH 1974

- Full Schottky Clamping for High Performance:
Address Access Time . . . 45 ns Typical
Chip Select Time . . . 15 ns Typical
Power Dissipation . . . 0.25 mW/Bit Typical
- 'S370 Is Organized as 512 Words by 4 Bits
- 'S371 Is Organized as 256 Words by 8 Bits and Is in a 20-Pin Package for 0.300-Inch Row Spacing
- Ideal for Microprogramming, Reference Tables, and High-Speed Code Converters
- Bus-Driving 3-State Outputs Are Easily Expandable
- SN54S270/SN74S270 and SN54S271 Are Functionally Equivalent But Have Open-Collector Outputs

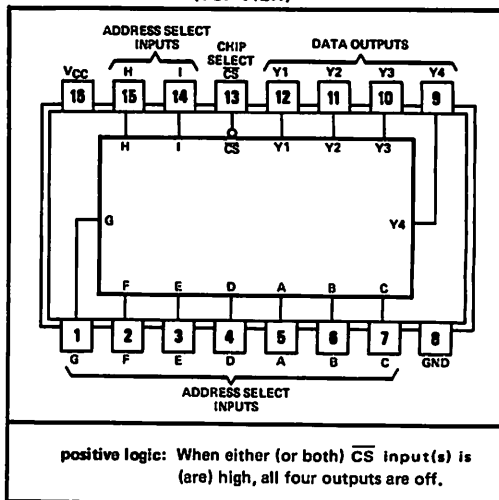
description

The SN54S370, SN74S370, and SN74S371 are 2048-bit monolithic custom-programmed read-only memories. The 'S370 is organized as 512 words of four bits each and the 'S371 is organized as 256 words of eight bits each. These Schottky-clamped, high-speed transistor-transistor-logic (TTL) memory arrays are addressed in straight binary with full on-chip decoding. Overriding chip-select inputs are provided which, when one or more is taken high, will inhibit the function causing all outputs to be in a high-impedance state that neither loads nor drives the bus lines. Data, as specified by the customer, are permanently programmed into the monolithic structure for the 2048 bit locations.

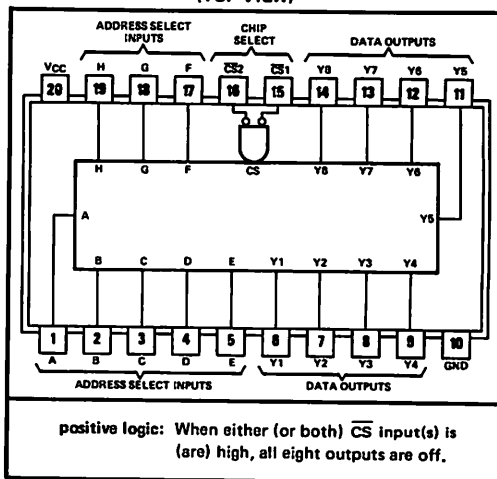
The memory matrix consists of 32 transistors comprising the X plane with each transistor having 64 emitters. Each of the 64 bit lines that comprise the Y plane through the matrix is connected to one emitter from each of the 32 transistors. The address of a word is accomplished through the buffered binary select inputs coincident with low-level voltages at all chip-select inputs. Five binary select inputs are decoded internally in the X plane to select one of the 32 matrix transistors. In the 'S370 the four remaining select inputs are internally decoded in the Y plane to select four of the 64 bit lines. These selected bit lines appear as a four-bit word output. In the 'S371 the three remaining select inputs are internally decoded in the Y plane to select eight of the 64 bit lines. These selected bit lines appear as an eight-bit word output.

The customer can specify the output logic level desired at each of the 2048 bit locations by completing the supplementary ordering data and a set of data cards punched in accordance with the data format shown under ordering instructions. Upon receipt of the order, Texas Instruments will assign a special device number to the device programmed according to the customer's order. The completed device will be marked with the TI special device number. It is important that the customer specify not only the output levels desired at all 2048 bit locations, but also the other information requested.

SN54S370 . . . J PACKAGE
SN74S370 . . . J OR N PACKAGE
(TOP VIEW)



SN74S371 . . . N PACKAGE
(TOP VIEW)



TENTATIVE DATA SHEET

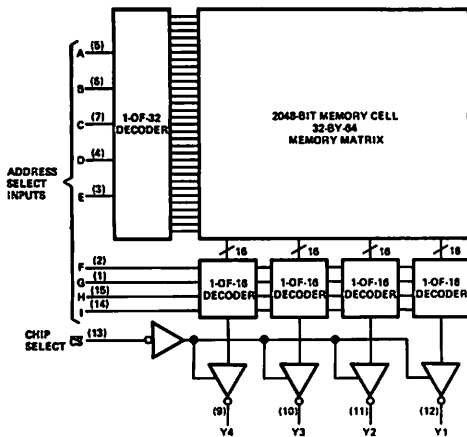
S-308

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TYPES SN54S370, SN74S370, SN74S371 2048-BIT READ-ONLY MEMORIES WITH 3-STATE OUTPUTS

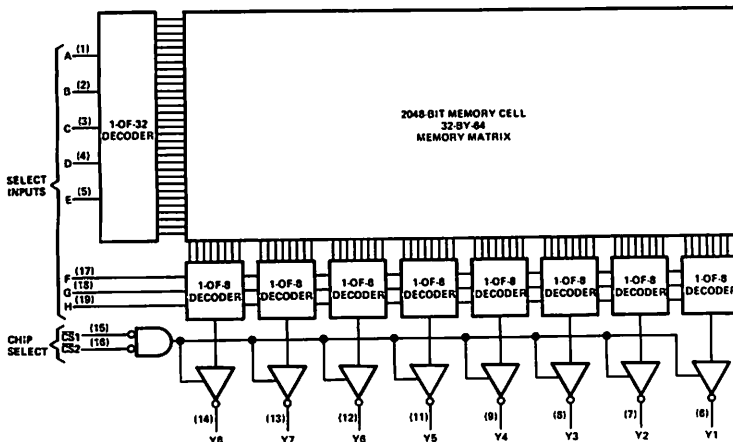
SN54S370/SN74S370 functional block diagram and word selection



WORD-SELECT TABLE	
WORD	INPUTS
	I H G F E D C B A
0	L L L L L L L L L
1	L L L L L L L L H
2	L L L L L L L H L
3	L L L L L L L H H
4	L L L L L L H L L
5	L L L L L L H L H
6	L L L L L L H H L
7	L L L L L L H H H
8	L L L L L H L L L
Words 9 thru 506 omitted	
507	H H H H H H L H H
508	H H H H H H L L L
509	H H H H H H H L L
510	H H H H H H H L H
511	H H H H H H H H H

Word selection is accomplished in a conventional 9-bit positive-logic binary code with the A select input being the least-significant bit progressing alphabetically through the select inputs to I which is the most significant bit.

SN74S371 functional block diagram and word selection



WORD-SELECT TABLE	
WORD	INPUTS
	H G F E D C B A
0	L L L L L L L L
1	L L L L L L L H
2	L L L L L L H L
3	L L L L L L H H
4	L L L L L H L L
5	L L L L L H L H
6	L L L L L H H L
7	L L L L L H H H
8	L L L L L H L L L
Words 9 thru 250 omitted	
251	H H H H H L H H
252	H H H H H L L L
253	H H H H H H L L
254	H H H H H H L H
255	H H H H H H H H

Word selection is accomplished in a conventional 8-bit positive-logic binary code with the A select input being the least-significant bit progressing alphabetically through the select inputs to H which is the most-significant bit.

TYPES SN54S370, SN74S370, SN74S371

2048-BIT READ-ONLY MEMORIES WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54S370	-55°C to 125°C
SN74S370, SN74S371	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S370			SN74S370 SN74S371			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-2			-6.5	mA
Low-level output current, I_{OL}			12			15	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S370			SN74S370 SN74S371			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4			2.4			V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 12 \text{ mA}$			0.5				V
	$I_{OL} = 15 \text{ mA}$						0.5	V
I_{OZ} Off-state (high-impedance state) output current	$V_{CC} = \text{MAX}, V_O = 2.4 \text{ V}, V_{IH} = 2 \text{ V}, V_O = 0.5 \text{ V}$			50			50	µA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			25			25	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-0.25			-0.25	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-30		-100	-30		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		105	155		105	155	mA
C_O Off-state output capacitance	$V_{CC} = 5 \text{ V}, V_O = 5 \text{ V}, f = 1 \text{ MHz}$		6.5			6.5		pF

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

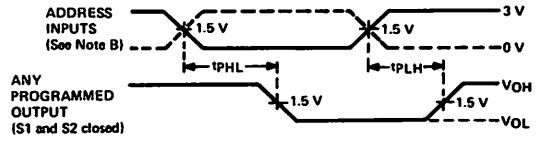
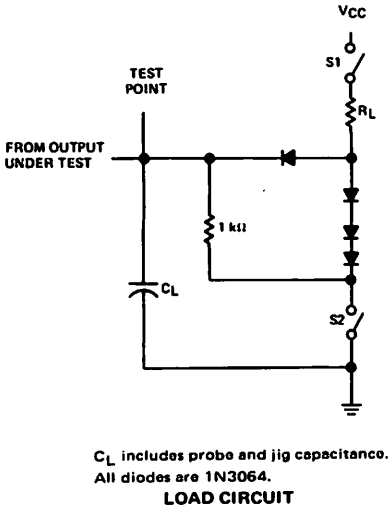
NOTE 2: With outputs open and \overline{CS} input(s) grounded, I_{CC} is measured first by selecting a word that contains the maximum number of programmed high-level outputs; then by selecting a word that contains the maximum number of programmed low-level outputs.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Access times from address select $C_L = 30\text{ pF}$, $R_L = 400\text{ }\Omega$, See Figure 1		45		ns
t_{PLH}	Propagation delay time, high-to-low-level output			45		
t_{ZH}	Output enable time to high level	Access times from chip select See Figure 1		15		ns
t_{ZL}	Output enable time to low level			15		
t_{HZ}	Output disable time from high level	Disable times from chip select $C_L = 5\text{ pF}$, $R_L = 400\text{ }\Omega$, See Figure 1		10		ns
t_{LZ}	Output disable time from low level			10		

TYPES SN54S370, SN74S370, SN74S371 2048-BIT READ-ONLY MEMORIES WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



ACCESS TIME FROM ADDRESS INPUTS
VOLTAGE WAVEFORMS

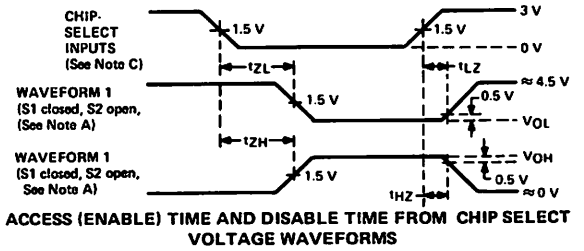
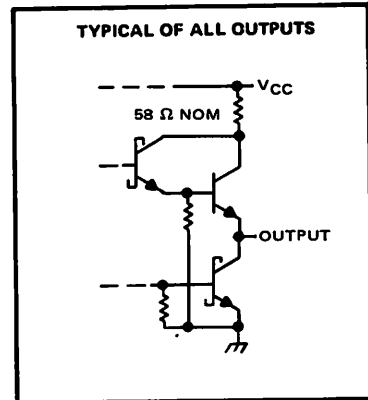
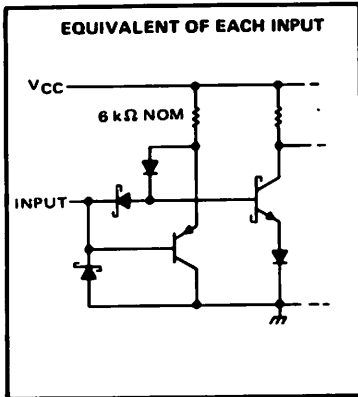


FIGURE 1—SWITCHING TIMES OF 'S370 AND 'S371

- NOTES: A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
B. When measuring delay times from address inputs, the chip-select inputs are low.
C. When measuring delay times from chip-select inputs, the address inputs are steady-state.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r < 2.5\text{ ns}$, $t_f < 2.5\text{ ns}$, $\text{PRR} < 1\text{ MHz}$, and $Z_{out} \approx 50\ \Omega$.

schematics of inputs and outputs



ordering instructions

The ordering instructions for the SN54S270, SN74S270, and SN74S271 also apply for the SN54S370, SN74S370, and SN74S371, respectively. See pages S-258 and S-259.

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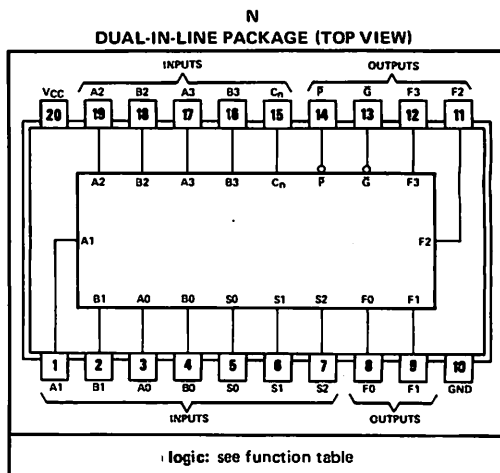
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S-311

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	17, 19, 1, 3	WORD A INPUTS
B3, B2, B1, B0	16, 18, 2, 4	WORD B INPUTS
S2, S1, S0	7, 6, 5	FUNCTION-SELECT INPUTS
C _n	15	CARRY INPUT FOR ADDITION, INVERTED CARRY INPUT FOR SUBTRACTION
F3, F2, F1, F0	12, 11, 9, 8	FUNCTION OUTPUTS
\bar{P}	14	INVERTED CARRY PROPAGATE OUTPUT
\bar{G}	13	INVERTED CARRY GENERATE OUTPUT
V _{CC}	20	SUPPLY VOLTAGE
GND	10	GROUND



- A Fully Parallel 4-Bit ALU in 20-Pin Package for 0.300-Inch Row Spacing
- Ideally Suited for High-Density Economical Processors
- Parallel Inputs and Outputs and Full Look-Ahead Provide System Flexibility
- Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:
 - A Minus B
 - B Minus A
 - A Plus B
 - and Five Other Functions
- Schottky-Clamped for High Performance
 - 16-Bit Add Time . . . 29 ns Typ Using Look-Ahead
 - 32-Bit Add Time . . . 34 ns Typ Using Look-Ahead

FUNCTION TABLE

SELECTION	ARITHMETIC/LOGIC		
S2	S1	S0	OPERATION
L	L	L	CLEAR
L	L	H	B MINUS A
L	H	L	A MINUS B
L	H	H	A PLUS B
H	L	L	A + B
H	L	H	A + B
H	H	L	AB
H	H	H	PRESET

H = high level, L = low level

description

The SN74S381 is a Schottky TTL arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. These operations are selected by the three function-select lines (S0, S1, S2). A full carry look-ahead circuit is provided for fast, simultaneous carry generation by means of two cascade outputs (\bar{P} and \bar{G}) for the four bits in the package. The method of cascading SN54182/SN74182 or SN54S182/SN74S182 look-ahead carry generators with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the '182 and 'S182. The typical addition times shown above illustrate the short delay time required for addition of longer words when full look-ahead is employed. The exclusive-OR, AND, or OR function of two Boolean variables is provided without the use of external circuitry. Also, the outputs can be either cleared (low) or preset (high) as desired.

TENTATIVE DATA SHEET

S-312

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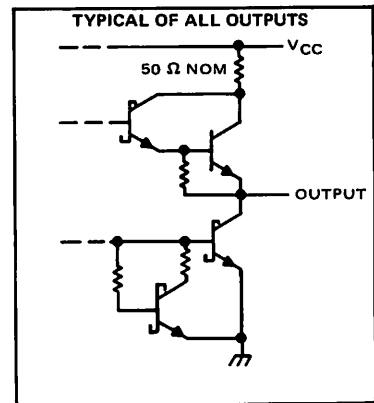
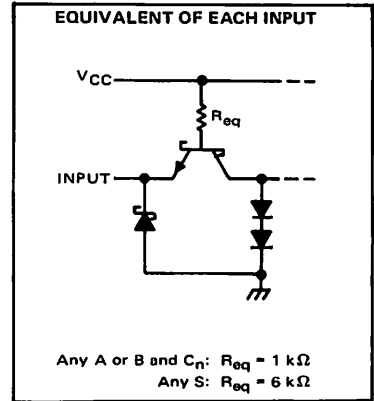
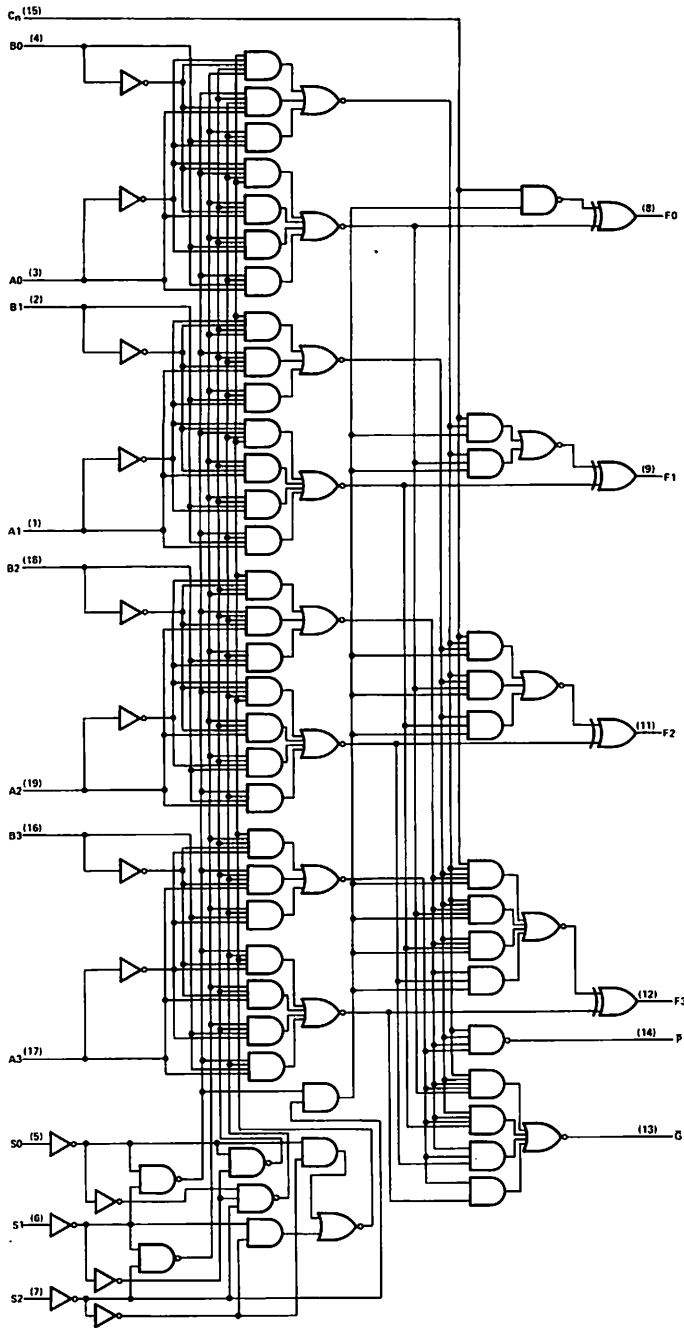
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TYPE SN74S381

ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

functional block diagram and schematics of inputs and outputs



3

TYPE SN74S381
ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (See Note 2)	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage free-air temperature range	-65°C to 150°C

- NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each A input in conjunction with its respective B input; for example A0 with B0, etc.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			-1	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	Any S input			50	μA
		All others			200	
I_{IL}	Low-level input current	Any S input			-2	mA
		All others			-6	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$		105	160	mA

- †For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.
§Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

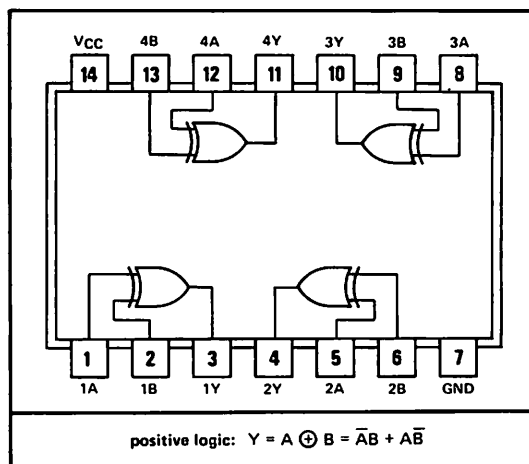
PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
^t PLH	C _n	Any F	C _L = 15 pF, R _L = 280 Ω, See Note 3	11		ns	
^t PHL				11			
^t PLH	Any A or B	\overline{G}		13		ns	
^t PHL				13			
^t PLH	Any A or B	\overline{P}		11		ns	
^t PHL				11			
^t PLH	A _i or B _i	F _i		20		ns	
^t PHL				20			
^t PLH	Any S	Any		28		ns	
^t PHL				28			

- ¶ t_{PLH} = propagation delay time, low-to-high-level output
¶ t_{PHL} = propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page S-87.

TYPES SN54LS386, SN74LS386 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

BULLETIN NO. DL-S 7412118, MARCH 1974

SN54LS386 . . . J OR W PACKAGE
SN74LS386 . . . J OR N PACKAGE
(TOP VIEW)



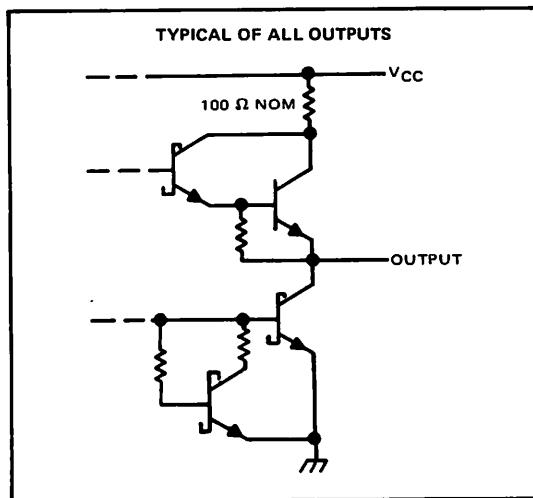
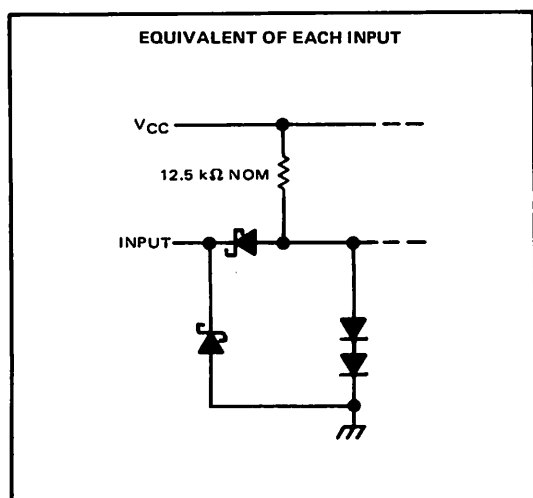
- Electrically Identical to SN54LS86/SN74LS86
- Mechanically Identical to SN54L86/SN74L86
- Total Average Propagation Delay Times . . . 10 ns
- Typical Total Power Dissipation . . . 30.5 mW

**FUNCTION TABLE
(EACH GATE)**

INPUTS		OUTPUT
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

H = high level
L = low level

schematics of inputs and outputs



TYPES SN54LS386, SN74LS386
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS386	−55°C to 125°C
SN74LS386	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS386			SN74LS386			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS386			SN74LS386			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			−1.5			−1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL} \text{ max}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL} \text{ max}$, $I_{OL} = \text{MAX}$		0.25	0.4		0.35	0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.2			0.2	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			−0.6			−0.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	−6		−40	−5		−42	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		6.1	10		6.1	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

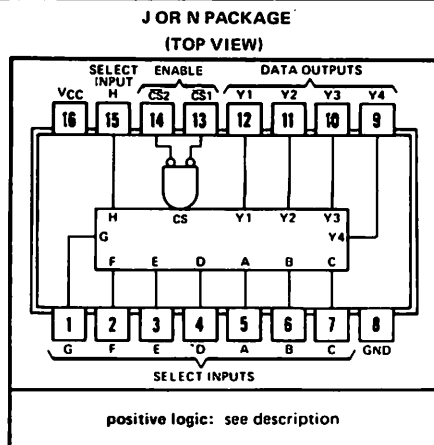
PARAMETER†	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Other input low	C _L = 15 pF, R _L = 2 kΩ, See Note 3	10	17	ns	
t _{PHL}				10	17		
t _{PLH}	A or B	Other input high	See Note 3	10	17	ns	
t _{PHL}				10	17		

¶ t_{PLH} \equiv propagation delay time, low-to-high-level output

t_{PHL} \equiv propagation delay time, high-to-low-level output

NOTE 3: Load circuit and voltage waveforms are shown on page S-88.

- Provides the Versatility of Custom Designs Virtually "Off the Shelf"
- Applications Include:
 - Microprogramming
 - Look-up Tables for any Fixed Program
 - Parallel Code Converters
 - Sequence, Routine, and Subroutine Generators
 - Random-Logic Function Generator
- Schottky-Clamped for High Performance:
 - Chip-Select Access Time . . . 15 ns Typ
 - Address Access Time . . . 40 ns Typ
- Interchangeable with Most Other 256 Word by 4 Bit TTL PROMs/ROMs
- Open-Collector Outputs for Easy Word Expansion
- SN74S287 Is Functionally Equivalent but Has Bus-Driving, 3-State Outputs
- Fully Decoded, Low-Current P-N-P Inputs
- Fully Compatible with Most TTL and Other Saturated Low-Level Logic Families



description

The SN74S387 is a field-programmable, 1024-bit, read-only memory organized as 256 words of four bits each. This monolithic, high-speed, Schottky-clamped TTL memory array is addressed in eight-bit binary with full on-chip decoding. Two overriding chip-select inputs are provided which, when either one or both are high, cause all four outputs to be high (off). This memory features p-n-p input transistors, which reduce the low-level-input-current requirement to a maximum of -0.25 milliamperes, only one-eighth that of a Series 74S standard load. The organization is expandable with no additional output buffering, as shown in Table 1 below.

The address of a four-bit word is accomplished through the buffered binary select inputs in coincidence with a low level at both chip-select inputs. Where multiple 'S387 devices are used in a memory system, the chip-select inputs allow easy decoding of additional address bits.

Data can be electronically programmed, as desired, at any of the 1024 bit locations in accordance with the programming procedure specified. Prior to programming, the memory contains a high-logic-level output condition at all bit locations. The programming procedure open-circuits metal links which results in a low-logic-level output at the selected locations. The procedure is irreversible; once altered, the output for that bit is permanently programmed to provide a low logic level. Outputs never having been altered may later be programmed to supply a low-level output. Operation of the device within the recommended operating conditions will not alter the memory content.

The programmable 'S387 can be used to replace the SN74187 as they are functionally and mechanically identical.

TABLE 1
WORD CAPACITY vs 74S LOADS

SERIES 74S LOADS	MIN R_L (Ω)	MAX NO WIRE-ANDS†	MAX NO OF WORDS
1	450	114	29 184
2	563	90	23 040
3	750	66	16 996
4	1125	42	10 752
5	2250	18	4 608

†Total number of outputs connected to each common bus

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPE SN74S387

1024-BIT PROGRAMMABLE READ-ONLY MEMORY

step-by-step programming procedure

1. Apply steady-state supply voltage ($V_{CC} = 5$ volts) and address the word to be programmed. See recommended conditions for programming on the following page.
2. Verify that the bit location needs to be programmed. (With the load circuit of Figure A, an unprogrammed output will be at 2 volts or greater; a programmed output will be at 0.8 volts or less.) If a bit is already programmed, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to both chip-select inputs.
4. Only one bit location is programmed at a time. Apply the load circuit of Figure A to the outputs not being programmed; then, ground the output to be programmed as a low logic level.
5. Ramp V_{CC} to 10.5 volts nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to both chip-select inputs. This should occur between 10 microseconds and 1 millisecond after V_{CC} has reached its 10.5-volt level. See programming sequence of Figure B.
7. After the X program pulse time (1 millisecond) is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within 10 microseconds to 1 millisecond after the chip-select inputs reach a high logic level, V_{CC} should be ramped down to 5 volts at which level verification can be accomplished.
9. The chip-select inputs may be taken to a low logic level (to permit program verification) 10 microseconds or more after V_{CC} reaches its steady-state value of 5 volts.
10. At a Y pulse duty cycle of 10% or less, repeat steps 1 through 8 for each output where a bit at this address is desired to be programmed.

NOTES: A) V_{CC} should be removed between program pulses to reduce total average power dissipation and resultant chip temperatures. See Figure B.

B) When verification indicates that a bit did not program (output is 2 volts or greater), repeat steps 3 through 9. If the bit did not program after the second application of a 1 millisecond X pulse, repeat steps 3 through 9 using an X pulse time of 50 to 75 milliseconds. Regardless of the X duration, the total average pulse time of Y should be no more than 10% of the programming cycle.

C) The circuit shown in Figure A, or equivalent, is used to limit voltage to 6 volts or less for outputs not being programmed.

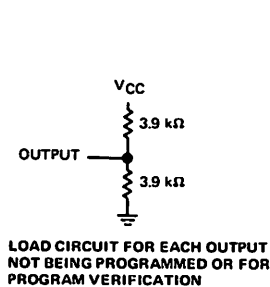
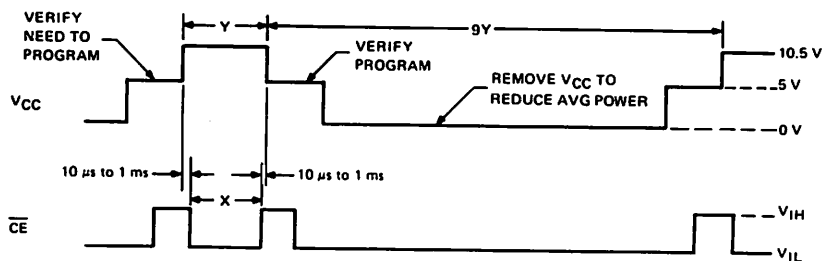


FIGURE A



VOLTAGE WAVEFORMS FOR PROGRAMMING

FIGURE B

TYPE SN74S387

1024-BIT PROGRAMMABLE READ-ONLY MEMORY

recommended conditions for programming

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 1)	Steady state	4.75	5	5.25	V
	Program pulse	10	10.5	11†	
Input voltage	High level	2.4		5	V
	Low level	0		0.5	
Output conditions for programming	To a high logic level	See Figure A			
	To a low logic level		0	-0.8	V
Duration of programming pulse X (see Figure B)		1		75	ms

NOTE 1: All voltage values are with respect to network ground terminal.

†Absolute maximum rating

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 2)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. This rating applies at all times except during programming.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5	V
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}$			50	μA
	$V_{OH} = 2.4 \text{ V}$ $V_{OH} = 5.5 \text{ V}$			250	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$			0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			25	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-250	μA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 3}$		110	150	mA

NOTE 3: I_{CC} is measured with outputs open and both \overline{CS} inputs grounded.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

TYPES SN54390, SN54393, SN74390, SN74393
DUAL 4-BIT DECADE AND BINARY COUNTERS

FUNCTION TABLES

'390
BCD COUNT SEQUENCE
(EACH COUNTER)
(See Note A)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'390
BI-QUINARY (5-2)
(EACH COUNTER)
(See Note B)

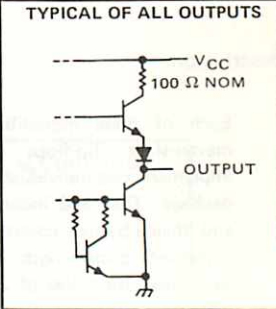
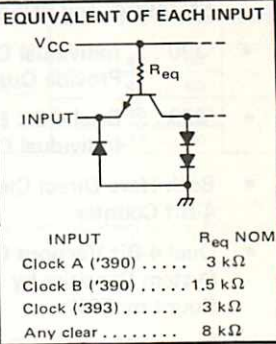
COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'393
COUNT SEQUENCE
(EACH COUNTER)

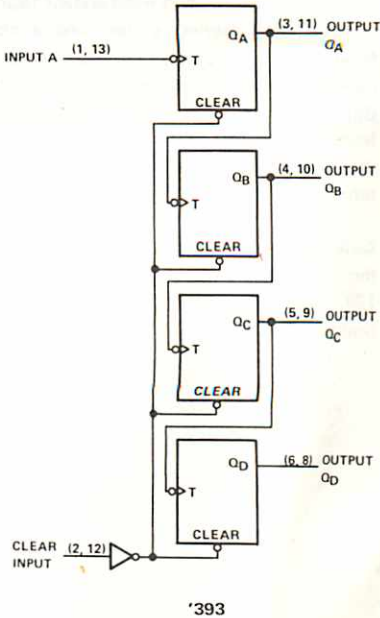
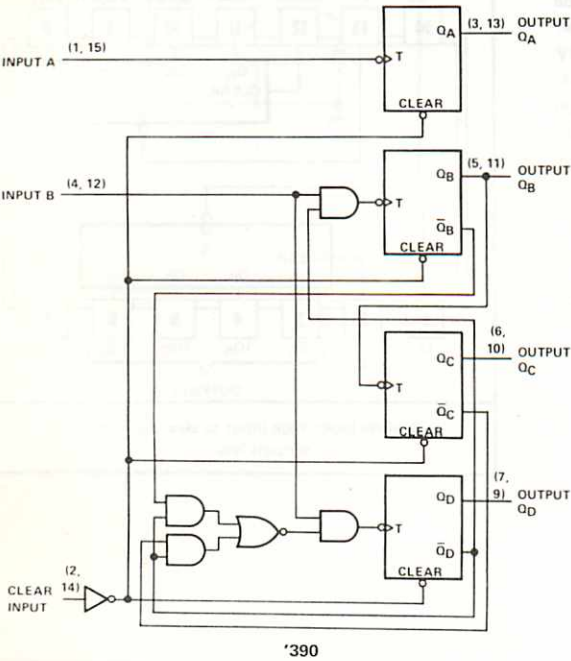
COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. H = high level, L = low level.

schematics of inputs and outputs



functional block diagrams



TYPES SN54390, SN54393, SN74390, SN74393

DUAL 4-BIT DECADE AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54390, SN54393	-55°C to 125°C
SN74390, SN74393	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54390 SN54393			SN74390 SN74393			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-800			-800			μ A
Low-level output current, I_{OL}		16			16			mA
Count frequency, f_{count}	A input	0		25	0		25	MHz
	B input	0		20	0		20	
Pulse width, t_w	A input high or low	20			20			ns
	B input high or low	25			25			
	Clear high	20			20			
Clear inactive-state setup time, t_{setup}		25			25			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

† The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'390			'393			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}^\S$			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1			1	mA
I_{IH}	High-level input current	Clear				40			40	μ A
		A	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			80			80	
		B				120				
I_{IL}	Low-level input current	Clear				-1			-1	mA
		A	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-3.2			-3.2	
		B				-4.8				
I_{OS}	Short-circuit output current §	$V_{CC} = \text{MAX}$	SN54' SN74'	-20	-57	-20	-57			mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 2		42	69	38	64			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ The Q_A outputs of the '390 are tested at $I_{OL} = 16 \text{ mA}$ plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

TYPES SN54390, SN54393, SN74390, SN74393
DUAL 4-BIT DECADE AND BINARY COUNTERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'390			'393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{\max}	A	Q_A	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, See Note 3 and Figure 1	25	35		25	35		MHz
	B	Q_B		20	30					
t_{PLH}	A	Q_A		12	20		12	20		ns
t_{PHL}		Q_A		13	20		13	20		
t_{PLH}	A	Q_C of '390		37	60		40	60		ns
t_{PHL}		Q_D of '393		39	60		40	60		
t_{PLH}	B	Q_B		13	21					ns
t_{PHL}		Q_B		14	21					
t_{PLH}	B	Q_C		24	39					ns
t_{PHL}		Q_C		26	39					
t_{PLH}	B	Q_D		13	21					ns
t_{PHL}		Q_D		14	21					
t_{PHL}	Clear	Any		24	39		24	39		ns

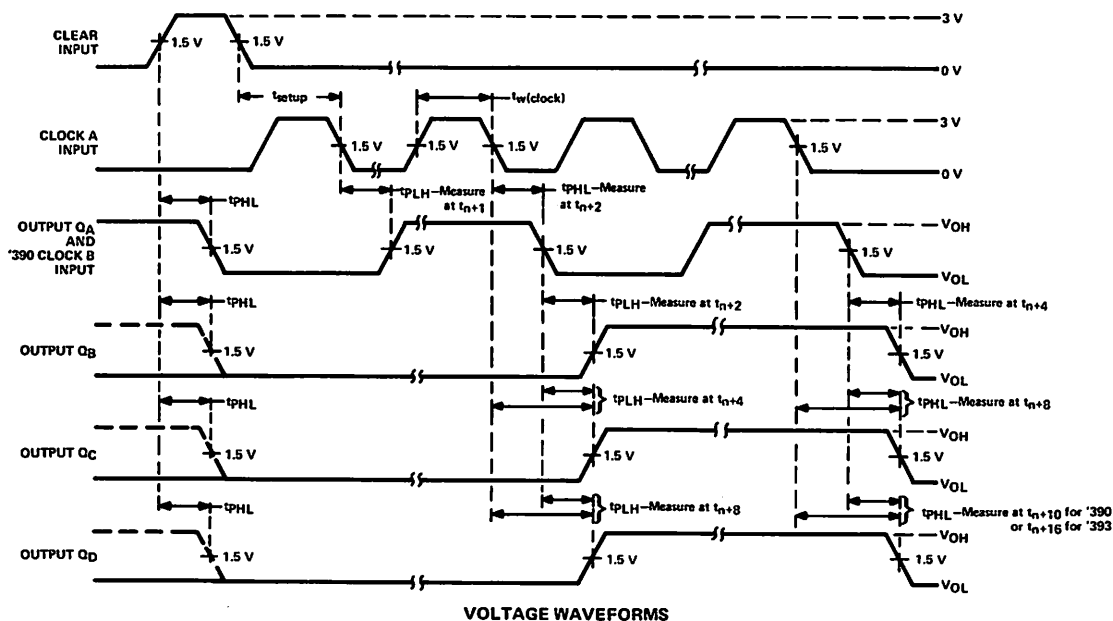
[†] f_{\max} = maximum count frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuit is shown on page S-87.

PARAMETER MEASUREMENT INFORMATION



NOTE A: Input pulses are supplied by a generator having the following characteristics $t_r \leq 5\text{ ns}$, $t_f \leq 5\text{ ns}$, $\text{PRR} = 1\text{ MHz}$, duty cycle = 50%, $Z_{\text{out}} \approx 50\text{ ohms}$.

FIGURE 1

TYPES SN54LS395, SN74LS395

4-BIT CASCADABLE SHIFT REGISTERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7412114, MARCH 1974

- Three-State, 4 Bit, Cascadable, Parallel-In, Parallel-Out Registers
- Schottky-Diode-Clamped Transistors
- Low Power Dissipation . . . 75 mW Typical (Enabled)
- Applications:
 - N-Bit Serial-To-Parallel Converter
 - N-Bit Parallel-To-Serial Converter
 - N-Bit Storage Register

description

These 4-bit registers feature parallel inputs, parallel outputs, and clock, serial, load/shift, output control and direct overriding clear inputs.

Shifting is accomplished when the load/shift control is low. Parallel loading is accomplished by applying the four bits of data and taking the load/shift control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

When the output control is low, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected. During the high-impedance mode, the output at Q_D' is still available for cascading.

The SN54LS395 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74LS395 is characterized for operation from 0°C to 70°C .

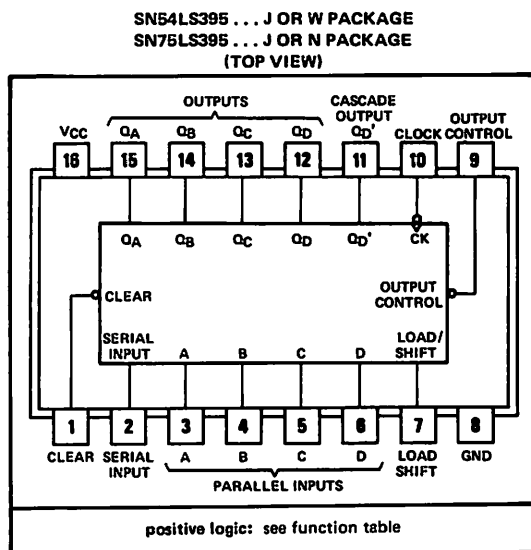
FUNCTION TABLE

INPUTS					3-STATE OUTPUTS				CASCADE
CLEAR	LOAD/SHIFT CONTROL	CLOCK	SERIAL	PARALLEL	Q _A	Q _B	Q _C	Q _D	OUTPUT Q _D '
				A B C D					
L	X	X	X	X X X X	L	L	L	L	L
H	H	H	X	X X X X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{D0}
H	H	↓	X	a b c d	a	b	c	d	d
H	L	H	X	X X X X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{D0}
H	L	↓	H	X X X X	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}
H	L	↓	L	X X X X	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}

When the output control is high, the 3-state outputs are disabled to the high-impedance state; however, sequential operation of the registers and the output at Q_D' are not affected.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.



TYPES SN54LS395, SN74LS395

4-BIT CASCADABLE SHIFT REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS395	−55°C to 125°C
SN74LS395	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS395			SN74LS395			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_w(\text{clock})$	25			25			ns
Setup time, high-level or low-level data, t_{setup}	20			20			ns
Hold time, high-level or low-level data, t_{hold}	10			10			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS395		SN74LS395		UNIT	
				MIN	TYP‡	MAX	MIN		TYP‡
V _{IH} High-level input voltage				2			2	V	
V _{IL} Low-level input voltage						0.7		0.8	V
V _I Input clamp voltage	V _{CC} = MIN, I _I = −18 mA					−1.5		−1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX			2.4	3.4		2.4	3.1	V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I _{OL} = 8 mA					0.35	0.5	
I _{OZH} Off-state output current, high-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V					20		20	μA
I _{OZL} Off-state output current, low-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V					−20		−20	μA
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V					0.1		0.1	mA
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.7 V					20		20	μA
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V					−0.4		−0.4	mA
I _{OS} Short-circuit output current §	V _{CC} = MAX			−6	−40		−5	−42	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 2	Condition A		18	29		18	29	mA
		Condition B		15	25		15	25	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with the outputs open, the serial input and mode control at 4.5 V, and the data inputs grounded under the following conditions:

- Output control at 4.5 V and a momentary 3 V, then ground, applied to clock input.
- Output control and clock input grounded.

TYPES SN54LS395, SN74LS395

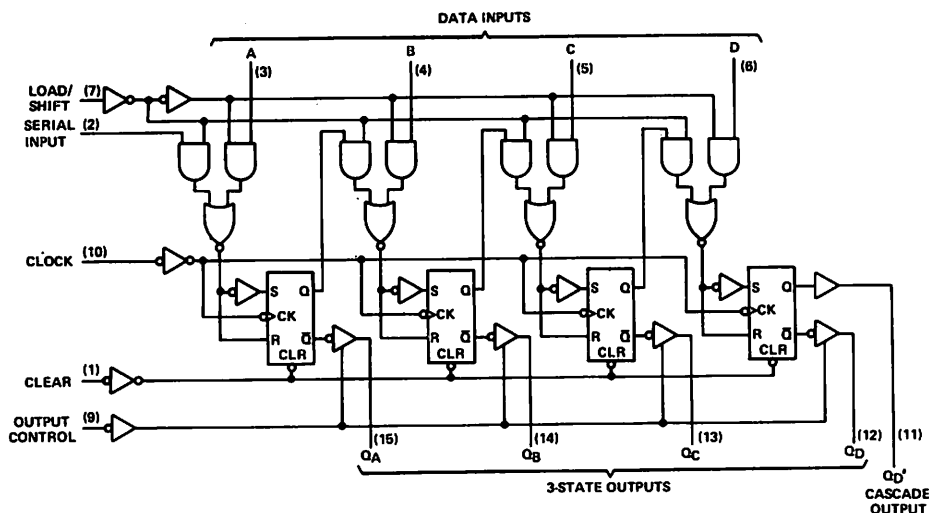
4-BIT CASCADABLE SHIFT REGISTERS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$

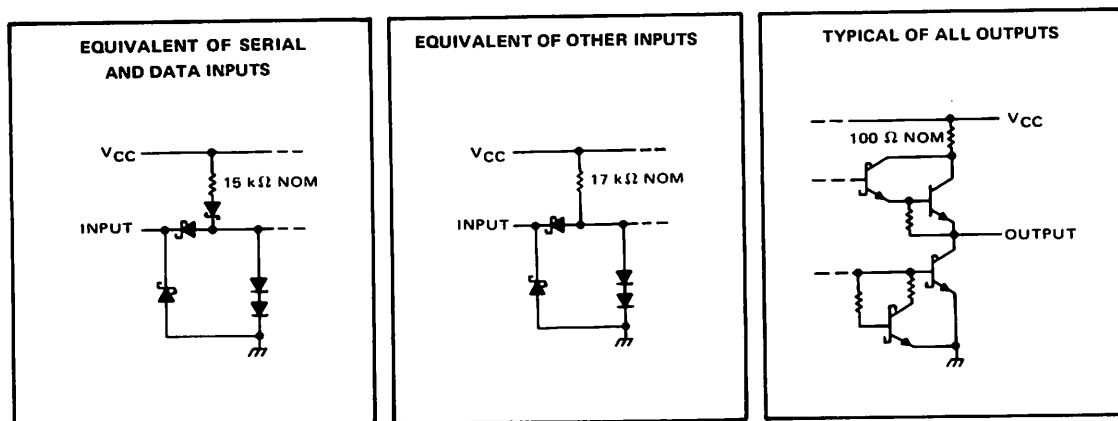
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{\max} Maximum clock frequency	$C_L = 15\text{ pF}$, See Note 3	25	35		MHz
t_{PLH} Propagation delay time, low-to-high-level output			18	27	ns
t_{PHL} Propagation delay time, high-to-low-level output			21	32	ns
t_{ZH} Output enable time to high level			15	25	ns
t_{ZL} Output enable time to low level			20	30	ns
t_{HZ} Output disable time from high level	$C_L = 5\text{ pF}$, See Note 3		30	50	ns
t_{LZ} Output disable time from low level			30	50	ns

NOTE 3: Load circuit and voltage waveforms are shown on page S-88.

functional block diagram



schematics of inputs and outputs



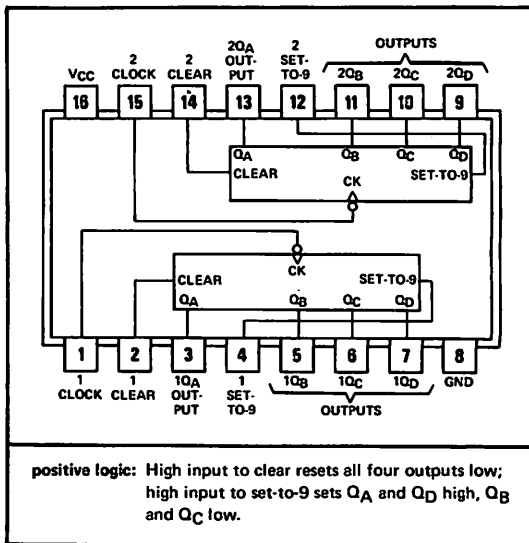
**TTL
MSI**

TYPES SN54490, SN74490 DUAL 4-BIT DECADE COUNTERS

BULLETIN NO. DL-S 7412089, JANUARY 1974

- Dual Version of Popular SN5490A, SN7490A Counters
- Direct Clear and Set-to-9 Inputs for Each 4-Bit Counter
- Individual Clock for Each 4-Bit Counter
- Dual Counters Can Significantly Improve System Densities as Package Count Can Be Reduced by 50%
- Maximum Count Frequency . . . 35 MHz Typical
- Active Pull-Down Provides Square Transfer Characteristics
- Buffered Outputs Reduce Possibility of Collector Commutation

SN54490 . . . J OR W PACKAGE
SN74490 . . . J OR N PACKAGE
(TOP VIEW)



description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual 4-bit decade counters in a single package. Each decade counter has individual clock, clear, and set-to-9 inputs. BCD count sequences of any length up to divide-by-100 may be implemented with a single SN54490 or SN74490. Buffering on each output is provided to ensure that susceptibility to collector commutation is reduced significantly. All inputs are diode-clamped to reduce the effects of line ringing.

The SN54490 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74490 is characterized for use in industrial systems operating from 0°C to 70°C .

BCD COUNT SEQUENCE
(EACH COUNTER)

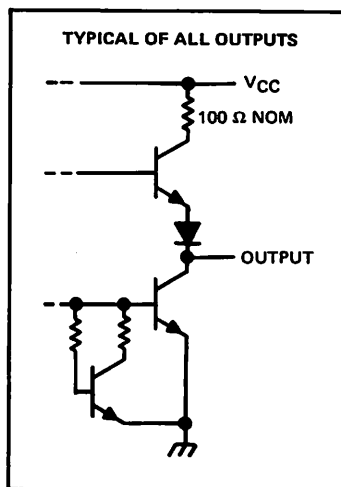
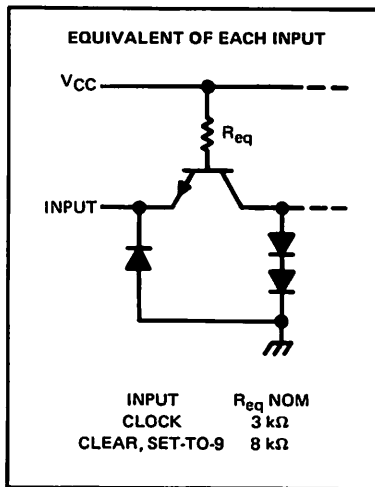
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

CLEAR/SET-TO-9
FUNCTION TABLE
(EACH COUNTER)

INPUTS		OUTPUTS			
CLEAR	SET-TO-9	Q_A	Q_B	Q_C	Q_D
H	L	L	L	L	L
L	H	H	L	L	H
L	L	COUNT			

H = high level, L = low level

schematics of inputs and outputs



TENTATIVE DATA SHEET

S-328

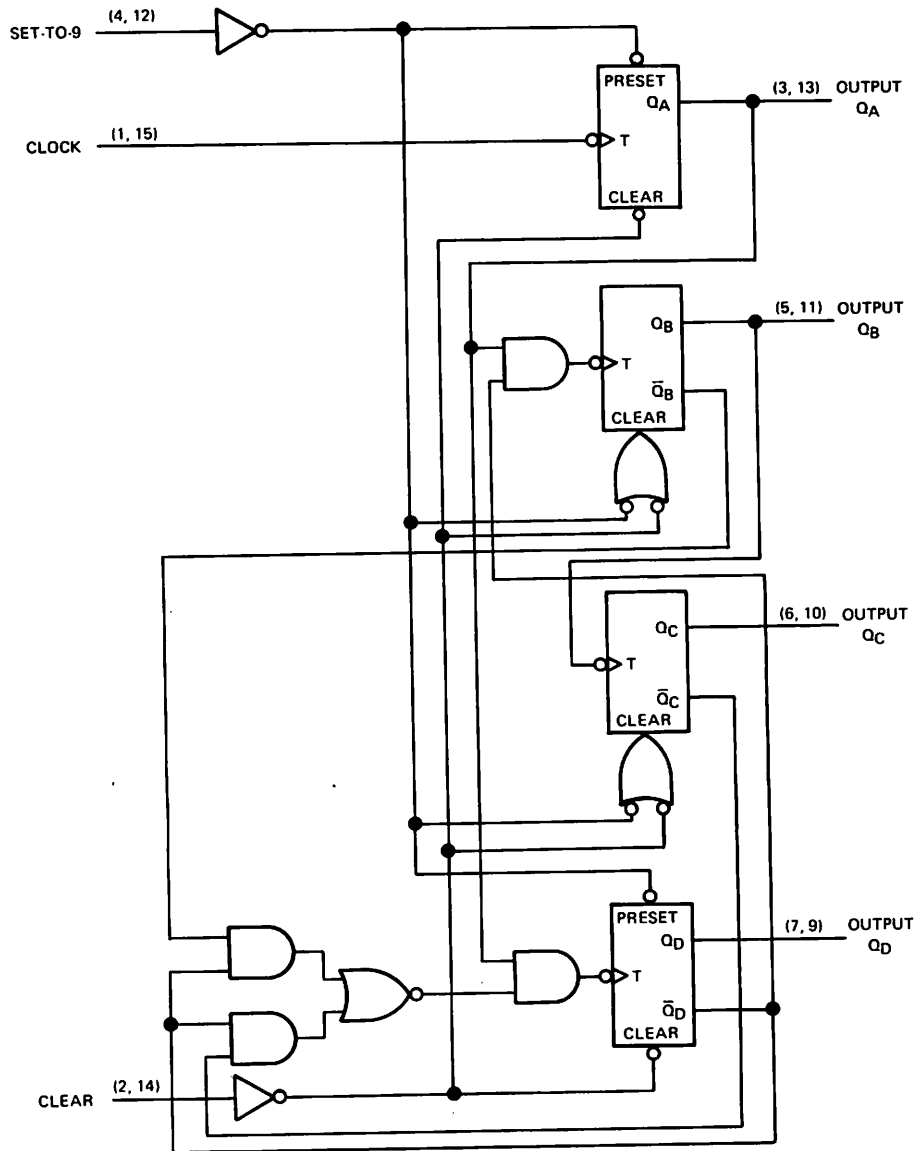
This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES SN54490, SN74490

DUAL 4-BIT DECADE COUNTERS

functional block diagram (each counter)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54490	-55°C to 125°C
SN74490	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54490, SN74490
DUAL 4-BIT DECADE COUNTERS

recommended operating conditions

		SN54490			SN74490			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-800			-800			μ A
Low-level output current, I_{OL}		16			16			mA
Count frequency, f_{count}		0 25			0 25			MHz
Pulse width, t_w	Clock	20			20			ns
	Clear or set-to-9	20			20			
Clear or set-to-9 inactive-state setup time, t_{setup}		25			25			ns
Operating free-air temperature, T_A		-55 125			0 70			$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	Clear, set-to-9			40	μ A
		Clock			80	
I_{IL}	Low-level input current	Clear, set-to-9			-1	mA
		Clock			-3.2	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	SN54490 -20 SN74490 -18		-57 -57	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		45	70	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{\max}	Clock	Q_A	$C_L = 15 \text{ pF},$ $R_L = 400 \Omega,$ See Figure 1		25	35		MHz
t_{PLH}	Clock	Q_A				12	20	ns
t_{PHL}						13	20	
t_{PLH}	Clock	Q_B, Q_D				24	39	ns
t_{PHL}						26	39	
t_{PLH}	Clock	Q_C				32	54	ns
t_{PHL}						36	54	
t_{PHL}	Clear	Any Q				24	39	ns
t_{PLH}	Set-to-9	Q_A, Q_D				24	39	ns
t_{PHL}		Q_B, Q_C				20	36	

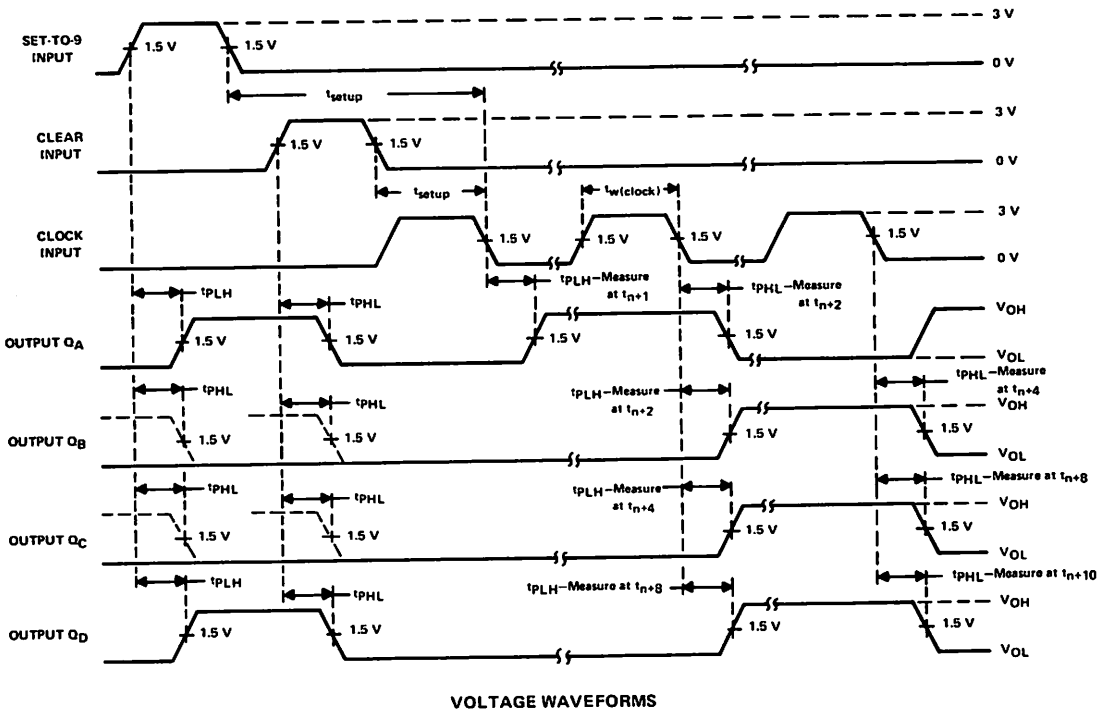
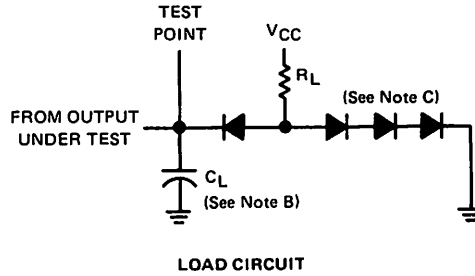
† f_{max} = maximum count frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

TYPES SN54490, SN74490 DUAL 4-BIT DECADE COUNTERS

PARAMETER MEASUREMENT INFORMATION

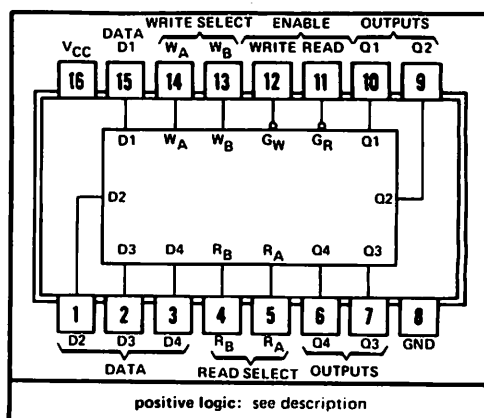


- NOTES: A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 5 \text{ ns}$, $t_f \leq 5 \text{ ns}$, $\text{PRR} = 1 \text{ MHz}$, duty cycle $\approx 50\%$, $Z_{out} \approx 50 \text{ ohms}$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N916 or 1N3064.

FIGURE 1

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Organized as 4 Words of 4 Bits
- Expandable to 1024 Words of n-Bits
- For Use as:
 - Scratch-Pad Memory
 - Buffer Storage between Processors
 - Bit Storage in Fast Multiplication Designs
- 3-State Outputs
- SN54LS170 and SN74LS170 Are Similar But Have Open-Collector Outputs

SN54LS670 . . . J OR W PACKAGE
SN74LS670 . . . J OR N PACKAGE
(TOP VIEW)



description

The SN54LS670 and SN74LS670 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W , is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R , is high, the data outputs are inhibited and go into the high-impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 nanoseconds typical) and the read time (24 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except read enable and write enable are buffered to lower the drive requirements to one Series 54LS/74LS standard load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and have high-sink-current, three-state outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

The SN54LS670 characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74LS670 is characterized for operation from 0°C to 70°C .

TENTATIVE DATA SHEET

TYPES SN54LS670, SN74LS670

4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

logic

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

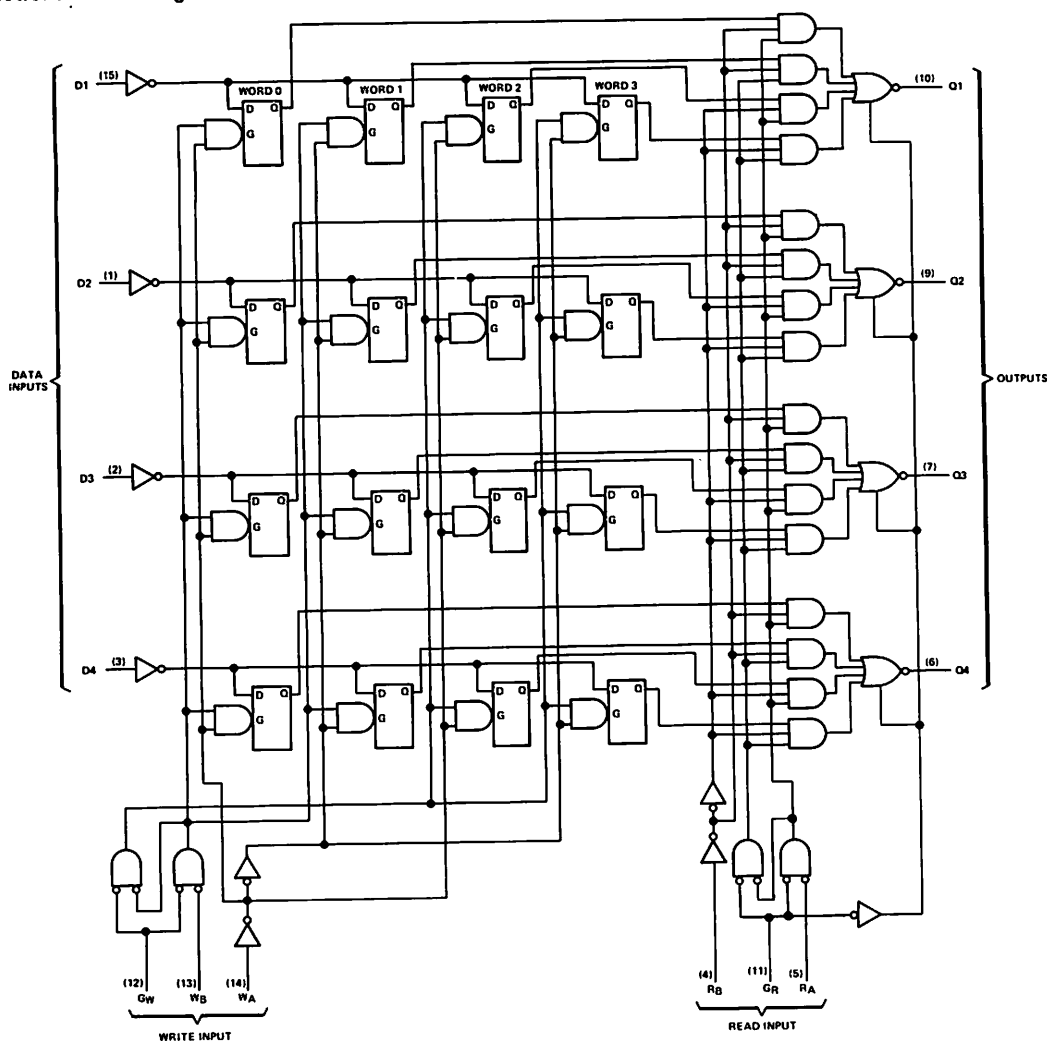
WRITE INPUTS			WORD			
W _B	W _A	G _W	0	1	2	3
L	L	L	Q = D	Q ₀	Q ₀	Q ₀
L	H	L	Q ₀	Q = D	Q ₀	Q ₀
H	L	L	Q ₀	Q ₀	Q = D	Q ₀
H	H	L	Q ₀	Q ₀	Q ₀	Q = D
X	X	H	Q ₀	Q ₀	Q ₀	Q ₀

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R _B	R _A	G _R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

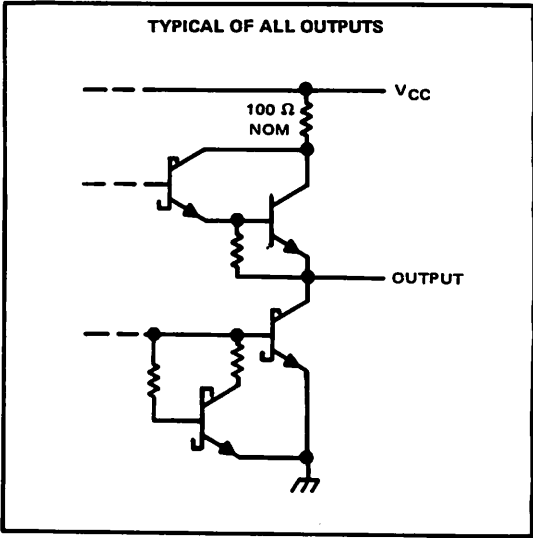
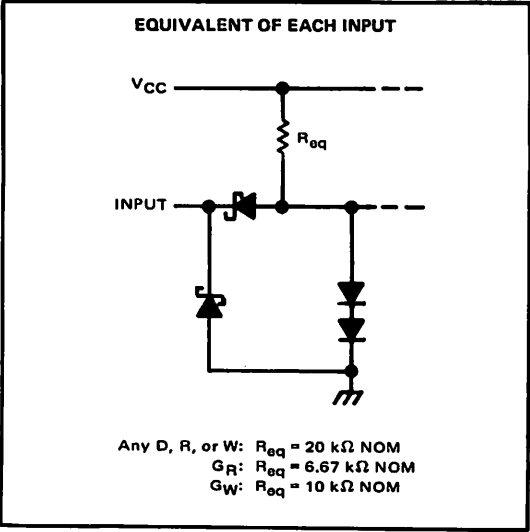
- NOTES: A. H = high level, L = low level, X = irrelevant, Z = high impedance (off)
 B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
 C. Q₀ = the level of Q before the indicated input conditions were established.
 D. W0B1 = The first bit of word 0, etc.

functional block diagram



TYPES SN54LS670, SN74LS670
4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS670	-55°C to 125°C
SN74LS670	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54LS670			SN74LS670			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-1			-2.6	mA
Low-level output current, I_{OL}				4			8	mA
Width of write-enable or read-enable pulse, t_W		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{setup}(D)$	10			10			ns
	Write select with respect to write enable, $t_{setup}(W)$	15			15			ns
Hold times, high- or low-level data (see Note 2 and Figure 2)	Data input with respect to write enable, $t_{hold}(D)$	15			15			ns
	Write select with respect to write enable, $t_{hold}(W)$	5			5			ns
Latch time for new data, t_{latch} (see Note 3)		25			25			ns
Operating free-air temperature range, T_A		-55		125	0		70	$^{\circ}\text{C}$

- NOTES: 1. Voltage values are with respect to network ground terminal.
 2. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{setup}(W)$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{hold}(W)$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
 3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

TYPES SN54LS670, SN74LS670

4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS670			SN74LS670			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage			0.7			0.8		V
V _I Input clamp voltage	V _{CC} = MIN, I _I = -18 mA		-1.5			-1.5		V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL max}	I _{OH} = -1 mA		2.4	3.4			V
		I _{OH} = -2.6 mA				2.4	3.1	
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL max}	I _{OL} = 4 mA		0.25	0.4	0.25	0.4	V
		I _{OL} = 8 mA				0.35	0.5	
I _{OZH} Off-state output current, high-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V			20		20		µA
I _{OZL} Off-state output current, low-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V			-20		-20		µA
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V	Any D, R, or W		0.1		0.1		mA
		G _W		0.2		0.2		
		G _R		0.3		0.3		
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.7 V	Any D, R, or W		20		20		µA
		G _W		40		40		
		G _R		60		60		
I _{IL} Low-level input current	V _{CC} = MAX	Any D, R, or W		-0.4		-0.4		mA
		G _W		-0.8		-0.8		
		G _R		-1.2		-1.2		
I _{OS} Short-circuit output current§	V _{CC} = MAX	-6	-40	-5	-42			mA
I _{CC} Supply current	V _{CC} = MAX, See Note 4	30	50	30	50			mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

NOTE 4: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Read select	Any Q	C _L = 15 pF, R _L = 2 kΩ, See Figures 1 and 2	23	40		ns
t _{PHL}				25	45		
t _{PLH}	Write enable	Any Q	C _L = 15 pF, R _L = 2 kΩ, See Figures 1 and 3	26	45		ns
t _{PHL}				28	50		
t _{PLH}	Data	Any Q		25	45		ns
t _{PHL}				23	40		
t _{ZH}	Read enable	Any Q	C _L = 5 pF, R _L = 2 kΩ, See Figures 1 and 4	15	35		ns
t _{ZL}				22	40		
t _{HZ}				30	50		ns
t _{LZ}				16	35		

¶t_{PLH} ≡ propagation delay time, low-to-high-level output

t_{PHL} ≡ propagation delay time, high-to-low-level output

t_{ZH} ≡ output enable time to high level

t_{ZL} ≡ output enable time to low level

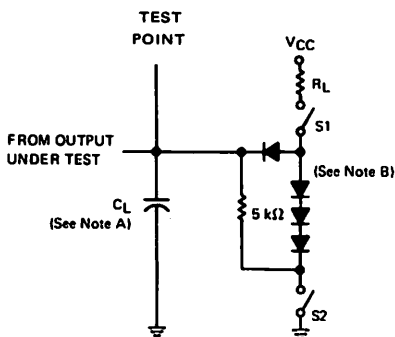
t_{HZ} ≡ output disable time from high level

t_{LZ} ≡ output disable time from low level

TYPES SN54LS670, SN74LS670

4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

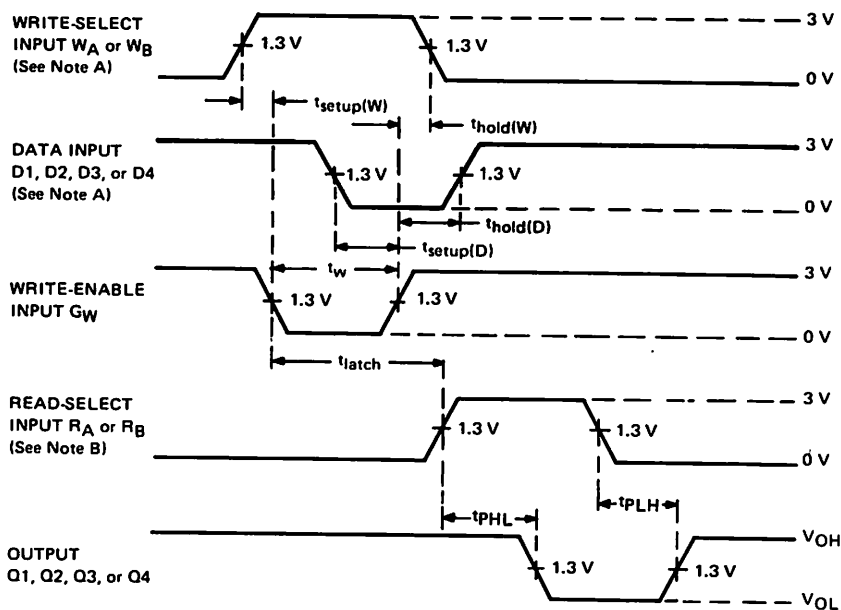
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

LOAD CIRCUIT

FIGURE 1

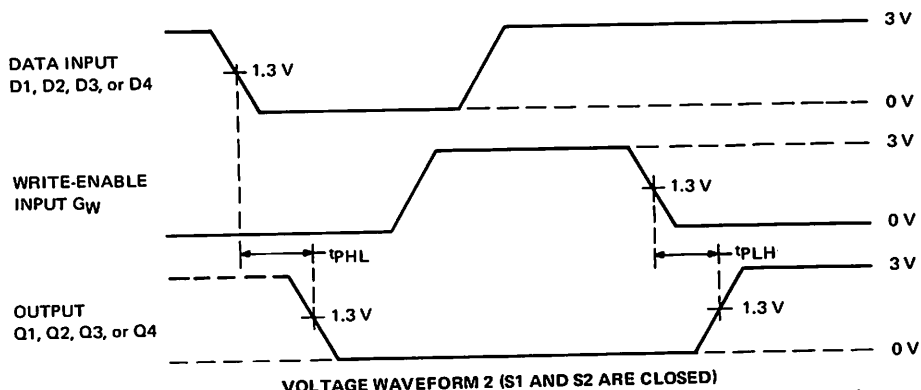
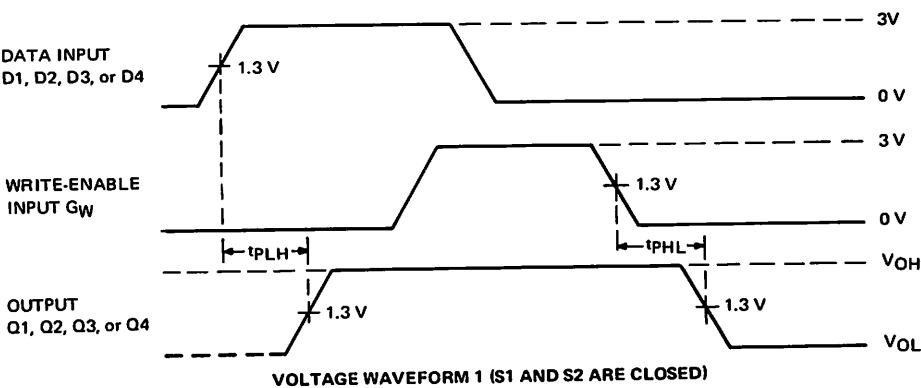


VOLTAGE WAVEFORMS (S1 AND S2 ARE CLOSED)

NOTES: A. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.
B. When measuring delay times from a read-select input, the read-enable input is low.
C. Input waveforms are supplied by generators having the following characteristics: $PRR \leq 2 \text{ MHz}$, $Z_{out} \approx 50 \Omega$, duty cycle $\leq 50\%$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$.

FIGURE 2

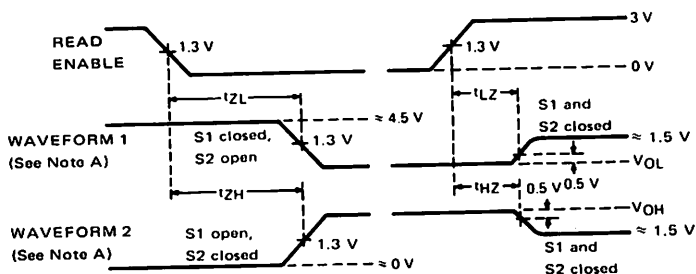
3



VOLTAGE WAVEFORM 2 (\$1 AND \$2 ARE CLOSED)

NOTES: A. Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.

B. Input waveforms are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_{out} \approx 50 \Omega$, duty cycle $\leq 50\%$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$.

FIGURE 3

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES:

- A. Waveforms 1 is for an output with internal conditions such that the output is low except when disabled by the read-enable input. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the read-enable input.
- B. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.
- C. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50 \Omega$, duty cycle $\leq 50\%$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

FIGURE 4

FIGURE 4

54/74 Family Beam-Lead TTL Circuits

BEAM-LEAD LOW-POWER SCHOTTKY[†] CHIPS

**TYPES BL54LS10, BL54LS76, BL54LS86,
BL54LS136, BL54LS266, BL74LS10, BL74LS76,
BL74LS86, BL74LS136, BL74LS266**
BULLETIN NO. DL-S 7412120, MARCH 1974

- Silicon-Nitride-Sealed Junctions
- Gold Beams

- Available in Two Temperature Ranges:
Series BL54LS . . . -55°C to 125°C
Series BL74LS . . . 0°C to 70°C

description

Series BL54LS/BL74LS integrated circuit chips comprise a family of TTL designed for general purpose and high-reliability applications and feature low power with medium operating speed. These chips utilize beam-lead sealed-junction technology and may be combined to form more complex beam-lead assemblies. The chips when assembled exhibit characteristics comparable to the Series 54LS/74LS devices of the same type number. The list below shows only the additions to the list shown in *The TTL Data Book for Design Engineers*, CC-411, and the BL54LS10Y and BL74LS10Y for which the beam assignments were shown incorrectly in CC-411.

DEVICE TYPES		FUNCTION	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION
BL54LS10	BL74LS10	Triple 3-Input NAND Gates	9.5 ns	6 mW
BL54LS76	BL74LS76	Dual J-K Negative-Edge Triggered Flip-Flops with Preset and Clear	13 ns	20 mW
BL54LS86	BL74LS86	Quadruple 2-Input Exclusive-OR Gates	10 ns	30.5 mW
BL54LS136	BL74LS136	Quadruple 2-Input Exclusive-OR Gates with Open-Collector Outputs	18 ns	30.5 mW
BL54LS266	BL74LS266	Quadruple 2-Input Exclusive-NOR Gates with Open-Collector Outputs	18 ns	40 mW

BEAM ASSIGNMENTS

TYPE	BL54LS10Y BL74LS10Y	BL54LS76Y BL74LS76Y	BL54LS86Y BL74LS86Y	BL54LS136Y BL74LS136Y	BL54LS266Y BL74LS266Y
FORMAT	50	65	45	45	45
BEAM					
1	1Y*	NC	1A	1A	1A
2	1A*	1 CLEAR	1B	1B	1B
3	V _{CC}	1J	1Y	1Y	1Y
4	NC	V _{CC}	2A	2A	2Y
5	1B*	2 CLOCK	2B	2B	2A
6	1C*	NC	2Y	2Y	2B
7	2A	2 PRESET	GND	GND	GND
8	2B	2 CLEAR	3Y	3Y	3A
9	2C	2J	3A	3A	3B
10	2Y	NC	3B	3B	3Y
11	GND	2Q	4Y	4Y	4Y
12	NC	NC	4A	4A	4A
13	3Y	2Q	4B	4B	4B
14	3A	2K	V _{CC}	V _{CC}	V _{CC}
15	3B	GND			
16	3C	1Q			
17		NC			
18		1Q			
19		NC			
20		1K			
21		1 CLOCK			
22		1 PRESET			

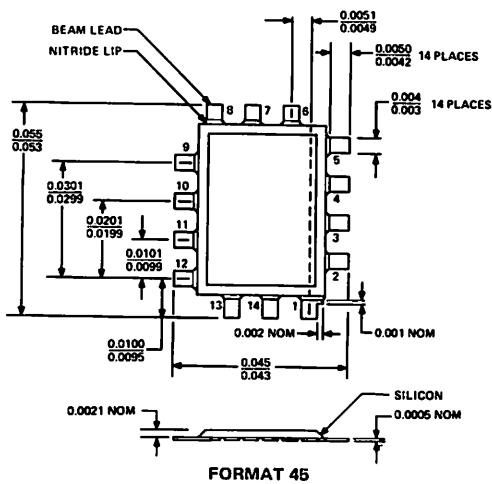
NC—No internal connection

*Changes from previously published data.

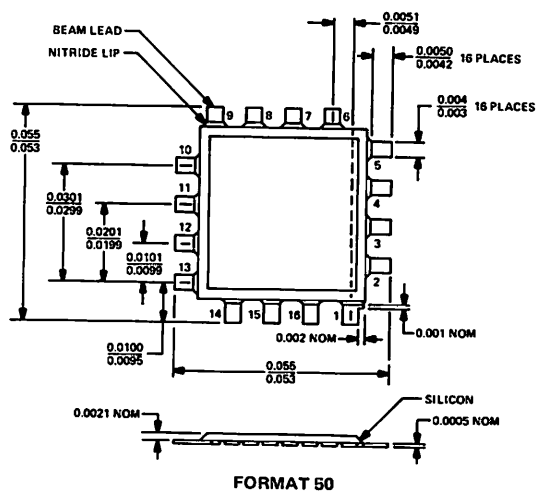
[†]Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

TYPES BL54LS10, BL54LS76, BL54LS86, BL54LS136, BL54LS266,
BL74LS10, BL74LS76, BL74LS86, BL74LS136, BL74LS266

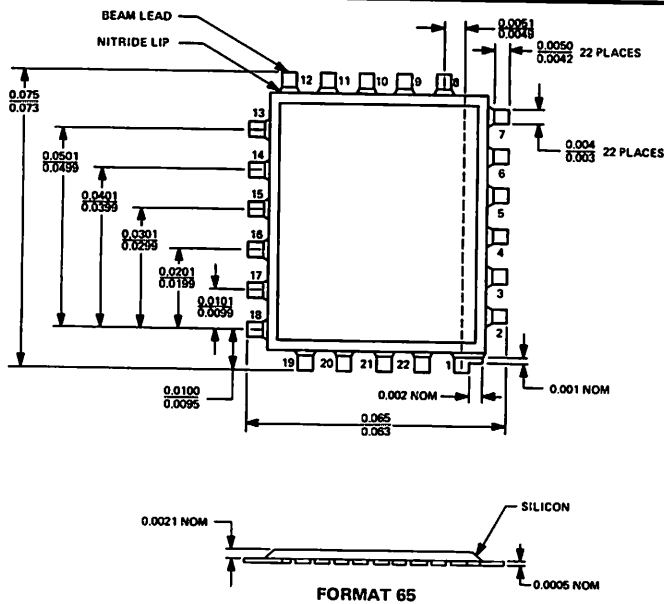
MECHANICAL DATA FOR BEAM-LEAD CHIPS



NOTES: a. Beam relative positions are identical on all four sides.
b. All dimensions are in inches.



NOTES: a. Beam relative positions are identical on all four sides.
b. All dimensions are in inches.




NOTES: a. Beam relative positions are identical on all four sides.
b. All dimensions are in inches.

38510/MACH IV
High Reliability Microelectronics
Procurement Specifications
MIL-STD-883

CONTENTS		
SECTION		PAGE
1.0	SCOPE	S-347
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4.0	QUALITY ASSURANCE PROVISIONS	S-359
5.0	PREPARATION FOR DELIVERY	S-369
6.0	NOTES	S-371

REVISIONS					
CLASSIFICATION (MAJOR/MINOR)	DATE CODE EFFECTIVITY	LTR	DESCRIPTION	DATE	APPROVED
Major	7040	A	Incorporate MIL-M-38510 and Revision Notice 2 of MIL-STD-883	8/15/70	<i>J. Adams</i>
Major	7239	B	Incorporate Revision Notice 3 and 4 of MIL-STD-883 and Revision A of MIL-STD-38510	9/1/72	<i>[Signatures]</i>
Major	7401	C	Incorporate revised Level IV (SNH) processing with inclusion of recorded electrical data with delta requirements; incorporate technological criteria in Table III for precap of complex circuits.	1/1/74	<i>[Signatures]</i>

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES $\pm 1^\circ$ 3 PLACE DECIMAL ± 0.010 2 PLACE DECIMAL ± 0.02 INTERPRET DWG. IN ACCORDANCE WITH STD. DESCRIBED IN MIL-STD-100 MATERIAL:	DR <i>C. E. Long</i> DATE <i>9/10/69</i>	 TEXAS INSTRUMENTS INCORPORATED SEMICONDUCTOR CIRCUITS DIVISION DALLAS, TEXAS		
	CHK <i>[Signature]</i> DATE <i>10/17/69</i> DES <i>[Signature]</i> DATE <i>10/16/69</i> QUALITY CONTROL <i>[Signature]</i> DATE <i>10/16/69</i> QA MGR. <i>J. D. Adams</i> DATE <i>10/16/69</i>			TITLE
	DESIGN ACTIVITY RELEASE DEPARTMENT <i>[Signature]</i> MANAGER, TAL <i>[Signature]</i> CIRCUITS DIVISION MANAGER <i>[Signature]</i>	SIZE A SCALE	CODE IDENT NO. 01295 REV C	DRAWING NO. 38510/MACH IV PROGRAM SHEET

38510/MACH IV PROCUREMENT SPECIFICATION

38510/MACH IV PROGRAM

The Texas Instruments 38510/MACH IV Program includes a complete procurement document encompassing general specification MIL-M-38510 and MIL-STD-883. The 38510/MACH IV Program is a realistic cost-effective supplement to JAN, offering 38510/883 screening for those device types not yet covered by JAN specifications or those JAN circuits without adequate availability. The 38510/MACH IV Program device types may be cross-referenced to JAN circuit types, class, package, and finish codes on pages S-376 through S-378. The 38510/MACH IV Program places major emphasis on designing and building quality and reliability into the device, realizing that no specification or screening procedure can substitute for inherent reliability. It is realized that irrespective of lot quality, there will always be some small percentage of devices that are subject to early failure ("infant mortality"). The 38510/MACH IV screening will reduce these early failures and serve to demonstrate with a high degree of statistical confidence that the required levels of quality and reliability have in fact been built into the device. The program is backed up by factory and distributor stocking programs on standard 38510/MACH IV Class B (SNC) devices, allowing quick delivery on most popular device types.

The 38510/MACH IV Program establishes the following reliability screening levels.

CLASS	NUMBER	ESTIMATED FAILURE RATE*
Class C	SNM54XX	0.010 — 0.020% per 1000 hours
Industrial Hi Rel	SNA54XX	0.007 — 0.020% per 1000 hours
Class B	SNC54XX	0.004 — 0.008% per 1000 hours
Class A	SNH54XX	0.002 — 0.005% per 1000 hours

*Not guaranteed

Each reliability screening level is tested to the following method of MIL-STD-883 test methods and procedures.

TEST METHOD	CLASS C	INDUSTRIAL HI-REL	CLASS B	CLASS A
	SNM	SNA	SNC	SNH
Precap Visual, 2010.1	Cond B	T1 Defined	Cond B	Cond A
Stab. Bake, 1008	100%	100%	100%	100%
Temp. Cycle, 1010	100%	100%	100%	100%
Centrifuge, 2001	100%	100%	100%	100%
Fine Leak, 1014	100%	Sample	100%	100%
Gross Leak, C1, 1014	100%	Sample	100%	100%
Pre-Burn In Data, 25°C, DC	—	—	—	100%
Burn-In, 1015	—	168 hours	168 hours	240 hours
Post-Burn In Data, 25°C, DC	—	—	—	100%
X-Ray, 2012	—	—	—	100%

The 38510/MACH IV Program also offers an aid to specification writing by providing a base 38510 and 883 document, whereby special device program specifications may be written invoking any additional testing options unique to a specific program. The 38510/MACH IV specification is organized and written per MIL-STD-100 to allow its use as a program specification by merely adding the user's company name and drawing number, as well as any required additions or deletions necessary to meet the specific program goals.

38510/MACH IV PROCUREMENT SPECIFICATION

38510/MACH IV PROGRAM

1.0 SCOPE

1.1 This specification establishes standards for materials, workmanship, performance capabilities, identification and processing of high-reliability bipolar monolithic integrated circuits.

1.2 Intent

The intent of this document is such as to recognize that quality and reliability are *built* into, not *tested* into, a product. There is no specification or screening procedure that can substitute for inherent, built-in reliability. However, it must be realized that irrespective of lot quality, there will always be some small percentage of devices that are subject to early failure (infant mortality). A well engineered screening procedure will eliminate most, if not all, of these early failures. Secondly, the screening and acceptance testing described herein will also serve to demonstrate, with a high degree of statistical confidence, that the required levels of quality and reliability have, in fact, been built into the product.

2.0 APPLICABLE DOCUMENTS

2.1 The following specifications and standards, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein:

2.2 Specifications

Military/NASA

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	Microcircuits devices, general specification for
NASA 85M03766	Microcircuit, Monolithic Silicon TTL Family of Devices, Specification Control Drawing for

1

38510/MACH IV PROCUREMENT SPECIFICATION

2.3 Standards

Military/NASA

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-883	Test Methods and Procedures for Microelectronics
MIL-STD-790	Reliability Assurance Program for Electronic Parts Specification
MIL-STD-1276	Leads, Weldable, for Electronic Components Parts
MIL-STD-1313	Microelectronics Terms and Definitions
MSFC-STD-355	Radiographic Inspection Standard for Electronic Parts

Detail Specifications

SNXXXX	Detail Specification for a Particular Part Type (e.g., Manufacturer's Data Sheet)
--------	---

2.4 Precedence of Documents

For the purpose of interpretation, in case of any conflicts, the following order of precedence shall apply:

- | | |
|------------------------------|--|
| a) Purchase Order | —The purchase order shall have precedence over any referenced specification. |
| b) Detail Specification | —The detail specification shall have precedence over this specification and other referenced specifications. |
| c) This Specification | —This specification shall have precedence over all referenced specifications. |
| d) Referenced Specifications | —Referenced Specifications shall apply to the extent specified herein. |

2.5 Federal and/or military specifications and standards required shall be obtained from the usual government sources.

38510/MACH IV PROCUREMENT SPECIFICATION

3.0 GENERAL REQUIREMENTS

The individual item requirements shall be as specified herein and in accordance with the applicable detail specification. In the event of any conflict between the requirements of this specification and the detail specification, the latter shall govern. The static and dynamic electrical performance requirements of the integrated circuits plus absolute maximum ratings and test methods shall be as specified in the detail specifications.

3.1.1 Definitions

- | | |
|-------------------|---|
| a) LTPD | Lot Tolerance Percent Defective shall be as defined by MIL-M-38510. |
| b) λ | Lambda, stated in percent per 1000 hours as defined by MIL-M-38510. |
| c) MRN | Minimum reject number as defined by MIL-M-38510. |
| d) Production Lot | For the purpose of this specification, a production lot shall be defined per MIL-M-38510. |
| e) Inspection Lot | An inspection lot shall be as defined in MIL-M-38510. |
| f) C | Acceptance number as defined by MIL-M-38510. |

3.1.2 Terms and Definitions

Terms and definitions shall be as defined in MIL-STD-1313.

3.1.3 Classification of Requirements

The requirements for the integrated circuits are classified herein as follows:

<u>Requirement</u>	<u>Paragraph</u>
Process Conditioning, Testing and Screening	3.2
Qualification	3.3
Design and Construction	3.4

38510/MACH IV PROCUREMENT SPECIFICATION

Marking of Integrated Circuits	3.5
Product Assurance	3.6
Workmanship	3.7
Performance Capabilities	3.8
Quality and Reliability Assurance Program Plan	3.9

3.2 Process Conditioning, Testing and Screening

Four levels of screening and quality assurance for integrated circuits are provided for in this specification. Process conditioning, testing and screening shall be as specified in 4.3 and the applicable figure for the appropriate quality assurance level stated on the purchase order and defined as follows:

Screening Level	Part Number Prefix	Applicable Process Flow Chart
38510/883A	SNH (Level IV)	Figure 4
38510/883B	SNC (Level III)	Figure 3
38510/883C	SNM (Level I)	Figure 1
Industrial High Reliability	SNA (Level II)	Figure 2

3.3 Qualification

Vendor qualification for delivery of integrated circuits to this specification shall be as specified in paragraph 4.2.

3.4 Design and Construction

Integrated circuit design and construction shall be in accordance with the requirements specified herein and in the applicable detail specification.

3.4.1 Topography

Integrated circuits furnished under this specification shall have topography information available for review by procuring activity. The information made available shall provide sufficient data for thorough circuit design, application, performance, and failure analysis studies.

3.4.1.1 Monolithic Die Topography

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showing the topography of elements formed on the silicon monolithic die shall be available for review. This shall be identified with the specific detail integrated circuit part-type in which it is used and the applicable detail specification.

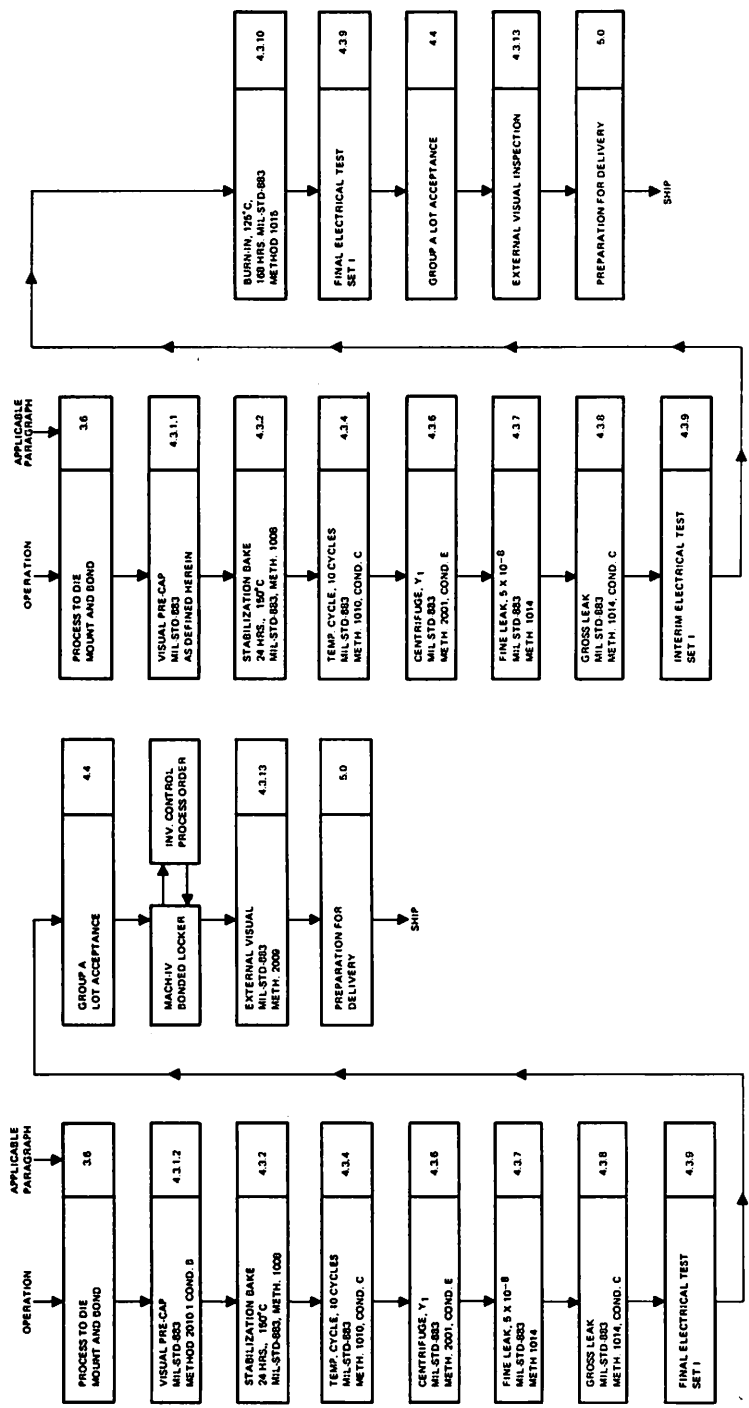


FIGURE 1—FLOW CHART FOR LEVEL I (SNM)

FIGURE 2—FLOW CHART FOR LEVEL II (SNA)

38510/MACH IV PROCUREMENT SPECIFICATION

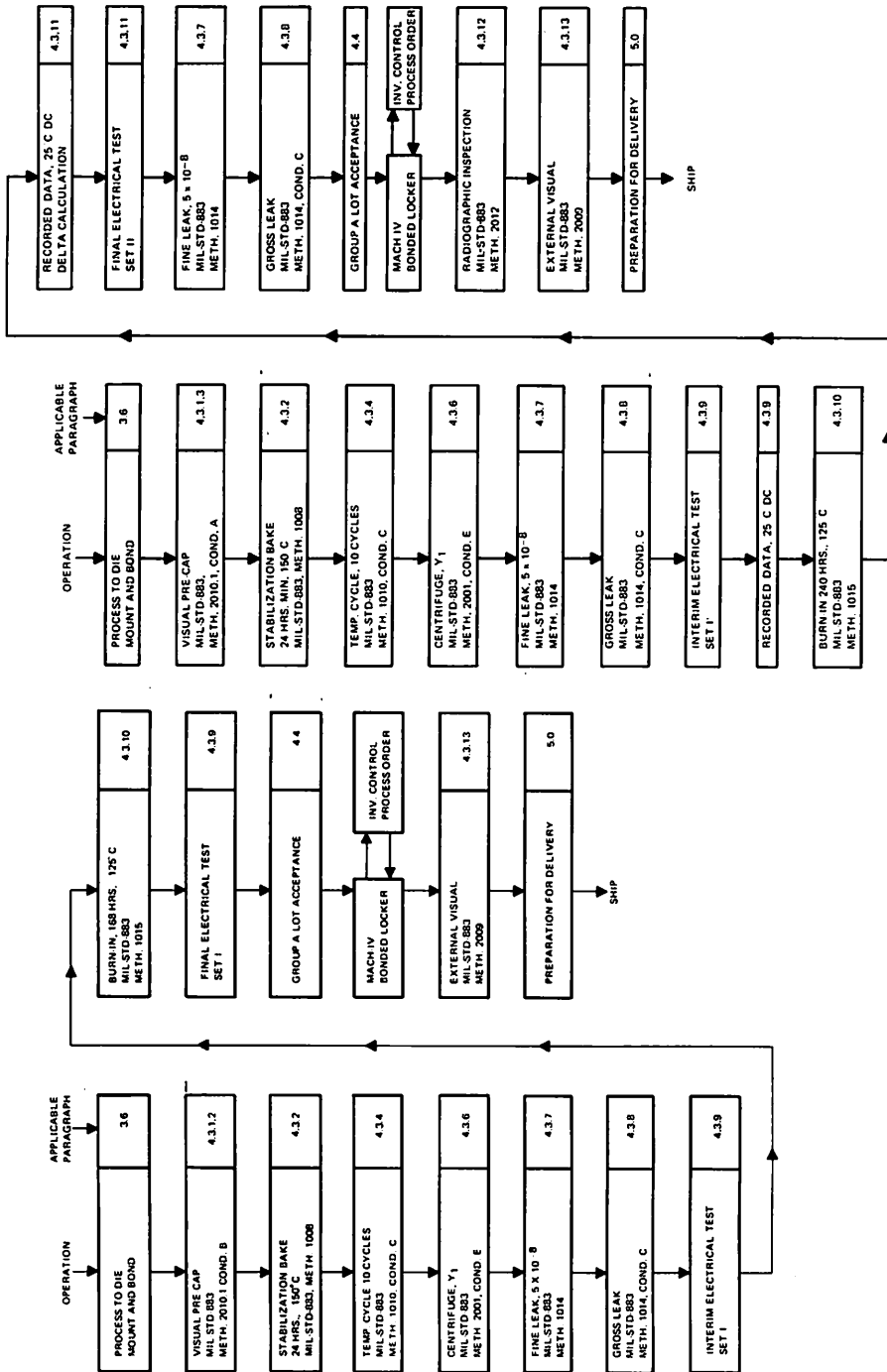


FIGURE 3—FLOW CHART FOR LEVEL III (SNC)

FIGURE 4—FLOW CHART FOR LEVEL IV (SNH)

38510/MACH IV PROCUREMENT SPECIFICATION

3.4.1.2 Die Intraconnection Pattern

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showing the specific intraconnection pattern utilized to intraconnect the elements in the circuit. This shall be in the same scale as the die topography 3.4.1.1 so that the elements utilized and those not being used can easily be determined.

3.4.2 Materials

Materials shall be inherently non-nutrient to fungus and shall not blister, crack, outgas, soften, flow or exhibit other immediate or latent defects that adversely affect storage, operation or environmental capabilities of integrated circuits.

3.4.2.1 Material Selection

Materials selected for use in the construction of the integrated circuits shall be chosen for maximum suitability for the application. This shall include consideration of the best balance for:

- a) Electrical performance
- b) Thermal compatibility and conductivity
- c) Chemical stability including resistance to deleterious interactions with other materials
- d) Metallurgical stability with respect to adjacent materials and change in crystal configuration
- e) Maximum stability with regard to continued uniform performance through the specified environmental conditions and life.

3.4.2.2 Foreign Materials

No lacquer, grease, paste, desiccant or other similar foreign encapsulant or coating material shall be included in the circuit enclosure nor applied to any part of the internal circuit assembly.

3.4.3 Mechanical

3.4.3.1 Case

Each integrated circuit shall be securely mounted and hermetically sealed within a case designed and constructed to conform to the outline and physical dimensions shown in the detailed specification. External surfaces of the integrated circuit case shall be unpainted except for markings.

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3.4.3.2 Interconnections

Interconnections within the integrated circuit case shall be minimized and there shall be no wire crossovers. Circuit intraconnections by means of wire jumpers shall not be used. (See Note 6.2)

3.4.3.3 Leads

Lead material, construction, and outline shall be as specified on the detail specification and shall be capable of meeting the solderability test of MIL-STD-883, Method 2003. (See note 6.4).

3.4.3.3.1 Lead Size

Lead outline and dimensions shall be as specified in the detail specification.

3.4.3.3.2 Lead Surface Condition

Leads shall be free of the following defects over their entire length when inspected under a minimum of 4X magnification:

- a) Foreign materials adhering to the leads such as paint, film, deposits and dust. Where adherence of such foreign materials is in question, leads may be subjected to a clean, contaminant-free (e.g., oil, dust, etc.), filtered air stream (suction or expulsion) of 88 feet per second maximum, or a wash/rinse as necessary and reinspected.
- b) Nicks, cuts, scratches or other surface defacing defects which expose the base metal.

3.4.3.3.3 Lead Straightness

Leads shall be aligned within a 0.050-inch diameter, 0.050-inch length cylinder concentric to the point of lead emergence from the case and the X-axis (the axis parallel to the lead axis). Along the remaining lead length, there shall be no unspecified bend whose radius is less than 0.10 inch and no twist whose angle is greater than 30° (ribbon leads, only).

3.4.3.3.4 Preformed Leads

Preformed leads, when specified, shall be in accordance with the detail specification. The part number of the integrated circuit shall remain as specified in the applicable detail specification or purchase order, the applicable suffix designation shall appear on the purchase order but shall not be marked on the device.

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3.4.3.3.5 Carriers (Mech-Pak Carrier)

Carrier-matrix assemblies consisting of individually mounted integrated circuits shall be furnished when so specified by purchase order. The individual carriers shall have provisions for use with automatic test equipment contacts. Devices supplied "clipped-out" of the Mech-Pak Carrier shall be supplied in the Barnes Carrier type 029-188 or equivalent. (Applicable to Flat Packs only.)

3.5 Marking of Integrated Circuits

3.5.1 Legibility

All marking shall be permanent in nature and remain legible when subjected to specified operating, storage, and environmental requirements. All markings shall be insoluble in standard solvents such as trichlorethylene, water and xylene.

3.5.2 Marking Details

Marking of the integrated circuits shall be located as follows unless otherwise specified in the detail specification:

- a) TO-99, TO-100, and similar "can" cases shall be marked on the top of the case. Where space limitations exist, the side of the case may be used.
- b) Flat Packs shall be marked on the top of the case. Where space limitation exists, the bottom of the package may be utilized as necessary. As a minimum the top of the package shall show the manufacturer's identification mark or symbol, the device part number, date code, and pin 1 orientation mark (where applicable).
- c) Dual-in-line plug-in packages shall be marked in the same manner as flat packs.

3.5.3 Required Device Marking

- a) Index point indicating the starting point for numbering of leads shall be as indicated in the detail specification. The indexing point may be a tab, color dot, or other suitable indicator.
- b) Manufacturer's identification mark or symbol.
- c) An alpha-numeric lot date code indicating the week of initial submission for screening or inspection. The date code shall be as follows:
 - 1) EIA four-digit date code, the first two numbers shall be the last two digits of the year, the last two numbers shall indicate the calendar week.

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- 2) A Gothic letter which identifies separate lots of the same device type processed within the same calendar week. (If no more than one lot is processed through screening or inspection in a given calendar week, the Gothic letter may be omitted.)
- d) Manufacturer's part number defining circuit type and applicable MACH IV screening level and MIL-M-38510 product assurance level as defined in paragraph 3.2.
- e) Individual device serial number is required for Level IV (SNH).
- f) A dot to indicate acceptance by Radiographic inspection

NOTE:

When a color dot is used to identify pin one, the radiographic inspection acceptance dot shall be placed on the bottom of the package.

3.6 Product Assurance

The manufacturer shall establish and maintain a reliability assurance program that complies with the basic intent of MIL-STD-790. Furthermore, it is intended that each integrated circuit delivered shall be free of any defect in design, material, manufacturing process, testing and handling, which would degrade or otherwise limit its performance when used within the specified limits.

3.6.1 Visual and Mechanical Examination

Integrated circuits shall be examined to verify that material, design, construction, physical dimensions, marking and workmanship are in accordance with the specified acceptance criteria.

3.6.2 Test Equipment

The manufacturer shall prepare and maintain a current list, by name and drawing number or other unique identification, of test equipment used in the manufacturing and testing of devices submitted for acceptance inspection under this specification. This list shall be made available to the procuring activity representative upon request.

3.6.3 Process Controls

Each integrated circuit shall be constructed by manufacturing processes which are under the surveillance of the manufacturer's Quality Control department. The processes shall be monitored and controlled by use of statistical techniques in accordance with published specifications and procedures. The manufacturer shall prepare and maintain suitable documentation (such as quality control manuals, inspection instructions, control charts, etc.) covering all phases of incoming part and material inspection and in-process inspections required to assure that product quality meets the requirements of this specification. The

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procuring activity may verify, with the permission of and in the company of the manufacturer's designated representative, that suitable documentation exists and is being applied. Information designated as proprietary by the manufacturer will be made available to the procuring activity or its representative only with the written permission of the manufacturer.

Process control is recognized as being vital to the concept of "built-in" quality. Appendix A defines an acceptable process-control system. Devices delivered to this specification shall be manufactured in a controlled system similar to that set forth in Appendix A. The process control program shall include a scanning electron microscope (SEM) monitor program for evaluating the metal integrity over oxide step and oxide step contour. The SEM analysis will be defined in a Quality & Reliability Assurance document.

3.6.4 Production Changes

The manufacturer shall advise the procuring activity of the time at which any major change(s) in production or QC methods or documentation become effective during the period of device production for delivery against any given purchase order referencing this specification.

3.7 Workmanship

Integrated circuits shall be manufactured and processed in a careful and workmanlike manner, in accordance with the production processes, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of the reliability assurance program established by paragraph 3.6.

3.7.1 Personnel Certification

The manufacturer shall be responsible for training, testing and certification of personnel involved in producing integrated circuits. Training shall be commensurate and consistent with the requirements of this specification and in conformance to the basic intent of MIL-STD-790. Training aids in the form of satisfactory criteria shall be available for operator and inspector review at any time.

3.7.2 Personnel Evaluation

The supplier shall maintain a continuous evaluation of the proficiency of personnel concerned with production and inspection. Retraining of an operator or inspector shall be required when this evaluation establishes that a degree of proficiency necessary to meet the requirements of this specification is not being exercised.

3.7.3 Rework Provisions

38510/MACH IV PROCUREMENT SPECIFICATION

3.7.3.1 Rework

All rework on microrcircuits manufactured under this specification shall be accomplished in accordance with paragraph 3.7.1 of MIL-M-38510 as defined herein.

3.7.3.2 Rebonding

Rebonding shall be in accordance with MIL-M-38510, with the total number of rebond attempts per microcircuit limited to a maximum of 10 percent of the total number of bonds in the microcircuit. The 10 percent limit on rebonds may be interpreted as the nearest whole number to the 10 percent value. A bond shall be defined as a wire to post or wire to pad bond (i.e., for a 14-lead wire-bonded package there are 28 bonds). Bond-offs required to clear the bonder after an unsuccessful first bond attempt need not be considered as rebonds provided they can be identified as bond-offs by being made physically off the plated post or if they contain a non-typical number of wedge marks. The initial bond attempt need not be visible. A replacement of one wire bonded at one end of an unsuccessful bond attempt at one end of the wire counts as one rebond; a replacement of a wire bonded at both ends counts as two rebonds. A ball bond on top of a ball bond is not permissible. No more than one rebond attempt shall be permitted at any pad or post and no rebonds shall be made where pad metallization has been lifted.

3.8 Performance Capabilities

The integrated circuits delivered to this specification shall be designed to be capable of meeting the environmental requirements specified in Table II. The manufacturer need not perform these tests specifically for the contract or specification, but shall provide data which demonstrates the ability of the integrated circuits to pass the environmental tests. The data shall have been generated on devices from the same generic family as the circuits being supplied to this specification, and the package configuration shall be the same as for the delivered parts (i.e., Flat Pack, TO-100, etc.).

3.9 Quality and Reliability Assurance Program Plan

The manufacturer shall establish and implement a Quality and Reliability Assurance Program Plan that meets the intent of MIL-M-38510, Appendix A. Submission of the program plan to the procuring activity shall not be a requirement of this specification, however, the program plan shall be maintained by the manufacturer and shall be available for review by the procuring activity.

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4.0 QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection

Unless otherwise specified in the contract or purchase order, the manufacturer is responsible for the performance of all inspection requirements specified herein. Except as otherwise specified, the manufacturer may utilize his own facilities or any commercial laboratory acceptable to the procuring activity. The procuring activity may, at its discretion, perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

4.1.1 Inspection and Testing Procedures Coverage

Inspection and testing processes and procedures prepared in fulfillment of the reliability assurance program established per paragraph 3.6 shall be prescribed by clear, complete and current instructions. These instructions shall assure inspection and test of materials, work in process and completed integrated circuits as required by this specification. In addition, criteria for approval and rejection of materials and integrated circuits shall be included.

4.1.2 Inspection at Point of Delivery

The procuring activity may, at its discretion, reinspect any or all of the delivered parts. (Excluding Group B destructive samples as defined by MIL-STD-883). All parts, found to be defective and/or lacking specified documentation (such as test documentation) may be returned to the manufacturer at the manufacturer's expense.

4.1.3 Inspection Records

The manufacturer shall maintain a reliability data and records library. This library shall have on file, for review by the procuring activity, records of examination, qualification test results, variables data (when required) and all other pertinent data generated on devices manufactured to this specification.

4.1.4 Control of Procurement Sources

The manufacturer shall be responsible for assuring that all supplies and services conform to this specification, the detail specification and the manufacturer's procurement requirements.

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4.1.4.1 Manufacturer's Receiving Inspection

Purchased supplies shall be subjected to inspection after receipt as necessary to ensure conformance to contract requirements. In selecting sampling plans, consideration shall be given to the controls exercised by the procurement source and evidence of sustained quality conformance.

4.1.4.2 The manufacturer shall provide procedures for withholding from use all incoming supplies pending completion of required tests or receipt of necessary certification or test records and their evaluation.

4.1.4.3 The manufacturer shall initiate corrective action with the procurement source depending upon the nature and frequency of receipt of nonconforming supplies.

4.1.5 Procuring Activity Quality Assurance Representative

The procuring activity, may, at its discretion, place quality assurance representatives in the manufacturer's plant as deemed necessary to assure conformance to contract requirements in any non-proprietary phase of design, fabrication, processing, inspection, testing, and reliability of the integrated circuits being produced. The manufacturer shall provide reasonable facilities and assistance for the safety and convenience of such personnel in the performance of their duties. Inspection and test procedures shall be made available for review by the quality assurance representative.

4.2 Qualification and Quality Conformance Inspection

4.2.1 Qualification

Manufacturer's qualification shall be based on compliance with the established reliability test program requirements of paragraph 4.2.1.1 herein. The manufacturer may, at his discretion, substitute the qualification test plan of paragraph 4.2.1.2 in order to establish initial qualification. However, the substitution of paragraph 4.2.1.2 does not relieve the manufacturer from the responsibility of establishing an in-house reliability evaluation program as defined by paragraph 4.2.1.1.

4.2.1.1 Established Reliability Test Program

The manufacturer shall have an established and well defined in-house reliability program. This program shall be so designed as to demonstrate that the manufacturer's product is capable of meeting, as a minimum, the environmental and minimum life requirements listed in Table I herein. The reliability program may be modeled after the test procedure of Table I or it may take the form of a step-stress testing program similar to that defined by

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MIL-STD-883, Method 5006. The program shall be on-going in nature; that is, at specified intervals the manufacturer shall randomly select product that is representative of current production techniques, and subject the devices to the specified tests. Sampling shall be done on each generic family.

4.2.1.2 Qualification Test Program

In lieu of meeting the requirements of 4.2.1.1, the manufacturer may establish qualification by performing an initial, one-time qualification test in accordance with Table I herein. Qualification testing shall be performed on each generic family supplied to this specification. Upon successful completion of the qualification program, the manufacturer shall remain qualified for a period not to exceed 12 calendar months. Continued qualification shall then be based on compliance with the requirements of paragraph 4.2.1.1.

4.2.1.3 Procedures and Definitions

4.2.1.3.1 Sampling Procedure

Device selection for the qualification procedure of 4.2.1.1 or 4.2.1.2 shall be based on a random sampling technique. Linear sample shall be obtained from one generic family. Digital testing shall be done on a mixture of device types that adequately represent the entire generic family. The following is a recommended mix ratio:

Gates	:	65% of total sample
Flip-Flops	:	25% of total sample
MSI	:	10% of total sample

4.2.1.3.2 Generic Family

Electrically and structurally similar devices shall be said to comprise a generic family (e.g., TTL) if they meet the following criteria:

- a) Are designed with the same basic circuit-element configuration such as TTL, DTL, ECL, or Linear, and differ only in the number or complexity of specified circuits which they contain.
- b) Are designed for the same supply, bias and signal voltage, and for input/output capability with each other under an established set of loading rules.
- c) Are enclosed in housings (packages) of the same basic construction (e.g., hermetically sealed flat packages, dual-in-line ceramic, dual-in-line plastic) and outline, differing only in the number of active housing terminals included and/or utilized.

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4.2.2 Quality Conformance Inspection (Groups B and C per Table II)

- a) When specifically called out and funded on the purchase order or contract, the manufacturer shall perform the quality conformance inspections (Group B and/or Group C) on a lot-by-lot basis.
- b) When specifically called out and funded on the purchase order or contract, the manufacturer shall provide quality conformance inspection and generic data from the previous quarterly test results.

4.2.2.1 Lot Acceptance Sampling

Statistical sampling for quality conformance inspections shall be in accordance with MIL-M-38510 Table B1.

Group B samples except bond strength samples shall be selected from sublots that have successfully completed all of the 100% processing steps specified on the applicable process flow chart.

4.2.2.2 Resubmission of Failed Lots

When any lot submitted for quality conformance inspection fails any subgroup requirement, it may be resubmitted a maximum of one time for that particular subgroup. One additional submission is permitted, provided an analysis is performed to determine the failure mechanism for each reject device in the subgroup, and that it is determined that the failures are due to one of the following:

- a) Testing error resulting in electrical damage to devices
- b) A defect that can effectively be removed by rescreening the lot
- c) Random defects which do not reflect poor basic device designs or poor workmanship.

4.2.2.3 Early Shipments

When quality conformance inspection is being performed for a specific contract or purchase order, the accepted Group A devices that are awaiting shipment pending successful completion of Group B and/or Group C, shall be stored in the 38510/MACH IV bonded locker. Under no circumstances shall such parts be shipped prior to the successful completion of the Group B tests.

4.2.2.4 Groups B and C Test Data

All lot-by-lot data generated by Group B and/or Group C testing shall accompany the initial shipment of devices. This data shall consist, at a minimum, of the following:

- a) Attributes data for Group B. Endpoints for the subgroups are visual per the applicable MIL-STD-883 test method.

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- b) Attributes data for Group C subgroups 1, 2, 4 and 5. Endpoints for these subgroups shall be "critical electrical parameters" only.

4.2.2.5 Procedure in Case of Test Equipment Failure or Operator Error

Where an integrated circuit is believed to have failed as a result of faulty test equipment or operator error, the failure shall be entered in the test record which shall be retained for review along with a complete explanation verifying why the failure is believed to be invalid. If it is determined that the failure is invalid, a replacement integrated circuit from the same inspection lot may be added to the sample. The replacement integrated circuit shall be subjected to all those tests to which the discarded integrated circuit was submitted prior to its failure, and any remaining specified test to which the discarded integrated circuit was not subjected prior to its failure.

4.3 Quality Assurance Processing, Methods and Procedures

This section establishes the test methods and conditions to be used for the 100% processing (screening) requirements specified by the applicable process flow chart.

4.3.1 Precap Visual Inspection

Each microcircuit shall be required to pass the appropriate precap visual inspection defined as follows. Precap Lot Acceptance shall be per paragraph 4.6.

- 4.3.1.1 Level II devices shall be visually inspected in accordance with the criteria listed in Section 6.1.2 of this specification. Inspection procedures and equipment requirements shall be as defined in MIL-STD-883.

- 4.3.1.2 38510C (Level I) and 38510B (Level III) devices shall be visually inspected in accordance with MIL-STD-883, Method 2010.1, Condition B (See Note 6.1.1).

- 4.3.1.3 38510A (Level IV) devices (designated for NASA type applications) shall be visually inspected in accordance with the NASA approved precap requirements of NASA specification 85MO3766 for digital circuits.

- 4.3.1.4 Complex MSI and LSI circuits as defined in Table III may be precap inspected per Note 6.1.2 in lieu of precap 2010.1, Condition A, paragraph 4.3.1.3, or 2010.1, Condition B, paragraph 4.3.1.2.

4.3.2 Stabilization Bake

The purpose of this test is to determine the effect on microelectronic devices of baking at elevated temperatures without electrical stress applied. Test shall be performed in accordance with MIL-STD-883, Method 1008, Condition C.

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4.3.3 Thermal Shock

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature. Test shall be performed in accordance with MIL-STD-883, Method 1011, Condition A.

4.3.4 Temperature Cycle

This test is conducted for the purpose of determining the resistance of a part to exposures at extremes of high and low temperatures, and to the effect of alternate exposures to these extremes, such as would be experienced when equipment or parts are transferred to and from heated shelters in arctic areas. Test shall be performed in accordance with MIL-STD-883, Method 1010, Condition C, minimum of 10 cycles.

4.3.5 Mechanical Shock

The shock test is intended to determine the suitability of the devices for use in electronic equipment which may be subjected to moderate severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Test shall be performed in accordance with MIL-STD-883, Method 2002, Condition B, five blows minimum.

4.3.6 Centrifuge (Constant Acceleration)

The centrifuge test is used to determine the effects on microelectronics devices of a centrifugal force. This test is designed to indicate structural and mechanical weaknesses not necessarily detected in shock and vibration tests. Test shall be performed in accordance with MIL-STD-883, Method 2001, Condition E.

4.3.7 Fine Leak Test

Each integrated circuit for 38510C (Level I), 38510B (Level III), and 38510A (Level IV) screens shall be subject to a fine leak test in accordance with paragraph 4.3.7.1 or 4.3.7.2. The method shall be optional providing it is consistent with and capable of detecting the specified leak rate of the applicable process flow chart. Level II devices will be sample tested to a 1% AQL.

4.3.7.1 Helium Leak Test

Helium leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition A. Helium bomb pressure shall be 30 psig maximum, bomb time shall be 4 hours minimum.

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4.3.7.2 Radiflo Leak Test

Radiflo leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition B. Krypton 85 bomb pressure and dwell time are a function of the radioactivity level and shall be selected so as to conform to the equations given in Condition B.

4.3.8 Gross-Leak Test

Each integrated circuit for 38510C (Level I), 38510B (Level III), and 38510A (Level IV) screens shall be subjected to the appropriate gross-leak test of paragraphs 4.3.8.1 or 4.3.8.2 or an approved equivalent. The manufacturer may, at his option, perform gross-leak testing after the Set I Electrical Tests of paragraph 4.3.9. Level II devices will be sample tested to a 1% AQL.

4.3.8.1 When specifically called out and funded on the purchase order or contract, units will be bombed 4 hours minimum at 30 psi in FC-78. Units will then be immersed in FC-40 or equivalent at $+125^{\circ}\text{C} \pm 5^{\circ}\text{C}$ for 20 seconds minimum and observed for one large bubble or a continuous stream of small bubbles, MIL-STD-883, Method 1014, Condition C, Step 2.

4.3.8.2 Units will be immersed in FC-40 or equivalent at $+125^{\circ}\text{C} \pm 5^{\circ}\text{C}$ for 20 seconds minimum and observed for one large bubble or a continuous stream of small bubbles, MIL-STD-883, Method 1014, Condition C, Step 1.

4.3.9 Final Electrical Test (Set I)

Each integrated circuit shall be required to pass the electrical requirements of Subgroup 1 of the detail specification. The manufacturer shall also perform such additional testing necessary to assure the parts will meet the temperature extreme limits. In addition, Level IV (SNH) parts shall have critical 25°C dc electrical parameters read and recorded by serial number.

When specifically called out and funded on the purchase order or contract, the manufacturer shall perform subgroups 2, 3, and 4 of paragraph 4.4 in accordance with Method 5004 of MIL-STD-883, Notice 3.

4.3.10 Burn-In

The burn-in screen is performed for the purpose of eliminating marginal devices and early-life failures evidenced as time and stress dependent. Test shall be in accordance with MIL-STD-883, Method 1015, Condition A, D, or E at $125 \pm 5^{\circ}\text{C}$ for digital circuits and Conditions A, B, C, or D for linear circuits. The bias shall be removed from the devices prior to their return to 25°C . (See note 6.3)

4.3.11 Final Electrical Test (Set II)

Each integrated circuit shall be required to pass the electrical requirements of the detail specifications. The following tests shall be performed as a minimum: dc parameters at maximum and minimum rated temperatures, and switching parameters at 25°C . In addition, prior to dc testing at minimum and maximum rated temperature, each Level IV (SNH) part shall have critical 25°C dc electrical parameters read and recorded by serial number and shall pass the following delta requirements.

<u>PARAMETER</u>	<u>DELTA LIMIT</u>
VOL	$\pm 10\%$ of detail specification limit
VOH	$\pm 10\%$ of detail specification limit
IIL	$\pm 10\%$ of detail specification limit
IiH	$\pm 10\%$ of detail specification limit

One copy of the pre-burn-in and post-burn-in recorded data with delta calculations shall be shipped with each lot. The manufacturer may, when deemed necessary, elect to perform additional electrical testing over and above the requirements stated herein.

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4.3.12 Radiographic Insepction (X-ray)

Test shall be performed in accordance with MIL-STD-883, Method 2012, the integrated circuit shall be required to pass a radiographic inspection to these requirements. In addition, the acceptance criteria shall meet, as a minimum, the requirements of NASA MSFC-STD-355 except delete voiding criteria. X-ray may be performed at any point after serialization at the manufacturer's option.

4.3.13 External Visual Inspection

The purpose of this examination is to verify that materials, construction, marking, and general workmanship are as specified. Examination shall be in accordance with MIL-STD-883, Method 2009.

4.4 Group A Conformance

Group A conformance shall consist of the electrical parameters in the manufacturer's data sheet. If an inspection lot is made up of a collection of sublots, each sublot shall conform to Group A, as specified.

SUBGROUP	LTPD (%)			
	LEVEL I 38510C	LEVEL II	LEVEL III 38510B	LEVEL IV 38510A
Subgroup 1 25°C, dc	5	7	5	5
Subgroup 2 High Temperature, dc	10	10	7	5
Subgroup 3 Low Temperature, dc	10	10	7	5
Subgroup 4	10	10	7	5

Dynamic and Switching Tests @ 25°C

NOTE: Functional tests included in dc tests.

4.5 Certification

The manufacturer shall include a certificate of compliance with each shipment of parts if requested on the purchase order. This certificate shall indicate that all specified tests and requirements of this specification have been made or met, and that the lot of devices (identified by lot and/or batch number) is acceptable. The certificate shall bear the name and signature of the manufacturer's Quality Control representative, the date of acceptance or signing, and any pertinent notes as applicable.

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4.6 Precap Lot Acceptance

After each precap inspection the lot of devices shall be sampled by quality control and inspected for the specified visual criteria. The sampling plan shall be:

40X criteria – 1.0% AQL
100X criteria – 1.0% AQL

**TABLE I
MANUFACTURERS QUALIFICATION PROCEDURE**

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD
Subgroup 1			
Physical Dimensions Visual and Mechanical	2008	Condition A & B	15
Subgroup 2 ¹			
Solderability	2003		15
Subgroup 3 ²			
Thermal Shock	1011	Condition B	
Temperature Cycling	1010	Condition C	
Moisture Resistance	1004	Omit step 7B and Initial Conditioning	
Critical Electrical Parameters	5004	25°C, DC -	15
Subgroup 4 ²			
Mechanical Shock	2002	Condition B	
Vibration Variable Freq.	2007	Condition A	
Constant Acceleration	2001	Condition E	
Critical Electrical Parameters	5004	25°C, DC -	15
Subgroup 5 ¹			
Lead Fatigue	2004	Condition B2	
Fine Leak	1014	Condition A, Per Para. 4.3.7 Herein	
Gross Leak	1014	Condition C, Per Para. 4.3.7 Herein	15
Subgroup 6 ¹			
Salt Atmosphere	1009	Condition A, Omit Initial Conditioning	15
Subgroup 7 ²			
Storage Life	1008	150°C, 1000 Hrs. Minimum	
Critical Electrical Parameters	5004	25°C, DC -	10
Subgroup 8 ²			
Operating Life	1005	125°C, 1000 Hrs. Minimum Return to 25°C without bias	
Critical Electrical Parameters	5004	25°C, DC -	10
Subgroup 9 ¹			
Bond Strength			10 devices not greater than 1% defective
a. Thermocompressions	2011	Condition B, D	
b. Ultrasonic	2011	Condition B, D	

1. Visual and/or hermetic end points hence electrical or visual rejects may be used. Reference MIL-STD-883, Method 5005, Para.3.4.
2. Electrical end points only.

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TABLE II
LOT ACCEPTANCE/PERIODIC QUALIFICATION TESTS
(GROUP B/GROUP C)

GROUP B			LEVEL IV 38510A	LTPD LEVEL III 38510B	LEVEL I ¹ 38510C
TEST	MIL-STD-883 METHOD	CONDITIONS			
Subgroup 1					
Physical Dimensions Visual and Mechanical	2008	Condition A	10	15	20
Subgroup 2					
Marking Permanency Visual and Mechanical	2008	Condition B, para. 3.2.1			
	2008	Condition B per applicable detail specification			
Bond Strength 3 ²	2011	Condition B or D 2 grams for Au bonds 1 gram for Al bonds	10	15	20
Subgroup 3 ³					
Solderability	2003		10	15	15
Subgroup 4 ³					
Lead Fatigue	2004	Conditions B2			
Fine Leak	1014	Conditions A or B, per para. 4.3.7 of this spec.			
Gross Leak	1014	Condition C, per para. 4.3.8 of this spec.	10	15	15
GROUP C					
Subgroup 1 ⁴					
Thermal Shock	1011	Condition B			
Temp. Cycle	1010	Condition C			
Moisture Resistance	1004	Omit Initial Cond. & step 7B			
Critical Electrical Parameters	5004	25°C, DC	10	15	15
Subgroup 2 ⁴					
Mechanical Shock	2002	Condition B			
Vibration Variable ⁴ Freq.	2007	Condition A			
Constant Acceleration	2001	Condition E			
Critical Electrical Parameters	5004	25°C, DC	10	15	15
Subgroup 3					
Salt Atmosphere	1009	Condition A Omit Initial Conditioning	10	15	15
Subgroup 4 ⁴					
High Temp. Storage	1008	150°C, 1000 Hrs.			
Critical Electrical Parameters	5004	25°C, DC	7	7	7
Subgroup 5 ⁴					
Operating Life Test	1005	125°C, 1000 Hrs. Minimum			
Critical Electrical Parameters		25°C, DC	5	5	5

1. Also applicable for Level II.

2. Bond strength test may be performed on
samples randomly selected immediately
following internal visual prior to sealing

3. See footnote 1 in Table I

4. See footnote 2 in Table I

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5.0 PREPARATION FOR DELIVERY

5.1 Final Visual Shipping Inspection

Each lot of microcircuits and its associated documentation shall be sampled by Quality Control and visually inspected for the following:

- a) Scratched, nicked or bent leads
- b) Damaged header (packages)
- c) All test data specified in section 4.0
- d) Certificate of Compliance as specified in section 4.0
- e) All other pertinent documentation required and specified by this specification.

5.2 Packing Requirements

Parts shall be packed in containers of the type, size, and kind commonly used which will ensure acceptance by common carriers and safe delivery at the destination and in accordance with MIL-M-55565, Level C. The containers shall be clearly marked with manufacturer's name or symbol. The manufacturer's FEDERAL SUPPLY CODE FOR MANUFACTURER (FSCM) shall be included if applicable.

5.3 Preservation and Package Identification

The package shall be marked with the following:

The country of origin if other than U.S.A.

Procuring activity parts number

Purchase order number

Material nomenclature

Quantity

Lot number

Date code

This information shall appear on the label or shall be directly marked on each container. Method is optional.

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TABLE III
CIRCUIT TECHNOLOGIES APPLICABLE TO
PRECAP INSPECTION PER PARAGRAPH 4.3.14

CIRCUIT TECHNOLOGY	MINIMUM COMPLEXITY CRITERIA
TTL and CMOS	200 components or 100 transistors
MOS and bipolar memories	275 transistors
Linear and interface	150 components or chip area of 7500 square mils

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6.0 NOTES

6.1 Precap Visual Method 2010.1

The following precap criteria may be in conflict with the circuit design topology and construction techniques of some microcircuit manufacturers. Where such a conflict does exist, the inspection criteria listed herein may be waived. (Reference paragraph 3.0 of MIL-STD-883, Method 2010.1)

6.1.1 Preseal Visual Inspection, Test Condition B [38510C and 38510C (Levels I and III)] .

6.1.1.1 Paragraph 3.2.1.7(b) delete the 40 percent perimeter requirement (selected devices only).

6.1.1.2 Paragraph 3.2.4.3(a) substitute the following criteria: "Bonds placed so that the wire exiting from the bond appears to come closer than two wire diameters to another wire, bonding pad, or package land, after a distance of 10 mils from the die surface.

6.1.1.3 Paragraph 3.2.4.3(c) delete. (Applicable to gold ball bonds only) "Bond in the fillet area (or the point where metallizations exit from the bonding pad) which do not exhibit a line of undisturbed metallization visible between the periphery of the bond and at least one side of the fillet (or one side of the connecting stripe) when viewed from above."

6.1.1.4 Paragraphs 3.2.1.1 and 3.2.1.2 are clarified as follows: when a bimetallic system is used (e.g., moly-gold), the scratch or void must penetrate entirely through the gold and expose moly or oxide.

6.1.2 Preseal Visual Inspection, Level II and Table III MSI and LSI circuits.

The same comments of 6.1.1 are applicable here plus the following:

6.1.2.1 Paragraph 3.2.1.1 and 3.2.1.2 delete and replace with: "Scratches or voids in the metallized lead exposing oxide for more than 50% of the lead width or 0.5 mils, whichever is less. Excluded from this criteria are peripheral ground metallization which may contain the defect for a maximum of 50% of its width. Bonding pad scratches or voids are acceptable provided a metal path equal to 1/2 of the width of the connecting lead exists between the bond and the lead."

6.1.2.2 Paragraph 3.2.2 delete.

6.1.2.3 Paragraph 3.2.3 delete and replace with: "Any chip or crack that intersects or crosses active metallization. Excluded from this criteria are peripheral ground metallization which may contain the defect for a maximum of 50% of its width."

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- 6.1.2.4 Paragraph 3.2.4.3(a) delete and replace with: "For all bonds, a minimum of 2 mils separation between the bond wire and other wires, metallization stripes and edge of die. For ultrasonic bonds, this criteria will apply after a distance of 10 mils from the die surface."

Paragraph 3.2.4.3(c) delete.

Paragraph 3.2.4.3(d) delete and replace with: Wire tails which exceed 2 mils in length at the pad or 4 mils in length at the post.

- 6.1.2.5 Paragraph 3.2.5(d) delete.

- 6.1.2.6 Paragraph 3.2.6.1 delete and replace with: "Attached bonding wire or ball inside cavity, or on bar which exceeds one mil in length dimension. All unattached metallic particles or silicon chips."

- 6.1.2.7 Paragraph 3.2.6.2(c) delete.

6.2 Interconnections

Circuit intraconnections (metallization pattern) shall be designed so that no properly fabricated connection shall experience a current density greater than 5×10^5 amperes/cm², including allowances for worst-case conductor composition, normal production tolerances on design dimensions, and nominal thickness at critical areas such as contact windows.

6.3 Burn-in Method 1015

The requirement to return the device to 25°C room ambient temperature with bias still applied should be omitted. Indications are that for most saturated logic integrated circuits, the high temperature bake after bias has been removed does not allow defective devices to recover and become good.

6.4 Salt Atmosphere Test, Method 1009

Where package design considerations necessitate (such as .75" tip-to-tip metal flat packs), there may be a conformal coating applied prior to the salt atmosphere test.

JAN MIL-M-38510

Integrated Circuits

JAN MIL-M-38510 INTEGRATED CIRCUITS

The Texas Instruments JAN MIL-M-38510 Program provides production availability of Hi-Rel JAN ICs. MIL-M-38510 and MIL-STD-883 have been fully implemented to provide a broad product line of JAN microcircuits for both military original equipment and logistic requirements. When the contract specifies that JAN ICs be used, or that microcircuits shall meet the quality provisions of MIL-M-38510, rely on the industry's broadest line of JAN ICs.

Table I provides a convient cross reference from the JAN part number to the corresponding standard catalog part numbers for ease in locating the commercial equivalent. The cross reference from the catalog numbers to the JAN slash sheet numbers is provided in Table II.

The following figure defines the reliability classes of MIL-M-38510 JAN ICs, and the intended areas of application. MIL-M-38510 recommends that for original equipment complements, the device class appropriate to the need be used, while Class B is recommended for spare parts for logistic support.

RECOMMENDED USE	TYPICAL SYSTEM APPLICATIONS	MIL-STD-883 MIL-M-38510 CLASS
Where repair or replacement is readily accomplished and "down time" is not critical	Prototype, noncritical ground systems	Class C
Where repair or replacement is difficult or impossible and reliability is vital	Avionics systems, space satellite	Class B
Where repair or replacement is difficult or impossible and reliability is imperative	Manned Space Program- NASA	Class A

JAN RECOMMENDED USAGE

When system designs utilize ICs not listed on the QPL, for which no slash sheets exist, the TI 38510/MACH IV Program may be used as the detail procurement specification. The 38510/MACH IV Program implements the processing and screening requirements of MIL-M-38510 and MIL-STD-883, and is intended as a supplement to the JAN slash sheets. For more information on the 38510/MACH IV Proqurement Specification, see Tab Section 8.

The complete JAN part number with the tables of class, case, and lead finish codes are given in Table III, along with a cross reference to the TI 38510/MACH IV part numbers. A table of standard TI JAN-qualified cases and lead finishes is also provided to assist in specifying the proper JAN part number. It is imperative that the proper case and lead finish shown in the table be specified on the parts list and procurement documentation. The specific package for each device is determined by referring to the proper data sheet.

The following military documents (see Note 1) establish the processing, quality, and reliability assurance requirements for JAN integrated circuits. The detail requirements of each individual JAN device are specified in the slash sheets.

MIL-M-38510/XXX, Microcircuits, Digital, TTL,
Monolithic Silicon (Slash Sheets)

MIL-M-38510, Microcircuits, General Specification for

MIL-STD-883, Test Methods and Procedures for Microelectronics

QPL-38510, Qualified Products List for MIL-M-38510

NOTE 1: Copies of these documents may be requested from the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, Pa. 19120.

JAN MIL-M-38510 INTEGRATED CIRCUITS

MARCH 1974

TABLE I. JAN INTEGRATED CIRCUITS AND CIRCUIT-TYPE CROSS-REFERENCE

JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE
00101	5430	01403	54153	05001	4011A
00102	5420	01404	9309	05002	4012A
00103	5410	01405	54157 (9322)	05003	4023A
00104	5400	01406†	54151	05101	4013A
00105	5404	01501	5475	05102	4027A
00106	5412	01502	5477	05201	4000A
00107	5401	01503	54116 (9308)	05202	4001A
00108	5405	01504	9314‡	05203	4002A
00109	5403	01601	5408	05204	4025A
00201	5472	01602	5409	05301	4007A
00202	5473	01701	54174	05302	4019A
00203	54107	01702	54175	05401	4008A
00204	5476	02001	54L30	05501	4009A
00205	5474	02002	54L20	05502	4010A
00206	5470	02003	54L10	05503	4049A
00207	5479‡	02004	54L00	05504	4050A
00301	5440	02005	54L04	05601	4017A
00302	5437	02006	54L01/54L03	05602	4018A
00303	5438	02101	54L71	05603	4020A
00401	5402	02102	54L72	05604	4022A
00402	5423	02103	54L73	05605	4024A
00403	5425	02104	54L78	05701	4006A
00404	5427	02105	54L74	05702	4014A
00501	5450	02201	54H72	05703	4015A
00502	5451	02202	54H73	05704	4021A
00503	5453	02203	54H74	05705	4031A
00504	5454	02204	54H76	05801†	4016A
00601	5482	02205	54H101	06001‡	10501‡
00602	5483	02206	54H103	06002‡	10502‡
00603	9304‡	02301	54H30	06003‡	10505‡
00701	5486	02302	54H20	06004‡	10506‡
00801	5406	02303	54H10	06005‡	10507‡
00802	5416	02304	54H00	06006†	10509‡
00803	5407	02305	54H04	07001	54S00
00804	5417	02306	54H01	07002	54S03
00901	5495	02307	54H22	07003	54S04
00902	5496	02401	54H40	07004	54S05
00903	54164	02501	54L90	07005	54S10
00904	54165	02502	54L93	07006	54S20
00905	54194	02503†	54L193	07007	54S22
00906	54195	02504†	93L10	07008	54S30
00907†	9300‡	02505†	93L16	07009	54S133
00908†	9328	02601	54L86	07010	54S134
00909†	54198	02701	54L02	07101†	54S74
00910†	54166	02801	54L95	07102†	54S112
01001	5442	02802	54L164	07103†	54S113
01002	5443	02803†	93L28‡	07104†	54S114
01003	5444	02806*	54L91	07105†	54S174
01004	5445	02901	54L42	07106†	54S175
01005	54145	02902	54L43	07201†	54S40
01006	5446	02903	54L44	07301†	54S02
01007	5447	02904	54L46	07401†	54S51
01008	5448	02905	54L47	07402†	54S64
01009	5449	03001	15930	07403†	54S65
01101	54181	03002	15935	07501†	54S86
01102†	54182 (9342)	03003	15936	07502†	54S135
01201	54121	03004	15946	07601†	54S194
01202	54122	03005	15962	07602†	54S195
01203	54123	03501†	MH0026	07701†	54S138
01301	5492	04001	54H50	07702†	54S139
01302	5493	04002	54H51	07703†	54S280
01303	54160	04003	54H53	07801†	54S181
01304	54163	04004	54H54	07802†	54S182
01305	54162	04005	54H55	07901†	54S151
01306	54161	04101	54L51	07902†	54S153
01307	5490	04102	54L54	07903†	54S157
01308	54182	04103	54L55	07904†	54S158
01309	54193	04104*	54L54	07905†	54S251
01401	54150	04201*	54L121	07906†	54S257
01402	9312‡	04202*	54L122	07907†	54S258

NOTE: Only the basic JAN and SN numbers are shown. Complete the numbers as shown in Table III.

†Slash sheets not released as of date of this publication.

‡Not recommended for new designs.

*Class S only.

JAN MIL-M-38510 INTEGRATED CIRCUITS

MARCH 1974

TABLE I. JAN INTEGRATED CIRCUITS AND CIRCUIT-TYPE CROSS-REFERENCE

JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE
08001†	54S11	10301	52710	10405	55113
08002†	54S15	10302	52711	10501†	52733
08101†	54S140	10303	52106	10601	LM102‡
08201†	54S85	10304	52111	10602	52110
10101	52741	10401	55107	10701	52109
10102	52747	10402	55108	20101	54186 (FROM 512)
10103	52101A	10403	55114 (9614)	20102	MCM5304‡
10104	52108A	10404	55115 (9615)	20201†	54S387 (FROM 1024)
10201	52723				

TABLE II. CIRCUIT-TYPE AND JAN INTEGRATED CIRCUITS CROSS-REFERENCE

CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.
4000A	05201	5425	00403	54186	20101
4001A	05202	5427	00404	54192	01308
4002A	05203	5430	00101	54193	01309
4006A	05701	5437	00302	54194	00905
4007A	05301	5438	00303	54195	00906
4008A	05401	5440	00301	54198	00909†
4009A	05501	5442	01001	54H00	02304
4010A	05502	5443	01002	54H01	02306
4011A	05001	5444	01003	54H04	02305
4012A	05002	5445	01004	54H10	02303
4013A	05101	5446	01006	54H20	02302
4014A	05702	5447	01007	54H22	02307
4015A	05703	5448	01008	54H30	02301
4016A	05801†	5449	01009	54H40	02401
4017A	05601	5450	00501	54H50	04001
4018A	05602	5451	00502	54H51	04002
4019A	05302	5453	00503	54H53	04003
4020A	05603	5454	00504	54H54	04004
4021A	05704	5470	00206	54H55	04005
4022A	05604	5472	00201	54H72	02201
4023A	05003	5473	00202	54H73	02202
4024A	05605	5474	00205	54H74	02203
4025A	05204	5475	01501	54H76	02204
4027A	05102	5476	00204	54H101	02205
4031A	05705	5477	01502	54H103	02206
4049A	05503	5479‡	00207	54L00	02004
4050A	05504	5482	00601	54L01	02006
52101A	10103	5483	00602	54L02	02701
52106	10303	5486	00701	54L03	02006
52108A	10104	5490	01307	54L04	02005
52109	10701	5492	01301	54L10	02003
52110	10602	5493	01302	54L20	02002
52111	10304	5495	00901	54L30	02001
52710	10301	5496	00902	54L42	02901
52711	10302	54107	00203	54L43	02902
52723	10201	54116	01503	54L44	02903
52733	10501†	54121	01201	54L46	02904
52741	10101	54122	01202	54L47	02905
52747	10102	54123	01203	54L51	04101
5400	00104	54145	01005	54L54	04102, 04104*
5401	00107	54150	01401	54L55	04103
5402	00401	54151	01406†	54L71	02101
5403	00109	54153	01403	54L72	02102
5404	00105	54157	01405	54L73	02103
5405	00108	54160	01303	54L74	02105
5406	00801	54161	01306	54L78	02104
5407	00803	54162	01305	54L86	02601
5408	01601	54163	01304	54L90	02501
5409	01602	54164	00903	54L91	02806*
5410	00103	54165	00904	54L93	02502
5412	00106	54166	00910†	54L95	02801
5416	00802	54174	01701	54L121	04201*
5417	00804	54175	01702	54L122	04202*
5420	00102	54181	01101	54L164	02802
5423	00402	54182	01102†	54L193	02503‡

NOTE: Only the basic JAN and SN numbers are shown. Complete the numbers as shown in Table III.

†Slash sheets not released as of date of this publication.

‡Not recommended for new designs.

*Class S only.

JAN MIL-M-38510 INTEGRATED CIRCUITS

MARCH 1974

TABLE II. CIRCUIT-TYPE AND JAN INTEGRATED CIRCUITS CROSS-REFERENCE

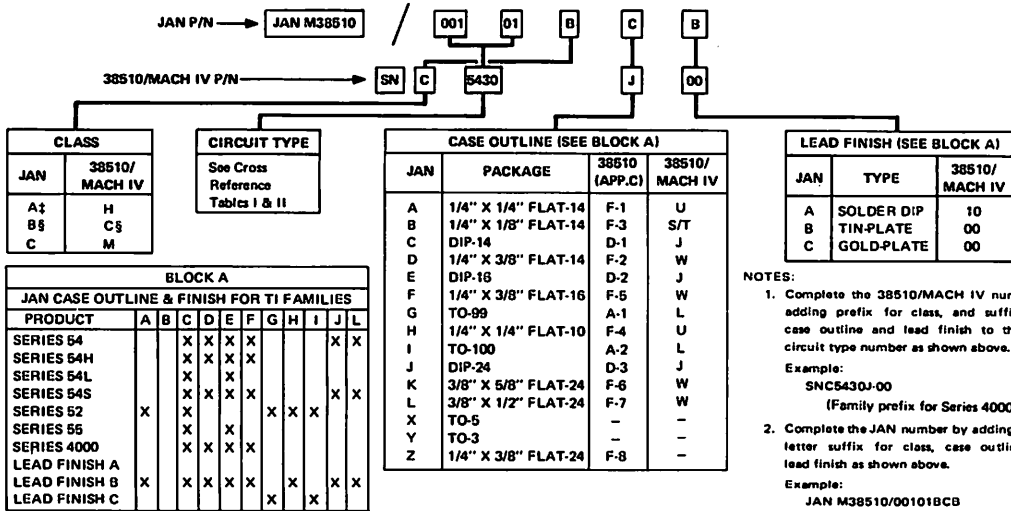
CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.
54S00	07001	54S140	08101†	9314‡	01504
54S02	07301†	54S151	07901†	9322	01405
54S03	07002	54S153	07902†	9328	00908†
54S04	07003	54S157	07903†	9342	01102†
54S05	07004	54S158	07904†	93L10	02504†
54S10	07005	54S174	07105†	93L16	02505†
54S11	08001†	54S175	07106†	93L28‡	02803†
54S15	08002†	54S181	07801†	9614	10403
54S20	07006	54S182	07802†	9615	10404
54S22	07007	54S194	07601†	10501‡	06001†
54S30	07008	54S195	07602†	10502‡	06002†
54S40	07201†	54S251	07905†	10505‡	06003†
54S51	07401†	54S257	07906†	10506‡	06004†
54S64	07402†	54S258	07907†	10507‡	06005†
54S65	07403†	54S280	07703†	10509‡	06006†
54S74	07101†	54S387	20201†	15930	03001
54S85	08201†	55107	10401	15935	03002
54S86	07501†	55108	10402	15936	03003
54S112	07102†	55113	10405	15946	03004
54S113	07103†	55114	10403	15962	03005
54S114	07104†	55115	10404	LM102‡	10801
54S133	07009	9300‡	00907†	MCM5304‡	20102
54S134	07010	9304‡	00603	MH0026	03501†
54S135	07502†	9308	01503	PROM512	20101
54S138	07701†	9309	01404	PROM1024	20201
54S139	07702†	9312‡	01402		

NOTE: Only the basic JAN and SN numbers are shown. Complete the numbers as shown in Table III.

‡Slash sheets not released as of date of this publication.

‡Not recommended for new designs.

TABLE III. TI JAN AND 38510/MACH IV INTEGRATED CIRCUITS†



‡Wide acceptance of JAN class B and 38510/MACH IV SNC integrated circuits have made possible improved availability thru distributor and factory stocking programs.

†For JAN Class A, Class S, and SNH contact Dallas plant.

‡Texas Instruments 38510/MACH IV program is TI's high reliability integrated circuits program designed as a supplement to JAN, and where specified circuit types are not covered by JAN Slash Sheets. The 38510/MACH IV devices utilize hi-rel IC chips from the same TI MIL-M-38510 qualified process and facility as JAN, and are assembled, processed and screened to the same specifications. Federal Stock numbers have been issued for many device types in JAN and 38510/MACH IV in FSC class 5962.

Errata for The TTL Data Book

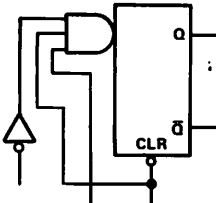

1

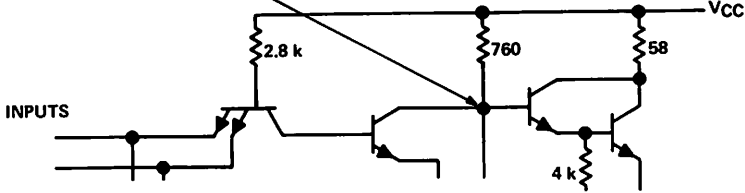
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Errata for
The TTL Data Book for Design Engineers
CC-411

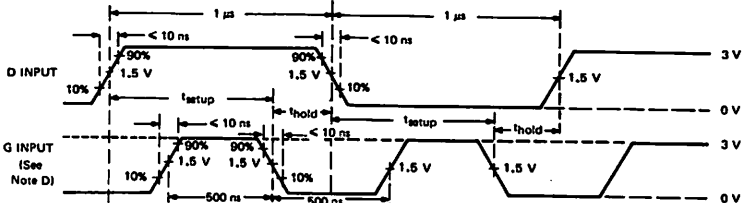
PAGE	LOCATION: AFFECTED TYPES	CHANGE									
16	1st Column: SN54L11, SN54LS11	Change SN54L11 to SN54LS11.									
23	Center Table: 'S140, '128	Interchange (in their entirety) the two entires under "Description".									
25	Last line in table: SN5470, SN7470	Change 0t under "HOLD (ns)" to read 5t.									
50,54 ★	24-Pin W Package Outline	<p>Change the label on the lead thickness dimension to reflect 24 leads.</p> <div><div><div><div>0.006 0.003</div><div>24 LEADS (See Note e)</div><div>PAGE 50</div></div><div><div>0.152 0.077</div><div>24 LEADS (See Note e)</div><div>PAGE 54</div></div></div></div>									
51,55 ★	24-Pin J Ceramic Package Outline	<p>At the right end of the side view, change the dimension controlling height.</p> <table><thead><tr><th></th><th>PAGE 51 (INCHES)</th><th>PAGE 55 (mm)</th></tr></thead><tbody><tr><td>FROM</td><td>0.200 0.150</td><td>5.08 3.81</td></tr><tr><td>TO</td><td>0.225 0.150</td><td>5.72 3.81</td></tr></tbody></table>		PAGE 51 (INCHES)	PAGE 55 (mm)	FROM	0.200 0.150	5.08 3.81	TO	0.225 0.150	5.72 3.81
	PAGE 51 (INCHES)	PAGE 55 (mm)									
FROM	0.200 0.150	5.08 3.81									
TO	0.225 0.150	5.72 3.81									
52,56 ★	16-Pin N Package Outline	<p>Anotate these outlines to indicate that the package configuration is at the option of TI.</p> <p>The corrected drawing for page 52 is shown here complete; the same changes apply to the metric version on page 56.</p> <div><div><p>16-PIN N PLASTIC DUAL-IN-LINE PACKAGE OUTLINE</p><p>INCH PAGE 52</p><p>Package configuration of 16-pin N package (see alternative sideviews) is at the option of TI.</p></div></div>									

*Corrections on these pages have been incorporated in the revised data sheets that appear in this supplement.

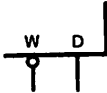
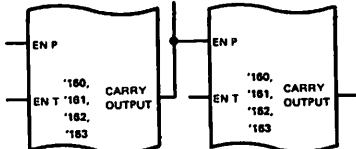
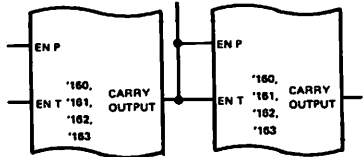
PAGE	LOCATION: AFFECTED TYPES	CHANGE																																																																																																																											
75	Function Table: '70	In the function table under CLOCK INPUT, change the first two entries from "X" to "L". Under positive logic add: "Preset or clear function can occur only when the clock input is low."																																																																																																																											
82	Pinout: '123, 'L123	<p>Add an input to the AND gate for the first multivibrator and connect it to the CLR input.</p> 																																																																																																																											
82	Notes: '121, '122, '123, 'L121, 'L122, 'L123	Change note C to read: "C. An external timing capacitor may be connected between C _{ext} (positive for '121 and 'L121) and R _{ext} /C _{ext} (positive for '122, '123, 'L122, and 'L123).																																																																																																																											
92	Electrical characteristics: 'LS27	Change the two MIN values of V _{OH} from 2.5 and 2.7 to 2.4 for both. This change does not affect 'LS02.																																																																																																																											
93	Supply current table: 'S260	Change TYP and MAX values currently shown as 20 and 35 to read 26 and 45 respectively.																																																																																																																											
	Switching characteristics: 'S260	Add MAX values: t _{PLH} = 5.5 and t _{PHL} = 6 and change the 3.5 TYP values to read 4; delete "*" 3 places and "Tentative data".																																																																																																																											
95	Supply current table: 'LS08	Change under I _{CC} H, the MAX value from 4.4 to 4.8, under I _{CCL} , the TYP value from 6.8 to 4.4.																																																																																																																											
99	Schematic: 'S132	<p>The two input diodes should be non-Schottky:</p> 																																																																																																																											
103	Supply current table: 'S40	<p>Last line entry of table should read:</p> <table><tr><th>TYPE</th><th>TYP</th><th>MAX</th><th>TYP</th><th>MAX</th><th>TYP</th></tr><tr><td>'S40</td><td>10</td><td>18</td><td>25</td><td>44</td><td>8.75</td></tr></table>	TYPE	TYP	MAX	TYP	MAX	TYP	'S40	10	18	25	44	8.75																																																																																																															
TYPE	TYP	MAX	TYP	MAX	TYP																																																																																																																								
'S40	10	18	25	44	8.75																																																																																																																								
106	Electrical characteristics: 'LS33, 'LS38	Change the MAX value of I _{OH} from 100 μA to 250 μA.																																																																																																																											
110	Electrical characteristics: 'LS54	Change the two MIN values of V _{OH} from 2.5 and 2.7 to 2.4 for both. This change does not affect 'LS51 and 'LS55.																																																																																																																											
114	Electrical characteristics using expander inputs: '23, '50, 'H50	<p>Revise first three entries for "I_X(mA)" and "V_{BE(Q)} (V)" to read as follows:</p> <table><tr><th rowspan="2">TYPE</th><th rowspan="2">TEST CONDITIONS</th><th colspan="3">I_X (mA)</th><th rowspan="2">TEST CONDITIONS</th><th colspan="3">V_{BE(Q)} (V)</th></tr><tr><th>MIN</th><th>TYP†</th><th>MAX</th><th>MIN</th><th>TYP†</th><th>MAX</th></tr><tr><td>SN5423</td><td>V_{XX} = 0.4 V,</td><td></td><td></td><td>-3.5</td><td>I_X + I_X = 410 μA,</td><td></td><td></td><td></td></tr><tr><td>SN5450</td><td>I_{OL} = 16 mA,</td><td></td><td></td><td>-2.9</td><td>R_{XX} = 0,</td><td></td><td></td><td>1.1</td></tr><tr><td>SN5453</td><td>See Figure 10</td><td></td><td></td><td>-2.9</td><td>I_{OL} = 16 mA,</td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td>See Figure 11</td><td></td><td></td><td></td></tr><tr><td>SN7423</td><td>V_{XX} = 0.4 V,</td><td></td><td></td><td>-3.5</td><td>I_X + I_X = 620 μA,</td><td></td><td></td><td></td></tr><tr><td>SN7450</td><td>I_{OL} = 16 mA,</td><td></td><td></td><td>-3.1</td><td>R_{XX} = 0,</td><td></td><td></td><td>1</td></tr><tr><td>SN7453</td><td>See Figure 10</td><td></td><td></td><td>-3.1</td><td>I_{OL} = 16 mA,</td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td>See Figure 11</td><td></td><td></td><td></td></tr><tr><td>SN54H50,</td><td>V_{XX} = 1.4 V,</td><td></td><td></td><td>-5.85</td><td>I_X + I_X = 700 μA,</td><td></td><td></td><td></td></tr><tr><td>SN54H53,</td><td>I_X = 0,</td><td></td><td></td><td></td><td>R_{XX} = 0,</td><td></td><td></td><td>1.1</td></tr><tr><td>SN54H55</td><td>I_{OL} = 0,</td><td></td><td></td><td></td><td>I_{OL} = 20 mA,</td><td></td><td></td><td></td></tr><tr><td></td><td>See Figure 10</td><td></td><td></td><td></td><td>See Figure 11</td><td></td><td></td><td></td></tr></table>	TYPE	TEST CONDITIONS	I _X (mA)			TEST CONDITIONS	V _{BE(Q)} (V)			MIN	TYP†	MAX	MIN	TYP†	MAX	SN5423	V _{XX} = 0.4 V,			-3.5	I _X + I _X = 410 μA,				SN5450	I _{OL} = 16 mA,			-2.9	R _{XX} = 0,			1.1	SN5453	See Figure 10			-2.9	I _{OL} = 16 mA,									See Figure 11				SN7423	V _{XX} = 0.4 V,			-3.5	I _X + I _X = 620 μA,				SN7450	I _{OL} = 16 mA,			-3.1	R _{XX} = 0,			1	SN7453	See Figure 10			-3.1	I _{OL} = 16 mA,									See Figure 11				SN54H50,	V _{XX} = 1.4 V,			-5.85	I _X + I _X = 700 μA,				SN54H53,	I _X = 0,				R _{XX} = 0,			1.1	SN54H55	I _{OL} = 0,				I _{OL} = 20 mA,					See Figure 10				See Figure 11			
TYPE	TEST CONDITIONS	I _X (mA)			TEST CONDITIONS	V _{BE(Q)} (V)																																																																																																																							
		MIN	TYP†	MAX		MIN	TYP†	MAX																																																																																																																					
SN5423	V _{XX} = 0.4 V,			-3.5	I _X + I _X = 410 μA,																																																																																																																								
SN5450	I _{OL} = 16 mA,			-2.9	R _{XX} = 0,			1.1																																																																																																																					
SN5453	See Figure 10			-2.9	I _{OL} = 16 mA,																																																																																																																								
					See Figure 11																																																																																																																								
SN7423	V _{XX} = 0.4 V,			-3.5	I _X + I _X = 620 μA,																																																																																																																								
SN7450	I _{OL} = 16 mA,			-3.1	R _{XX} = 0,			1																																																																																																																					
SN7453	See Figure 10			-3.1	I _{OL} = 16 mA,																																																																																																																								
					See Figure 11																																																																																																																								
SN54H50,	V _{XX} = 1.4 V,			-5.85	I _X + I _X = 700 μA,																																																																																																																								
SN54H53,	I _X = 0,				R _{XX} = 0,			1.1																																																																																																																					
SN54H55	I _{OL} = 0,				I _{OL} = 20 mA,																																																																																																																								
	See Figure 10				See Figure 11																																																																																																																								

PAGE	LOCATION: AFFECTED TYPES:	CHANGE									
116	'H53 CIRCUITS (Schematic at bottom left as viewed in the turned position)	<p>Show omitted connection:</p> 									
117	Electrical characteristics: '60	<p>Change "TEST CONDITIONS" for two parameters as indicated below:</p> <table border="1"> <thead> <tr> <th>PARAMETER</th><th>SN5460 TEST CONDITIONS</th><th>SN7460 TEST CONDITIONS</th></tr> </thead> <tbody> <tr> <td>$V_{\bar{X}X(on)}$</td><td>$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_X = 1.1 \text{ V}$, $I_{\bar{X}} = 3.5 \text{ mA}$, $T_A = -55^\circ\text{C}$</td><td>$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_X = 1 \text{ V}$, $I_{\bar{X}} = 3.5 \text{ mA}$, $T_A = 0^\circ\text{C}$</td></tr> <tr> <td>$I_{X(on)}$</td><td>$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_X = 1.1 \text{ V}$, $I_{\bar{X}} = 0$, $T_A = -55^\circ\text{C}$</td><td>NO CHANGE</td></tr> </tbody> </table>	PARAMETER	SN5460 TEST CONDITIONS	SN7460 TEST CONDITIONS	$V_{\bar{X}X(on)}$	$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_X = 1.1 \text{ V}$, $I_{\bar{X}} = 3.5 \text{ mA}$, $T_A = -55^\circ\text{C}$	$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_X = 1 \text{ V}$, $I_{\bar{X}} = 3.5 \text{ mA}$, $T_A = 0^\circ\text{C}$	$I_{X(on)}$	$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_X = 1.1 \text{ V}$, $I_{\bar{X}} = 0$, $T_A = -55^\circ\text{C}$	NO CHANGE
PARAMETER	SN5460 TEST CONDITIONS	SN7460 TEST CONDITIONS									
$V_{\bar{X}X(on)}$	$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_X = 1.1 \text{ V}$, $I_{\bar{X}} = 3.5 \text{ mA}$, $T_A = -55^\circ\text{C}$	$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_X = 1 \text{ V}$, $I_{\bar{X}} = 3.5 \text{ mA}$, $T_A = 0^\circ\text{C}$									
$I_{X(on)}$	$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_X = 1.1 \text{ V}$, $I_{\bar{X}} = 0$, $T_A = -55^\circ\text{C}$	NO CHANGE									
118	Electrical characteristics: 'H60, 'H62	Change unit for the parameter $I_{X(on)}$ from mA to μA .									
121, 125, 127	Switching characteristics: Series 54/74 and 54H/74H flip-flops	Delete the values for all MIN t_{pLH} and t_{pHL} propagation delay time specifications.									
128	Recommended operating conditions: 'L74	Change the MIN value of hold time from 0† to 15†.									
132	Recommended operating conditions: 'S74	Under the 'S74 column delete the "10" and the "12" shown as NOM for the input setup time, t_{setup} .									
134	Description: '121, 'L121	Change 1st line of 4th paragraph to read "Pulse width stability is achieved . . .									
135	Switching characteristics: '121, 'L121	Under the '121 column delete the values for MIN t_{pLH} and t_{pHL} propagation delay time specifications. Also delete the MIN of 20 shown for the $t_{w(out)}$ for the '121 and 'L121.									
136	Figure 4: '121, 'L121	Add conditions: " $V_{CC} = 5 \text{ V}$, $C_T = 60 \text{ pF}$, $R_T = 10 \text{ k}\Omega$ ".									
140	Switching characteristics: '122, '123, 'L122, 'L123	Change MAX value for t_{pLH} (A input to Q output for '122, '123) from 23 ns to 33 ns. Change MAX value of $t_{wQ(min)}$ for 'L123 from 130 to 135 and change MIN value for t_{wQ} from 1.5 to 1.3. Delete all 4 stars in the table and the associated note.									
143	Switching characteristics: 'S134	Delete the values for all MIN specifications (delete "2", two places).									
180 *	Switching characteristics TEST CONDITIONS: '48	<p>Change to read:</p> <p>$C_L = 15 \text{ pF}$, $R_L = 1 \text{ k}\Omega$, See Note 4</p> <p>The same value of R_L applies for both SN5448 and SN7448.</p>									

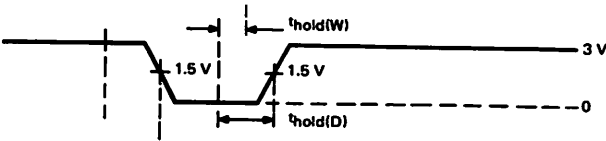
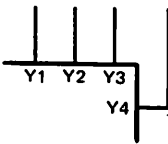
*Corrections on these pages have been incorporated in the revised data sheets that appear in this supplement.

PAGE	LOCATION: AFFECTED TYPES	CHANGE																																
181 ★	Switching characteristics TEST CONDITIONS: '49	Change to read: $C_L = 15 \text{ pF}$, $R_L = 667 \Omega$, See Note 4 The same value of R_L applies for both SN5449 and SN7449.																																
184 ★	Recommended operating conditions: '75, '77	Add: "Data hold time, t_{hold} : MIN = 5 ns".																																
185 ★	Recommended operating conditions: 'L75, 'L77	Add: "Data hold time, t_{hold} : MIN = 10 ns".																																
186 ★	Voltage waveforms: '75, '77, 'L75, 'L77	Add: t_{hold} in two places to existing D and G input waveforms. 																																
198 ★	Note under function table: '83A, 'LS83	Change the note to read "Input conditions at A1, B1, A2, B2, and C0 . . ."																																
218	Electrical characteristics: '88A	Change the maximum value, currently shown as 45 mA for I_{CCL} to read 80 mA.																																
226 ★	Footnote ¶: '90A, '92A, '93A	Footnote ¶ is applicable for Q_A outputs only; therefore, change "¶ Outputs" to "¶ Q_A outputs . . ."																																
228 ★	Footnote ¶: 'L90, 'L93	Footnote ¶ is applicable for Q_A outputs only; therefore, change "¶ Outputs" to "¶ Q_A outputs . . ."																																
239 ★	Recommended operating conditions: '95A	Make the values for $t_w(\text{clock})$ and t_{setup} read as follows: <table><tr><td></td><td colspan="3">SN5495A</td><td colspan="3">SN7495A</td><td></td></tr><tr><td>$t_w(\text{clock})$</td><td>MIN</td><td>NOM</td><td>MAX</td><td>MIN</td><td>NOM</td><td>MAX</td><td>UNIT</td></tr><tr><td>t_{setup}</td><td>20</td><td></td><td></td><td>20</td><td></td><td></td><td>ns</td></tr><tr><td></td><td>15</td><td></td><td></td><td>15</td><td></td><td></td><td>ns</td></tr></table>		SN5495A			SN7495A				$t_w(\text{clock})$	MIN	NOM	MAX	MIN	NOM	MAX	UNIT	t_{setup}	20			20			ns		15			15			ns
	SN5495A			SN7495A																														
$t_w(\text{clock})$	MIN	NOM	MAX	MIN	NOM	MAX	UNIT																											
t_{setup}	20			20			ns																											
	15			15			ns																											
241 ★	Recommended operating conditions: 'LS95A	Change the MIN value of t_{hold} from 0 to 20 in both columns.																																
241 ★	Switching characteristics TEST CONDITIONS: 'LS95A	Change the value of R_L from 400 Ω to 2 k Ω .																																
251	Switching characteristics: '97	Interchange TYP and MAX values to read: <table><tr><th>PARAMETER</th><th>FROM</th><th>TO</th><th>MIN</th><th>TYP</th><th>MAX</th></tr><tr><td>t_{PLH}</td><td rowspan="2">Rate</td><td rowspan="2">Z</td><td rowspan="2"></td><td>6</td><td>10</td></tr><tr><td>t_{PHL}</td><td>9</td><td>14</td></tr></table>	PARAMETER	FROM	TO	MIN	TYP	MAX	t_{PLH}	Rate	Z		6	10	t_{PHL}	9	14																	
PARAMETER	FROM	TO	MIN	TYP	MAX																													
t_{PLH}	Rate	Z		6	10																													
t_{PHL}				9	14																													
260	Recommended operating conditions: '100	ADD: "Data hold time, t_{hold} : MIN = 5 ns"																																
268	FIGURE 5: '120	Change NOTE to read "Input R is low and the unused S input is high."																																
281	Recommended operating conditions: SN74142	Change the minimum value, currently shown as 15 ns, for t_{setup} to read 25 ns.																																
292 ★	Switching characteristics: '147	Change the TYP and MAX values, currently shown as 10 ns and 15 ns respectively, for t_{PHL} (bottom entry), to read 12 ns and 19 ns, respectively.																																

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PAGE	LOCATION: AFFECTED TYPES	CHANGE																																																																																																		
292	Switching characteristics: '148	<p>Change the TYP and MAX values as follows:</p> <p>CURRENTLY SHOWN:</p> <table><thead><tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr></thead><tbody><tr><td>10</td><td>15</td><td></td><td>10</td><td>15</td><td></td><td rowspan="2">ns</td></tr><tr><td>9</td><td>14</td><td></td><td>9</td><td>14</td><td></td></tr><tr><td>13</td><td>19</td><td></td><td>13</td><td>19</td><td></td><td rowspan="2">ns</td></tr><tr><td>10</td><td>15</td><td></td><td>12</td><td>19</td><td></td></tr><tr><td>6</td><td>10</td><td></td><td>6</td><td>10</td><td></td><td rowspan="2">ns</td></tr><tr><td>9</td><td>14</td><td></td><td>14</td><td>25</td><td></td></tr><tr><td>14</td><td>21</td><td></td><td>18</td><td>30</td><td></td><td rowspan="2">ns</td></tr><tr><td>12</td><td>18</td><td></td><td>14</td><td>25</td><td></td></tr><tr><td>10</td><td>15</td><td></td><td>10</td><td>15</td><td></td><td rowspan="2">ns</td></tr><tr><td>10</td><td>15</td><td></td><td>10</td><td>15</td><td></td></tr><tr><td>8</td><td>12</td><td></td><td>8</td><td>12</td><td></td><td rowspan="2">ns</td></tr><tr><td>10</td><td>15</td><td></td><td>10</td><td>15</td><td></td></tr><tr><td>8</td><td>13</td><td></td><td>10</td><td>15</td><td></td><td rowspan="2">ns</td></tr><tr><td>13</td><td>19</td><td></td><td>17</td><td>30</td><td></td></tr></tbody></table> <p>(Arrows indicate lines changed)</p>	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	10	15		10	15		ns	9	14		9	14		13	19		13	19		ns	10	15		12	19		6	10		6	10		ns	9	14		14	25		14	21		18	30		ns	12	18		14	25		10	15		10	15		ns	10	15		10	15		8	12		8	12		ns	10	15		10	15		8	13		10	15		ns	13	19		17	30	
MIN	TYP	MAX	MIN	TYP	MAX	UNIT																																																																																														
10	15		10	15		ns																																																																																														
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6	10		6	10		ns																																																																																														
9	14		14	25																																																																																																
14	21		18	30		ns																																																																																														
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8	13		10	15		ns																																																																																														
13	19		17	30																																																																																																
294	Terminal assignment drawing: '150	<p>Add inversion indicator for the W output.</p> 																																																																																																		
295	Functional block diagram: '151A, 'LS151, 'S151	Interchange the terminal function callouts for the outputs. Pin (5) is to be "Output Y" and pin (6) is to be "Output W".																																																																																																		
306	Electrical characteristics: SN54LS153	Change the MAX value of V_{IL} from 0.6 to 0.7.																																																																																																		
329 ★	Recommended operating conditions: '160, '161, '162, '163	Change the MIN values, currently shown as 15 ns (two places), for t_{setup} at data inputs A, B, C, D for all types to read 20 ns.																																																																																																		
330 ★	Switching characteristics: '160, '161, '162, '163	<p>Change the TYP and MAX values for the three parameters as shown:</p> <table><thead><tr><th>PARAMETER</th><th>FROM (INPUT)</th><th>TO (OUTPUT)</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr></thead><tbody><tr><td>t_{PLH}</td><td>enable T</td><td>carry</td><td></td><td>11</td><td>16</td><td>ns</td></tr><tr><td>t_{PHL}</td><td>enable T</td><td>carry</td><td></td><td>11</td><td>16</td><td>ns</td></tr><tr><td>t_{PHL}</td><td>clear</td><td>any Q</td><td></td><td>26</td><td>38</td><td>ns</td></tr></tbody></table>	PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT	t_{PLH}	enable T	carry		11	16	ns	t_{PHL}	enable T	carry		11	16	ns	t_{PHL}	clear	any Q		26	38	ns																																																																						
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT																																																																																														
t_{PLH}	enable T	carry		11	16	ns																																																																																														
t_{PHL}	enable T	carry		11	16	ns																																																																																														
t_{PHL}	clear	any Q		26	38	ns																																																																																														
333 ★	Typical application data: '160, '161, '162, '163	<p>Complete the logic connections for the carry circuit between the first two stages as follows:</p> <p>CURRENTLY SHOWN:</p>  <p>CHANGED TO:</p> 																																																																																																		

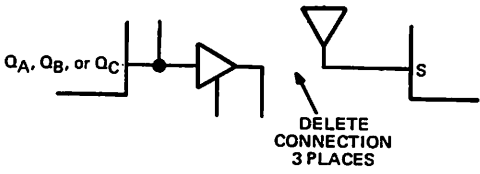
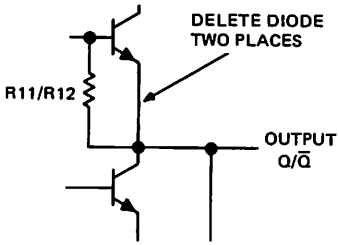
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PAGE	LOCATION: AFFECTED TYPES	CHANGE																													
339	Description: '165	Change first line to read "The SN54165 and SN74165 are 8-bit serial shift . . .". Also change "SN54105" to "SN54165" in the third paragraph.																													
355 ★	Voltage waveforms: '170	Change (invert) the data input waveform: <div><div>DATA INPUT D1, D2, D3, or D4 (See Note A)</div></div>																													
365	Schematic of inputs: 'LS174, 'LS175	For the Clear and D inputs, change the value of R_{eq} from 30 k Ω NOM to 20 k Ω NOM.																													
366	Switching characteristics: '174, '175	Change the TYP and MAX values for t_{PHL} high-to-low-level output from clock (last entry) to read TYP 24 and MAX 35.																													
367	Electrical characteristics: 'LS174, 'LS175	Change the block for I_{IL} under PARAMETER to read: <div><table><tr><td>I_{IL}</td><td>Low-level input current</td><td>Clock, Clear</td></tr><tr><td></td><td></td><td>Data</td></tr></table> Change the values for I_{CC} to read:<table><tr><td></td><td>MIN</td><td>TYP</td><td>MAX</td><td>MIN</td><td>TYP</td><td>MAX</td><td>UNIT</td></tr><tr><td>'LS174</td><td></td><td>16</td><td>26</td><td></td><td>16</td><td>26</td><td rowspan="2">mA</td></tr><tr><td>'LS175</td><td></td><td>11</td><td>18</td><td></td><td>11</td><td>18</td></tr></table></div>	I_{IL}	Low-level input current	Clock, Clear			Data		MIN	TYP	MAX	MIN	TYP	MAX	UNIT	'LS174		16	26		16	26	mA	'LS175		11	18		11	18
I_{IL}	Low-level input current	Clock, Clear																													
		Data																													
	MIN	TYP	MAX	MIN	TYP	MAX	UNIT																								
'LS174		16	26		16	26	mA																								
'LS175		11	18		11	18																									
367	Switching characteristics: 'LS174, 'LS175	Change the TYP and MAX values for t_{PHL} high-to-low-level output from clock (last entry) to read TYP 23 and MAX 35.																													
388	Electrical characteristics TEST CONDITIONS: 'S181	For I_{IH} change the V_I condition from 2.4 V to 2.5 V; for I_{IL} change the V_I condition from 0.4 V to 0.5 V.																													
407	Switching characteristics: '186	Delete the values for all MIN t_{PLH} and t_{PHL} propagation delay time specifications.																													
410	Terminal assignment drawing: '187	Delete the inversion indicators from the four Y outputs: 																													
417	Above description: 'LS190, 'LS191	Change typical power dissipation from 90 mW to 100 mW.																													
423	Electrical characteristics: 'LS190, 'LS191	Change the values for I_{CC} to read: <table><tr><td>TYP</td><td>MAX</td><td>TYP</td><td>MAX</td></tr><tr><td>20</td><td>35</td><td>20</td><td>35</td></tr></table>	TYP	MAX	TYP	MAX	20	35	20	35																					
TYP	MAX	TYP	MAX																												
20	35	20	35																												
425	FIGURE 1: '190, '191, 'LS190, 'LS191	Change the output identifier to read "QA, QB, QC, QD, MAX/MIN, or RIPPLE CLOCK".																													
429	Schematics of inputs: 'LS192, 'LS193	Change "Enable input: $R_{eq} = 8.33$ k Ω NOM" to read "Load input: $R_{eq} = 25$ k Ω NOM".																													

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PAGE	LOCATION: AFFECTED TYPE	CHANGE																
434	Electrical characteristics: 'LS192, 'LS193	Under TEST CONDITIONS for the parameter V_I , change the value of I_I to read -18 mA. Also change the values for I_{CC} to read: <table><tr><td>TYP</td><td>MAX</td><td>TYP</td><td>MAX</td></tr><tr><td>19</td><td>34</td><td>19</td><td>34</td></tr></table>	TYP	MAX	TYP	MAX	19	34	19	34								
TYP	MAX	TYP	MAX															
19	34	19	34															
434	Switching characteristics: 'LS192, 'LS193	Change t_{PHL} on the 3rd and the 5th lines: <table><tr><td colspan="2">FROM</td><td colspan="2">TO</td></tr><tr><td>TYP</td><td>MAX</td><td>TYP</td><td>MAX</td></tr><tr><td>16</td><td>24</td><td>21</td><td>33</td></tr><tr><td>16</td><td>24</td><td>21</td><td>33</td></tr></table>	FROM		TO		TYP	MAX	TYP	MAX	16	24	21	33	16	24	21	33
FROM		TO																
TYP	MAX	TYP	MAX															
16	24	21	33															
16	24	21	33															
435 436	NOTE E NOTE G: 'LS192, 'LS193	Change NOTE E page 435 and NOTE G page 436 to read: " V_{ref} is 1.5 volts for '192 and '193; 1.3 volts for 'L192, 'L193, 'LS192 and 'LS193".																
440 ★	Switching characteristics: '194	Delete the values for the MIN t_{PLH} and t_{PHL} propagation delay time specifications.																
442 ★	Recommended operating conditions: 'S194	Change the MIN values, currently shown as 8 ns (two places), for t_{setup} at mode control to read 11 ns																
442 ★	Electrical characteristics: 'S194	Change the maximum value, currently shown as 1.5 V for " V_I Input clamp voltage" to read -1.2 V in both columns.																
445 ★	Functional block diagram: '195, 'LS195, 'S195	Reverse the pin numbers for J and \bar{K} inputs. J is pin (2) and \bar{K} is pin (3).																
447 ★	Recommended operating conditions: '195	Change the MIN values, currently shown as 15 ns (two places), for t_{setup} at serial and parallel data to read 20 ns.																
447 ★	Switching characteristics: '195	Delete the values for the MIN t_{PLH} and t_{PHL} propagation delay time specifications.																
449 ★	Recommended operating conditions: 'S195	Change the MIN values, currently shown as 8 ns (two places), for t_{setup} at shift/load to read 11 ns.																
455	Electrical characteristics: 'LS196, 'LS197	For I_{IL} , change "Low-level output current" to "Low-level input current".																
462	Switching characteristics: '198, '199	Delete the MIN values for t_{PLH} and t_{PHL} propagation delay time specifications.																
473	Switching characteristics: 'LS251	Change the MAX NO. OF COMMON OUTPUTS from 19 to 49 for SN54LS251 and to 129 for SN74LS251.																
476	Electrical characteristics: 'LS251	Change the MIN limit of V_{OH} , for both types, to read 2.4 instead of 2.5 and 2.7.																
481	Electrical characteristics: 'LS253	Change the MAX value of V_{IL} from 0.6 to 0.7.																
484 ★	Electrical characteristics TEST CONDITIONS 'S257, '285	Change the test condition for V_{OL} that reads " $I_{OH} = 20$ mA" to read " $I_{OL} = 20$ mA".																
497	FIGURE B: '284, '285	The C_n inputs of the SN54S182/SN74S182 in the lower left corner and of the SN54S181/SN74S181 in the lower right corner, each presently grounded, should be connected instead to a high-logic-level voltage.																
503 ★	Recommended operating conditions: 'LS295	Change the MIN value of t_{hold} from 0 to 20 in both columns.																

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PAGE	LOCATION: AFFECTED TYPES	CHANGE															
504 ★	Functional block diagram: 'LS295	<p>Delete connection as follows:</p> 															
521	Description: SN29300, SN39300	In the next to the last line (last paragraph) change "SN29300" to read SN39300".															
569 ★	Beam assignments: BL54LS10Y, BL74LS10Y	<table> <thead> <tr> <th>BEAM</th><th>SHOWN AS</th><th>CHANGE TO</th></tr> </thead> <tbody> <tr> <td>1</td><td>1A</td><td>1Y</td></tr> <tr> <td>2</td><td>1B</td><td>1A</td></tr> <tr> <td>5</td><td>1C</td><td>1B</td></tr> <tr> <td>6</td><td>1Y</td><td>1C</td></tr> </tbody> </table>	BEAM	SHOWN AS	CHANGE TO	1	1A	1Y	2	1B	1A	5	1C	1B	6	1Y	1C
BEAM	SHOWN AS	CHANGE TO															
1	1A	1Y															
2	1B	1A															
5	1C	1B															
6	1Y	1C															
598	Schematic: RSN54H74, RSN74H74	<p>Delete the two diodes at the Q and \bar{Q} outputs as follows:</p> 															

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IC Sockets and Interconnection Panels

IC SOCKETS AND INTERCONNECTION PANELS

Texas Instruments lines of off-the-shelf interconnection products are designed specifically to meet the performance needs of volume commercial applications. They provide both the economy of a standard product line and performance features developed after many year's experience with custom designs. Foremost among these is our ability to selectively bond a wrought gold stripe at the contact point. No waste. Reduced cost. Reliable contacts.

Wrought Gold Contact

Plate a contact with gold and you get a better contact. More reliable, longer lasting. Increase the gold, you improve the contact. But gold is precious, so improved performance has to be costly — right? Wrong. Because now you can get the gold only where it is needed — at the point of contact.

How? With selective metallurgical bonding; a gold stripe inlay. Not porous plating, but durable wrought gold bonded to the contact by the same technology used to produce clad coins and thermostat metals.

Texas Instruments, Attleboro, Massachusetts, is the world's largest producer of these multimetal systems. We also know our way around electronics. The result? A full line of reliable, low cost, interconnection systems featuring an extra measure of gold where it's needed. Premium performance at no premium in price.

IC Sockets

Texas Instruments family of IC sockets includes every type and size in common use today, and as wide a choice of contact materials as you'll find anywhere. Choose from open or closed entry *wire-wrapped*[†] sockets, standard or low profile solder tail sockets, cable plugs, and component platforms. Sizes from 8 to 40 pins.

IC Panels

To match the industry's broadest line of IC sockets TI offers one of the industry's widest selections of off-the-shelf pin and socket panel products. Logic panels. Logic cards. Accessories. Add TI's custom design capability and wire wrapping for full service.

Additional information including pricing and delivery quotations may be obtained from your nearest TI Distributor, TI Representative, or:

Texas Instruments Incorporated
Connector Product Marketing
MS 11-1
Attleboro, Massachusetts 02703
Telephone: (617) 22-2800
TELEX: ABORA927708

[†] Registered trademark of Gardner-Denver

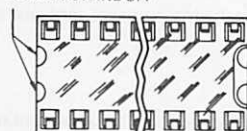
LOW PROFILE SOCKETS

SOLDER TAIL

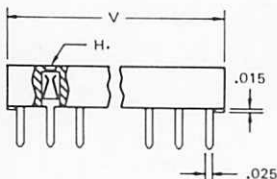
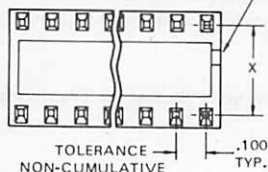
C-93 SERIES GOLD CLAD CONTACTS

- Universal mounting and packaging
- Mylar anti-wicking wafer
- Stand-off tabs on base for solder flush
- Redundant contact points for low contact resistance, high reliability and repetitive insertion
- Closed entry construction

SOLDER STANDOFF



IDENTIFICATION NOTCH FOR PIN NO. 1

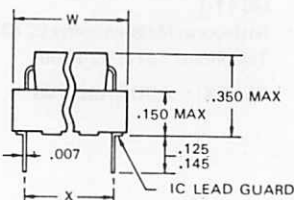


MATERIAL:


- Body-glass filled nylon (GFN)
- Contact-copper nickel alloy
- Finish-see part number schedule

NOTES:

- Sockets meet requirements of Texas Instruments test specification TS-0005 and test report TR-0003
- Operating temperature -65°C to $+150^{\circ}\text{C}$
- Contacts have redundant spring elements
- Accommodates standard IC leads up to .024" square, rectangular, or .024" diameter
- Contact is designed and oriented in the plastic body to generate maximum possible contact pressure
- Socket is designed to achieve maximum density on boards
- Sockets may be mounted end to end on .100" centers continuous line or on .400" centers row to row
- Socket is designed to prevent IC leads from contacting P.C. board
- Closed entry feature provided to facilitate automatic IC insertion and protects the IC leads against damage



PART NO. SCHEDULE

BLACK BODY	
Pins	
8	C930802
14	C931402
16	C931602
18	C931802
22	C932202
24	C932402
28	C932802
40	C934002

CONTACT FINISH
100 microinch min.
gold stripe inlay

	8 Pin	14 Pin	16 Pin	18 Pin	20 Pin	24 Pin	28 Pin	40 Pin
Dimension X $\pm .005$.300	.300	.300	.300	.400	.600	.600	.600
Dimension V $\pm .010$.400	.700	.800	.900	1.100	1.200	1.400	2.000
Dimension W (max)	.400	.400	.400	.400	.500	.700	.700	.700

STANDARD PROFILE SOCKET

WIRE WRAP

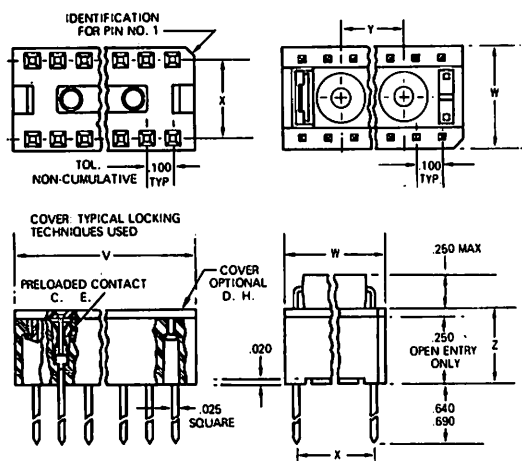
C-82 SERIES PLATED CONTACTS • C-92 SERIES GOLD CLAD CONTACTS

SOLDER TAIL

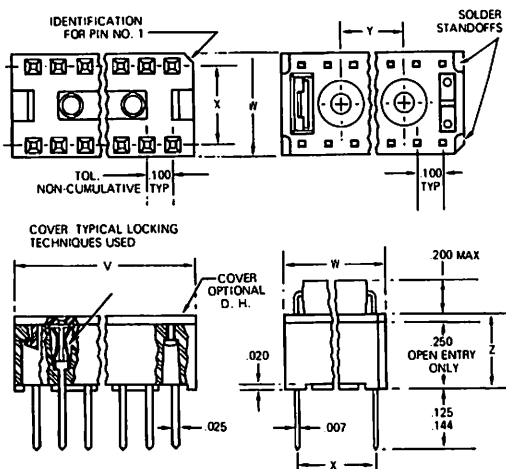
C-81 SERIES PLATED CONTACTS • C-91 SERIES GOLD CLAD CONTACTS

- Designed for low cost, reliable, high density production packaging
- Universal mounting and packaging capabilities
- 8 to 40 pin lead configurations
- Contacts accommodate .015" through .024" rectangular or round dual-in-line leads
- Wire wrap posts held to true position of .015" providing a true position of .020" on boards for efficient automatic wire wrapping

WIRE WRAP



SOLDER TAIL



MATERIAL:

- A. Body-glass filled nylon (GFN)
 B. Contact-phosphor bronze per QQ-B-750 (C-81) copper nickel alloy (C-91)
 C. Finish-see part number schedule





NOTES:

- A. Sockets meet requirements of Texas Instruments test specification TS-0003 and test report TR-0001
 B. Contacts are replaceable
 C. Contacts have redundant spring elements
 D. Cover is removable
 E. Contact is designed and oriented in the plastic body to generate maximum possible contact pressure
 F. Operating temperature -65°C to +150°C





- G. Sockets are designed to achieve maximum density on boards and may be mounted .400" row to row centers
 H. Closed entry cover is provided to facilitate automatic insertion and protect IC leads against damage
 I. Accommodates standard IC leads up to .024" square, rectangular or .024" dia.
 J. Contact retention - 7 lbs. min.
 K. Sockets are capable of being automatically or semiautomatically wire wrapped

	8 Pin	14 Pin	16 Pin	18 Pin	24 Pin	28 Pin	36 Pin	40 Pin
Dimension V $\pm .010$.465	.765	.865	.965	1.280	1.480	1.845	2.045
Dimension W (max)	.400	.400	.400	.400	.700	.700	.700	.700
Dimension X $\pm .005$.300	.300	.300	.300	.600	.600	.600	.600
Dimension Y $\pm .010$	NA	.400	.400	.400	.500	.500	.800	1.000
Dimension Z $\pm .005$.280	.280	.280	.280	.280	.280	.325	.325

WIRE WRAP

		OPEN ENTRY		CLOSED ENTRY	
PART NUMBER SCHEDULE					
Contact Finish	Pins	Black Body	White Body	Black Cover	White Cover
Series C-81 200-400 microinch min tin per MIL-T-10727	8	C810854	C810855	C810804	C810805
	14	C811454	C811455	C811404	C811405
	16	C811654	C811655	C811604	C811605
	18	C811854	C811855	C811804	C811805
	24	C812454	C812455	C812404	C812405
	28	C812854	C812855	C812804	C812805
	36			C813604	C813605
	40			C814004	C814005
Series C-91 50 microinch min gold stripe inlay	8	C910850	C910851	C910800	C910801
	14	C911450	C911451	C911400	C911401
	16	C911650	C911651	C911600	C911601
	18	C911850	C911851	C911800	C911801
	24	C912450	C912451	C912400	C912401
	28	C912850	C912851	C912800	C912801
	36			C913600	C913601
	40			C914000	C914001

SOLDER TAIL

		OPEN ENTRY		CLOSED ENTRY	
PART NUMBER SCHEDULE					
Contact Finish	Pins	Black Body	White Body	Black Cover	White Cover
Series C-82 30 microinch min gold per MIL-G-45204 over 50 microinch min nickel per QQ-N-290	8	C820850	C820851	C820800	C820801
	14	C821450	C821451	C821400	C821401
	16	C821650	C821651	C821600	C821601
	18	C821850	C821851	C821800	C821801
	24	C822450	C822451	C822400	C822401
	28	C822850	C822851	C822800	C822801
	36			C823600	C823601
	40			C824000	C824001
Series C-82 50 microinch min gold per MIL-G-45204 over 100 microinch min nickel per QQ-N-290	8	C820852	C820851	C820802	C820803
	14	C821452	C821453	C821402	C821403
	16	C821652	C821653	C821602	C821603
	18	C821852	C821853	C821802	C821803
	24	C822452	C822453	C822402	C822403
	28	C822852	C822853	C822802	C822803
	36			C823602	C823603
	40			C824002	C824003
Series C-82 200-400 microinch min tin per MIL-T-10727	8	C820854	C820855	C820804	C820805
	14	C821454	C821455	C821404	C821405
	16	C821654	C821655	C821604	C821605
	18	C821854	C821855	C821804	C821805
	24	C822454	C822455	C822404	C822405
	28	C822854	C822855	C822804	C822805
	36			C823604	C823605
	40			C824004	C824005
Series C-92 100 microinch min gold stripe inlay	8	C920850	C920851	C920800	C920801
	14	C921450	C921451	C921400	C921401
	16	C921650	C921651	C921600	C921601
	18	C921850	C921851	C921800	C921801
	24	C922450	C922451	C922400	C922401
	28	C922850	C922851	C922800	C922801
	36			C923600	C923601
	40			C924000	C924001

SOCKET PANELS

STANDARD

D4 SERIES

- **180 position panel or multiples of 30 position with 14 or 16 position socket pattern**
- **I/O — 4 rows with 13 pins per row or 3 - 14 pin sockets**
- **Low cost standard hardware**
- **Available in 98 standard series**
- **Off-the-shelf availability**

SELECT-A-WRAP

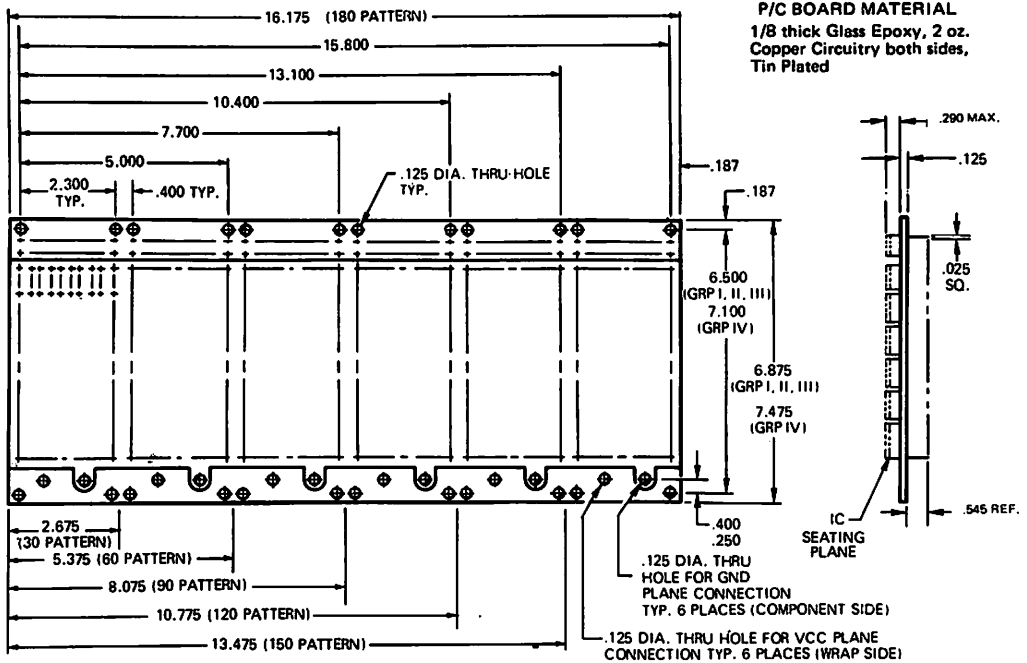
D1 SERIES

- **180 position panel or multiples of 30 position with 14 or 16 position socket pattern**
- **I/O — 2 rows with 23 pins per row or 3 - 14 pin sockets**
- **Low cost standard hardware — no tooling**
- **Available in 98 standard series**
- **Off-the-shelf availability**
- **Uncommitted ground and power pin for custom design**

MULTIPURPOSE

Z3 SERIES / SELECT-A-WRAP

- Assemble your own custom panel with off-the-shelf hardware and sockets or Texas Instruments will assemble to your prints
- Holes on continuous .100 centers within rows .300 centers between rows
- Accepts 8, 14, 16, 18, 24, 28, 36, and 40 pin dual-in-line sockets, discrete component platforms and interfacing plugs
- Any pin may be soldered to power and ground with solder preform and bridging tabs



NOTE: Dimensions shown are nominal. Detail information and tolerances available on request (indicate series and group number).

STANDARD SOCKETS

C-81 or C-91 series, 14 pin or 16 pin, closed entry sockets as designated in the Part No. Schedule at right. See pages 7 and 8 for complete socket information.

C-81 SERIES SOCKETS

Body..... Glass filled nylon
Contact Phosphor bronze per QQ-B-750
Finish 30 microinch min. gold per
MIL-G-45204 *over*
50 microinch min. nickel per
QQ-N-290

C-91 SERIES SOCKETS

Body Glass filled nylon
Contact Copper nickel alloy
Finish 50 microinch min.
gold stripe inlay

STANDARD PANEL PART NO. SCHEDULE -D4 Series

Group No.	I/O Option	Sockets Per Panel	C-81 Sockets	C-91 Sockets
Group I 14 Pin PIN 14 VCC PIN 7 GRD	SOCKETS 	30 60 90 120 150 180	D411211 D411212 D411213 D411214 D411215 D411216	D411231 D411232 D411233 D411234 D411235 D411236
	FEED-THRU PINS 	30 60 90 120 150 180	D411411 D411412 D411413 D411414 D411415 D411416	D411431 D411432 D411433 D411434 D411435 D411436
Group II 14 Pin PIN V VCC PIN G GRD	SOCKETS 	30 60 90 120 150 180	D434211 D434212 D434213 D434214 D434215 D434216	D434231 D434232 D434233 D434234 D434235 D434236
	FEED-THRU PINS 	30 60 90 120 150 180	D434411 D434412 D434413 D434414 D434415 D434416	D434431 D434432 D434433 D434434 D434435 D434436
Group III 16 Pin PIN 16 VCC PIN 8 GRD	SOCKETS 	30 60 90 120 150 180	D423211 D423212 D423213 D423214 D423215 D423216	D423231 D423232 D423233 D423234 D423235 D423236
	FEED-THRU PINS 	30 60 90 120 150 180	D423411 D423412 D423413 D423414 D423415 D423416	D423431 D423432 D423433 D423434 D423435 D423436
Group IV 16 Pin PIN V VCC PIN G GRD	SOCKETS 	30 60 90 120 150 180	D444211 D444212 D444213 D444214 D444215 D444216	D444231 D444232 D444233 D444234 D444235 D444236
	FEED-THRU PINS 	30 60 90 120 150 180	D444411 D444412 D444413 D444414 D444415 D444416	D444431 D444432 D444433 D444434 D444435 D444436

SELECT-A-WRAP PANEL PART NO. SCHEDULE -D1 Series

Group No.	I/O Option	Sockets Per Panel	C-81 Sockets	C-91 Sockets
Group-I 14 Pin VCC and GRD Uncommitted	SOCKETS 	30 60 90 120 150 180	D114211 D114212 D114213 D114214 D114215 D114216	D114231 D114232 D114233 D114234 D114235 D114236
	FEED-THRU PINS 	30 60 90 120 150 180	D114311 D114312 D114313 D114314 D114315 D114316	D114331 D114332 D114333 D114334 D114335 D114336
Group IV 16 Pin VCC and GRD Uncommitted	SOCKETS 	30 60 90 120 150 180	D124211 D124212 D124213 D124214 D124215 D124216	D124231 D124232 D124233 D124234 D124235 D124236
	FEED-THRU PINS 	30 60 90 120 150 180	D124311 D124312 D124313 D124314 D124315 D124316	D124331 D124332 D124333 D124334 D124335 D124336

MULTIPURPOSE PANEL PART NO. SCHEDULE -Z3 Series

I/O Option	Rows	Part No.
no pins 2 x 23 I/O hole pattern	9	Z301100
	18	Z302100
	27	Z303100
	36	Z304100
	45	Z305100
2 x 23 feed-thru pins	54	Z306100
	9	Z301200
	18	Z302200
	27	Z303200
	36	Z304200
	45	Z305200
	54	Z306200

PIN PANELS

STANDARD

D7 SERIES

- Low profile — high density
- Immediate delivery
- Modular construction—1-6 modules per panel—30 patterns per module 14 or 16 pin patterns
- 4 lb minimum strip force
- 10 lb minimum pin push-out force
- Optional I/O interface

SELECT-A-WRAP

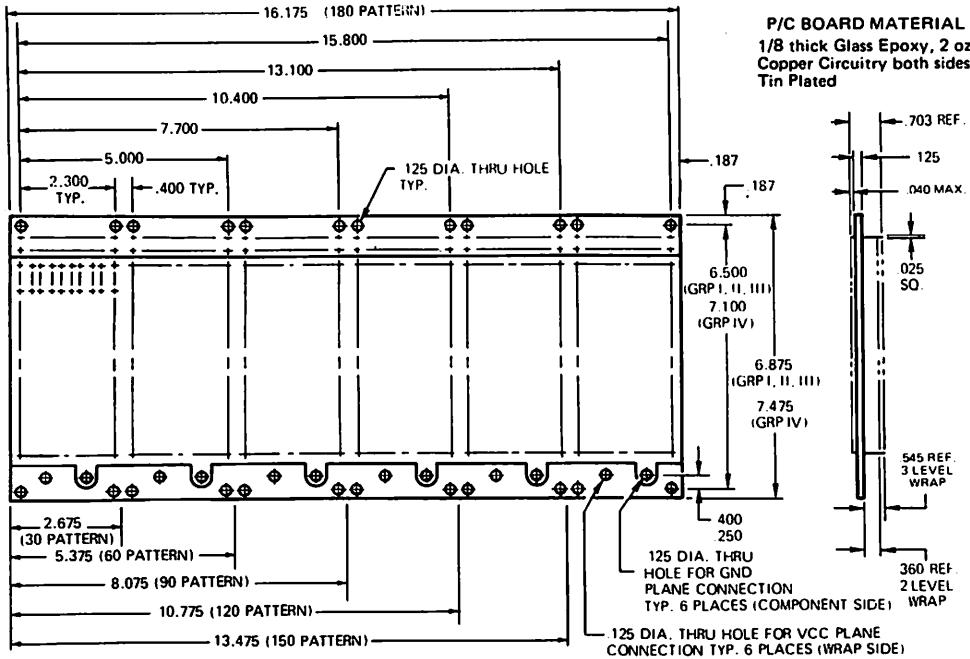
D2 SERIES

- Low cost — no tooling — standard hardware — off-the-shelf availability
- Uncommitted ground and power pin for custom design
- Optional feed-thru pins or pin-in-board terminal for I/O interface
- 4 lb minimum strip force
- 10 lb minimum push-out force

UNIVERSAL

D3 SERIES

- Prototype/production
- Meets automatic wire wrapping tolerances
- Modular construction — up to 6 modules — 9 rows per module
- Accepts 8, 14, 16, 18, 24, 28, 36, and 40 pin dual-in-line packages, discrete component platforms and interfacing plugs



STANDARD PANEL PART NO. SCHEDULE -D7 Series

Group No.	I/O Option	Pos. Per Panel	2 Level Wrap	3 Level Wrap
Group I 14 Pin PIN 14 VCC PIN 7 GRD	PINS	30	D711521	D711511
		60	D711522	D711512
		90	D711523	D711513
		120	D711524	D711514
		150	D711525	D711515
		180	D711526	D711516
	FEED-THRU PINS	30	D711421	D711411
		60	D711422	D711412
		90	D711423	D711413
		120	D711424	D711414
		150	D711425	D711415
		180	D711426	D711416
Group II 14 Pin PIN V VCC PIN G GRD	PINS	30	D734521	D734511
		60	D734522	D734512
		90	D734523	D734513
		120	D734524	D734514
		150	D734525	D734515
		180	D734526	D734516
	FEED-THRU PINS	30	D734421	D734411
		60	D734422	D734412
		90	D734423	D734413
		120	D734424	D734414
		150	D734425	D734415
		180	D734426	D734416
Group III 16 Pin PIN 16 VCC PIN 8 GRD	PINS	30	D723521	D723511
		60	D723522	D723512
		90	D723523	D723513
		120	D723524	D723514
		150	D723525	D723515
		180	D723526	D723516
	FEED-THRU PINS	30	D723421	D723411
		60	D723422	D723412
		90	D723423	D723413
		120	D723424	D723414
		150	D723425	D723415
		180	D723426	D723416
Group IV 16 Pin PIN V VCC PIN G GRD	PINS	30	D744521	D744511
		60	D744522	D744512
		90	D744523	D744513
		120	D744524	D744514
		150	D744525	D744515
		180	D744526	D744516
	FEED-THRU PINS	30	D744421	D744411
		60	D744422	D744412
		90	D744423	D744413
		120	D744424	D744414
		150	D744425	D744415
		180	D744426	D744416

SELECT-A-WRAP PANEL PART NO. SCHEDULE -D2 Series

Group No.	I/O Option	Pos. Per Panel	2 Level Wrap	3 Level Wrap
Group II 14 Pin VCC and GRD Uncommitted	PINS	30	D214421	D214411
		60	D214422	D214412
		90	D214423	D214413
		120	D214424	D214414
		150	D214425	D214415
		180	D214426	D214416
	FEED-THRU PINS	30	D214321	D214311
		60	D214322	D214312
		90	D214323	D214313
		120	D214324	D214314
		150	D214325	D214315
		180	D214326	D214316
Group IV 16 Pin VCC and GRD Uncommitted	PINS	30	D224421	D224411
		60	D224422	D224412
		90	D224423	D224413
		120	D224424	D224414
		150	D224425	D224415
		180	D224426	D224416
	FEED-THRU PINS	30	D224321	D224311
		60	D224322	D224312
		90	D224323	D224313
		120	D224324	D224314
		150	D224325	D224315
		180	D224326	D224316

UNIVERSAL PANEL PART NO. SCHEDULE -D3 Series

PATTERN LAYOUT	I/O Option	Rows	2 Level Wrap	3 Level Wrap
Double sided board with power and ground planes connected to additional wire wrap terminations outside of contact row.	no pins 2 x 23 I/O hole pattern	9	D381501	D381500
		18	D382501	D382500
		27	D383501	D383500
		36	D384501	D384500
		45	D385501	D385500
50 contacts on .100 centers	2 x 23 feed-thru pins	54	D386501	D386500
		9	D381401	D381400
		18	D382401	D382400
		27	D383401	D383400
		36	D384401	D384400
		45	D385401	D385400
		54	D386401	D386400

SOCKET CARDS

STANDARD

DO2 SERIES

- Low Cost
- 14 - 16 pin socket pattern - 60 position
- Standard ground and power pin commitment
- 8 standard designs
- Mates with dual 60 position edge connector

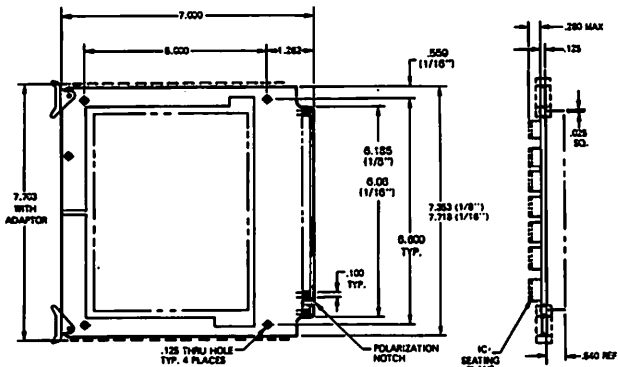
MULTIPURPOSE

DO SERIES/SELECT-A-WRAP

- Assemble your own custom logic cards with off-the-shelf hardware and sockets or Texas Instruments will assemble to your prints
- Accepts 8, 14, 16, 18, 24, 28, 36, and 40 pin dual-in-line packages, discrete component platforms and I/O plugs
- 60 position

P/C BOARD MATERIAL

1/16 and 1/8 thick Glass Epoxy, 2 oz. Copper Circuitry both sides, Tin Plated

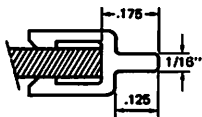


NOTE: Dimensions shown are nominal. Detail information and tolerances available on request (indicate series and group number).

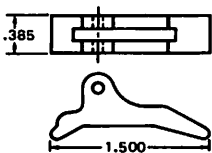
DO2 Series

STANDARD CARD PART NO. SCHEDULE

Group No.	Board Thk.	C-81 Sockets	C-81 Sockets
Group I 14 Pin PIN 14 VCC PIN 7 GRD	1/16"	D022110	D022130
	1/8"	D021110	D021130
Group II 14 Pin PIN V VCC PIN G GRD	1/16"	D022310	D022330
	1/8"	D021310	D021330
Group III 16 Pin PIN 16 VCC PIN 8 GRD	1/16"	D022210	D022230
	1/8"	D021210	D021230
Group IV 16 Pin PIN V VCC PIN G GRD	1/16"	D022410	D022430
	1/8"	D021410	D021430



ADAPTER
Part no. Z501300



EJECTOR KEYS
Material: Nylon
Part no. Z501200 (1/8")
Z501201 (1/16")

DO Series MULTIPURPOSE CARD PART NO. SCHEDULE

I/O	
Board Thk.	Part No.
1/16"	Z012510
1/8"	Z011510

PIN CARDS

STANDARD

DO1 SERIES

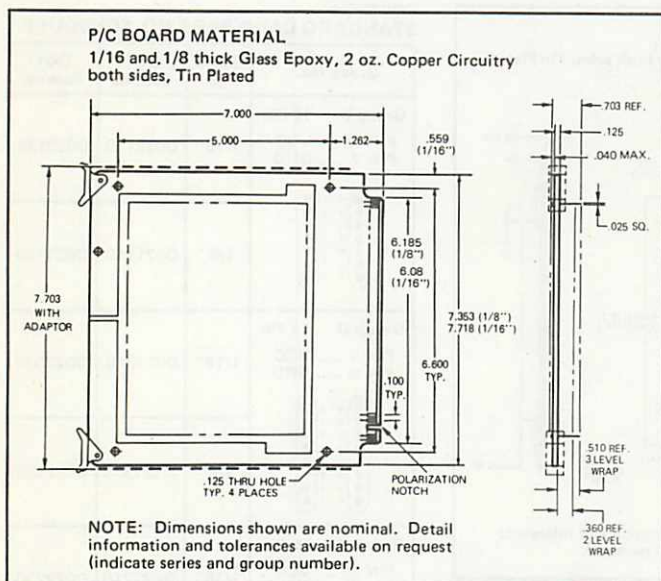
- Low profile — high density
- 14 - 16 pin pattern — 60 position
- 2 sided P/C board with ground and voltage connected to each pattern
- 4 lb minimum strip force
- 10 lb minimum pin push-out force
- Available on 1/16" or 1/8" P/C board

UNIVERSAL

DO1 SERIES

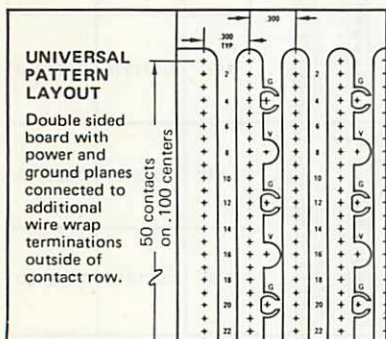
- Universal pattern accepts wide choice of dual-in-line packages
- 20 rows of 50 contacts per row on .100 X .300 grid
- Meets all requirements for automatic wire wrapping
- Available on 1/16" or 1/8" P/C board

High retention 4-leaf beryllium copper spring contacts



DO1 Series STANDARD CARD PART NO. SCHEDULE

Group No.	Board Thk.	2 Level Wrap	3 Level Wrap
Group I 14 Pin PIN 14 VCC PIN 7 GRD 	1/16"	D012120	D012110
	1/8"	D011120	D011110
Group II 14 Pin PIN V VCC PIN G GRD 	1/16"	D012320	D012310
	1/8"	D011320	D011310
Group III 16 Pin PIN 16 VCC PIN 8 GRD 	1/16"	D012220	D012210
	1/8"	D011220	D011210
Group IV 16 Pin PIN V VCC PIN G GRD 	1/16"	D012420	D012410
	1/8"	D011420	D011410



I/O CONFIGURATION

**DO1 Series
UNIVERSAL CARD
PART NO. SCHEDULE**

Board Thk.	2 Level Wrap	3 Level Wrap
1/16"	D012520	D012510
1/8"	D011520	D011510



